4-Mbit (128K x 36) Pipelined Sync SRAM

Features

- **Fully registered inputs and outputs for pipelined operation**
- **128K by 36 common I/O architecture**
- **3.3V core power supply**
- **2.5V/3.3V I/O operation**
- **Fast clock-to-output times**
  - **— 2.6 ns (for 250-MHz device)**
  - **— 2.6 ns (for 225-MHz device)**
  - **— 2.8 ns (for 200-MHz device)**
  - **— 3.5 ns (for 166-MHz device)**
  - **— 4.0 ns (for 133-MHz device)**
- **User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **JEDEC-standard 100-pin TQFP, 119-pin BGA and 165-pin fBGA packages**
- **"ZZ" Sleep Mode option and Stop Clock option**
- **Available in Industrial and Commercial temperature ranges**

Functional Description[1]

The CY7C1347F is a 3.3V, 128K by 36 synchronous-pipelined SRAM designed to support zero-wait-state secondary cache with minimal glue logic.

CY7C1347F I/O pins can operate at either the 2.5V or the 3.3V level, the I/O pins are 3.3V tolerant when V_{DDQ} = 2.5V.

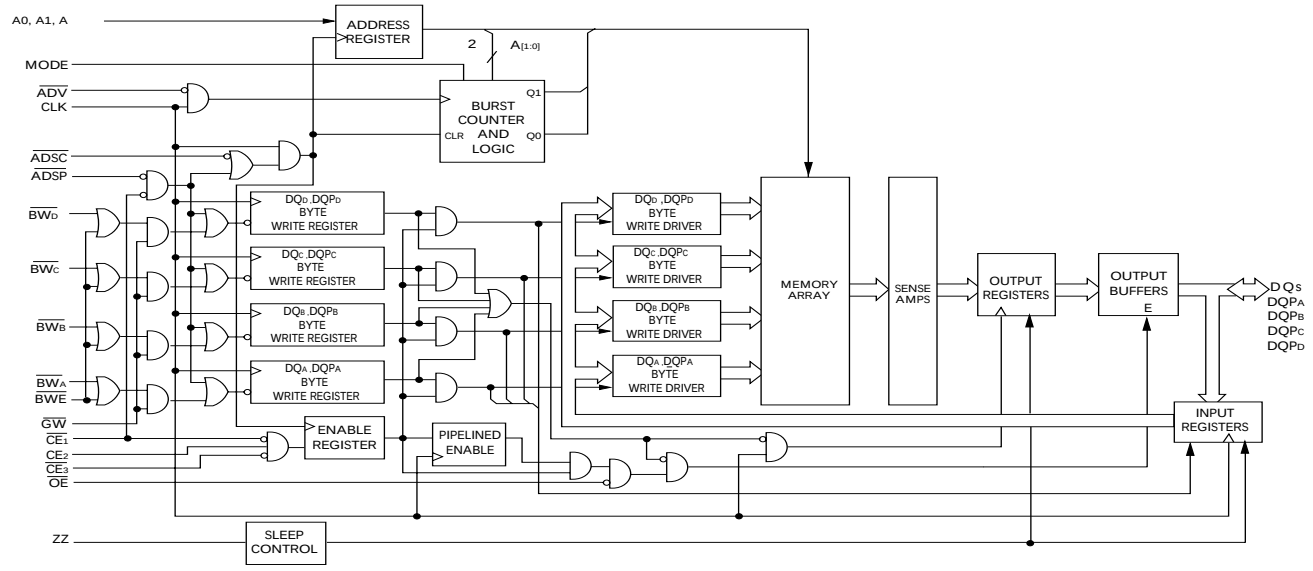
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 2.6 ns (250-MHz device)

CY7C1347F supports either the interleaved burst sequence used by the Intel Pentium processor or a linear burst sequence used by processors such as the PowerPC®. The burst sequence is selected through the MODE pin. Accesses can be initiated by asserting either the Address Strobe from Processor (ADSP) or the Address Strobe from Controller ($\overline{ADSC}$) at clock rise. Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the four Byte Write Select ($\overline{BW}_{[A:D]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to provide proper data during depth expansion, $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.

Logic Block Diagram



Note:
1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

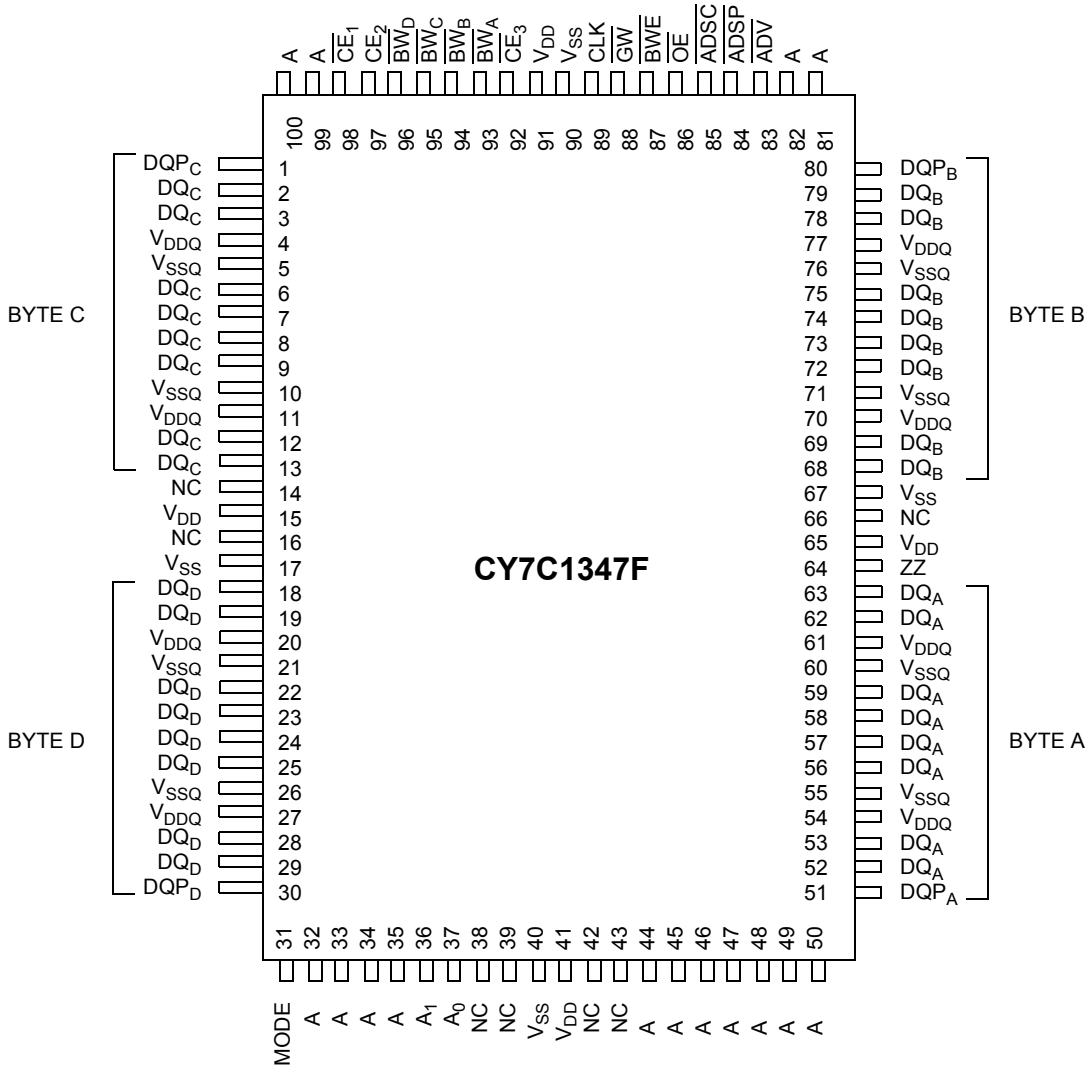
Selection Guide

	-250	-225	-200	-166	-133	Unit
Maximum Access Time	2.6	2.6	2.8	3.5	4.0	ns
Maximum Operating Current	325	290	265	240	225	mA
Maximum CMOS Standby Current	40	40	40	40	40	mA

Shaded areas contain advance information. Please contact your local Cypress Sales representative for availability of these parts.

Pin Configurations

100-Pin TQFP



Pin Configurations (continued)

119-Ball BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CE_2	A	$\overline{ADSC}$	A	$\overline{CE_3}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE_1}$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW_C}$	$\overline{ADV}$	$\overline{BW_B}$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW_D}$	NC	$\overline{BW_A}$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BWE}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

165-Ball fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE_1}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{CE_3}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC	A	CE_2	$\overline{BW_D}$	$\overline{BW_A}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	NC	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC	A	A	NC	A1	NC	A	A	A	NC
R	MODE	NC	A	A	NC	A0	NC	A	A	A	A

Pin Definitions

Name (BGA,FBGA)	Name (100TQFP)	I/O	Description
A_0,A_1,A	$A_{[16:0]}$	Input-Synchronous	**Address Inputs used to select one of the 128K address locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feeds the 2-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	$\overline{BW}_{[A:D]}$	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$).
$\overline{BWE}$	$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH.
CE_2	CE_2	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	$\overline{OE}$	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	$\overline{ADV}$	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	ZZ	Input-Asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQ_A, DQ_B DQ_C, DQ_D DQP_A, DQP_B, DQP_C, DQP_D	DQs DQPs	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQPs are placed in a three-state condition.
V_{DD}	V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	V_{SS}	Ground	**Ground for the core of the device**.
V_{DDQ}	V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
V_{SSQ}	V_{SSQ}	I/O Ground	**Ground for the I/O circuitry**.
MODE	MODE	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DDQ} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
NC	NC		**No Connects**.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (T_{CO}) is 2.6 ns (250-MHz device).

The CY7C1347F supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Address Strobe from Processor (ADSP) or the Address Strobe from Controller (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}_{[A:D]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. ADSP is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs ($A_{[16:0]}$) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the Output Register and onto the data bus within 2.6 ns (250-MHz device) if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output will three-state immediately.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active. The address presented to $A_{[16:0]}$ is loaded into the Address Register and the address advancement logic while being delivered to the RAM core. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_{[A:D]}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$-triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQs and DQPs inputs is written into the corresponding address location in the RAM core. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW}_{[A:D]}$ signals. The CY7C1347F provides byte write capability that is described in the Write Cycle Description table. Asserting the Byte Write Enable input ($\overline{BWE}$) with the selected Byte Write ($\overline{BW}_{[A:D]}$) input will selectively write to only the desired bytes.

Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1347F is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQs and DQPs inputs. Doing so will three-state the output drivers. As a safety precaution, DQs and DQPs are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_{[A:D]}$) are asserted active to conduct a write to the desired byte(s). ADSC-triggered write accesses require a single clock cycle to complete. The address presented to $A_{[16:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQs and DQPs is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1347F is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQs and DQPs inputs. Doing so will three-state the output drivers. As a safety precaution, DQs and DQPs are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1347F provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user-selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	ZZ ≥ V_{DD} − 0.2V		40	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} − 0.2V		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2V	$2t_{CYC}$		ns
t_{ZZI}	ZZ Active to snooze current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit snooze current	This parameter is sampled	0		ns

Truth Table[2, 3, 4, 5, 6]

Next Cycle	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	three-state
Deselect Cycle, Power-down	None	L	L	X	L	L	X	X	X	X	L-H	three-state
Deselect Cycle, Power-down	None	L	X	H	L	L	X	X	X	X	L-H	three-state
Deselect Cycle, Power-down	None	L	L	X	L	H	L	X	X	X	L-H	three-state
Deselect Cycle, Power-down	None	L	X	H	L	H	L	X	X	X	L-H	three-state
Snooze Mode, Power-down	None	X	X	X	H	X	X	X	X	X	X	three-state
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	three-state
WRITE Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	three-state
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	three-state
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	three-state
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	three-state
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	three-state

Notes:

2. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
3. $\overline{WRITE}$ = L when any one or more Byte Write enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte write enable signals (BW_A, BW_B, BW_C, BW_D), BWE, GW = H.
4. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. The SRAM always initiates a read cycle when $\overline{ADSP}$ asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_{[A:D]}}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to three-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are three-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table[2, 3, 4, 5, 6]

Next Cycle	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Partial Truth Table for Read/write[2, 7]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – DQ_A	H	L	H	H	H	L
Write Byte B – DQ_B	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C– DQ_C	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D– DQ_D	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Notes:
7. Table only lists a partial listing of the byte write combinations. Any combination of $BW_{[A:D]}$ is valid. Appropriate write will be done based on which byte write is active.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State..... –0.5V to V_{DD} + 0.5V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	3.3V –5%/+10%	2.5V –5% to V_{DD}
Ind'l	–40°C to +85°C		

Electrical Characteristics Over the Operating Range [8, 9]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OH} = –4.0 mA		2.4		V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OH} = –2.0 mA		2.0		V
V_{OL}	Output LOW Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OL} = 8.0 mA			0.4	V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OL} = 2.0 mA			0.7	V
V_{IH}	Input HIGH Voltage[8]	V_{DDQ} = 3.3V		2.0	V_{DD} + 0.3V	V
		V_{DDQ} = 2.5V		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[8]	V_{DDQ} = 3.3V		–0.3	0.8	V
		V_{DDQ} = 2.5V		–0.3	0.7	V
I_X	Input Load Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DDQ}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DDQ}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz		325	mA
			4.4-ns cycle, 225 MHz		290	mA
			5-ns cycle, 200 MHz		265	mA
			6-ns cycle, 166 MHz		240	mA
			7.5-ns cycle, 133 MHz		225	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz		120	mA
			4.4-ns cycle, 225 MHz		115	mA
			5-ns cycle, 200 MHz		110	mA
			6-ns cycle, 166 MHz		100	mA
			7.5-ns cycle, 133 MHz		90	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speeds		40	mA

Notes:
8. Overshoot: $V_{IH}(AC) < V_{DD} + 1.5V$ (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2V$ (Pulse width less than $t_{CYC}/2$).
9. $T_{Power\text{-}up}$: Assumes a linear ramp from 0v to V_{DD}(min.) within 200ms. During this time $V_{IH} \le V_{DD}$ and $V_{DDQ} \le V_{DD}$

Electrical Characteristics Over the Operating Range (continued)[8, 9]

Parameter	Description	Test Conditions		Min.	Max.	Unit
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or $V_{IN} \le 0.3V$ or $V_{IN} \ge V_{DDQ} - 0.3V$ $f = f_{MAX} = 1/t_{CYC}$	4-ns cycle, 250 MHz		105	mA
			4.4-ns cycle, 225 MHz		100	mA
			5-ns cycle, 200 MHz		95	mA
			6-ns cycle, 166 MHz		85	mA
			7.5-ns cycle, 133 MHz		75	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = 0			45	mA

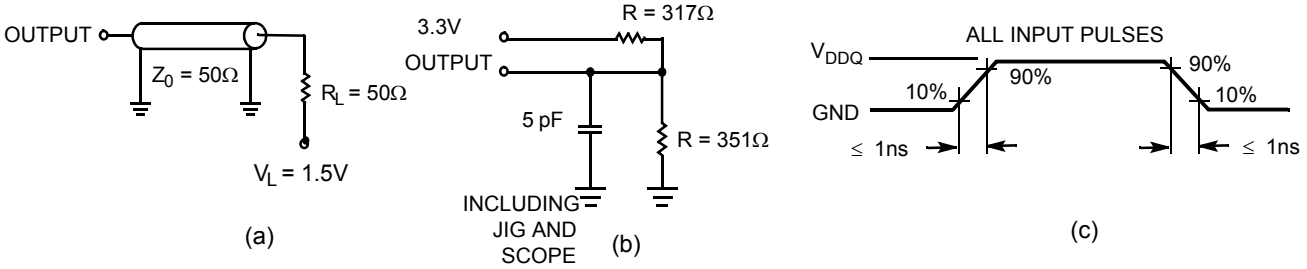
Shaded areas contain advance information.

Capacitance[10]

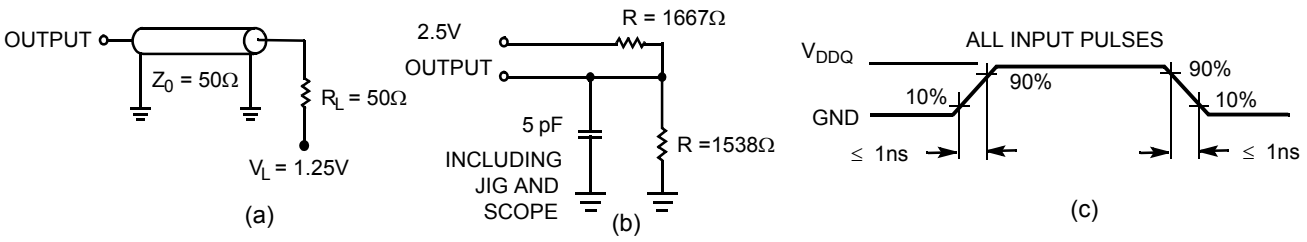
Parameter	Description	Test Conditions	TQFP Package	BGA Package	fBGA Package	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V. V_{DDQ} = 3.3V	5	5	5	pF
C_{CLK}	Clock Input Capacitance		5	5	5	pF
$C_{I/O}$	Input/Output Capacitance		5	7	7	pF

AC Test Loads and Waveforms

3.3V I/O Test Load



2.5V I/O Test Load



Thermal Resistance[10]

Parameter	Description	Test Conditions	TQFP Package	BGA Package	fBGA Package	Unit
Q_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	41.83	47.63	20.3	°C/W
Q_{JC}	Thermal Resistance (Junction to Case)		9.99	11.71	4.6	°C/W

Note:
10. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[15, 16]

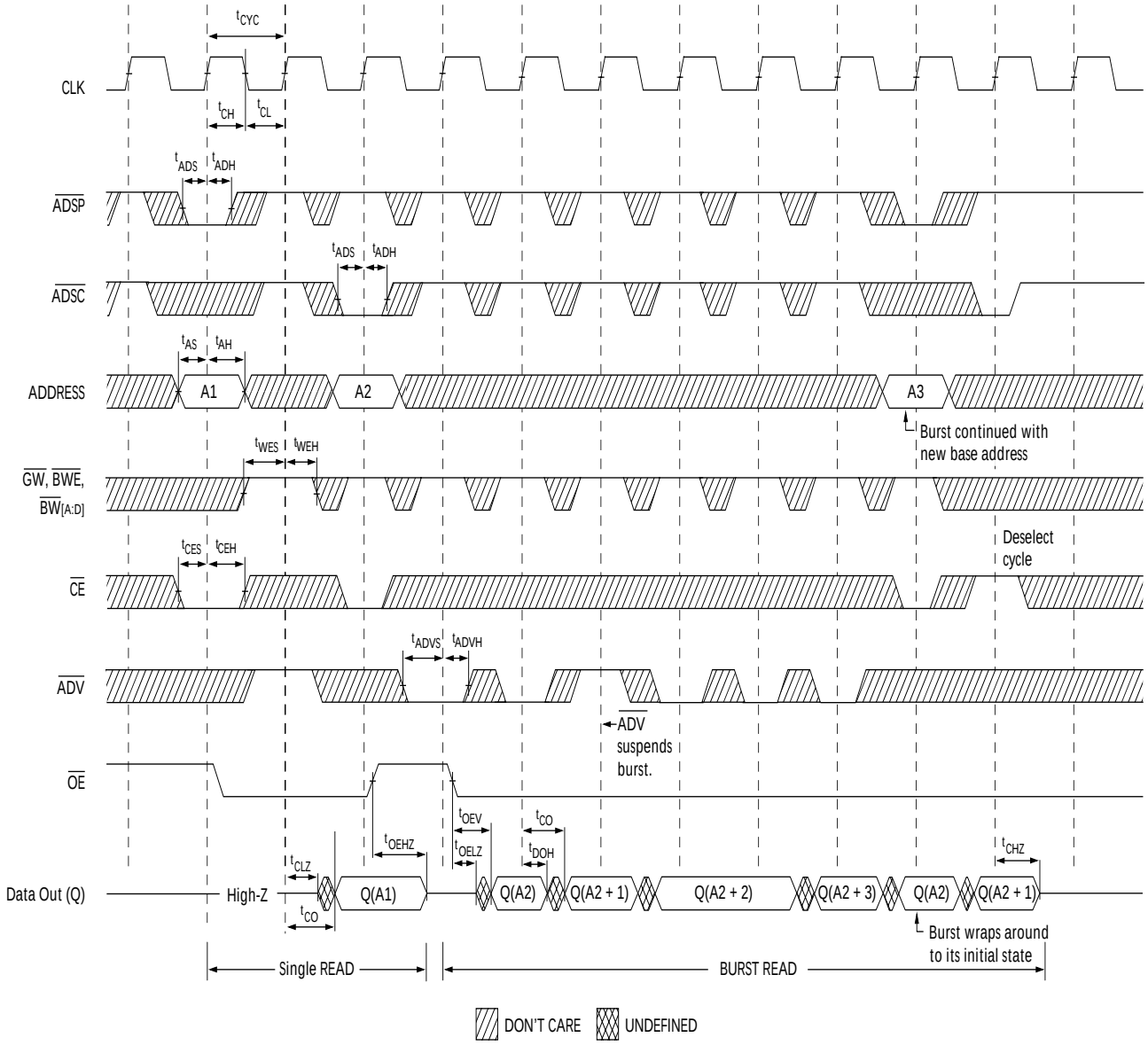
Parameter	Description	-250		-225		-200		-166		-133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{POWER}	V_{DD}(min.) to the first access read or write [11]	1		1		1		1		1		ms
t_{CYC}	Clock Cycle Time	4.0		4.4		5.0		6.0		7.5		ns
t_{CH}	Clock HIGH	1.7		2.0		2.0		2.5		3.0		ns
t_{CL}	Clock LOW	1.7		2.0		2.0		2.5		3.0		ns
t_{AS}	Address Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		ns
t_{AH}	Address Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		ns
t_{CO}	Data Output Valid After CLK Rise		2.6		2.6		2.8		3.5		4.0	ns
t_{DOH}	Data Output Hold After CLK Rise	1.0		1.0		1.0		2.0		2.0		ns
t_{WES}	$\overline{GW}$, $\overline{BWS}_{[3:0]}$ Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		ns
t_{WEH}	$\overline{GW}$, $\overline{BWS}_{[3:0]}$ Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		ns
t_{ALS}	ADV/$\overline{LD}$ Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.4		0.5		0.5		0.5		0.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		ns
t_{CES}	Chip Enable Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		ns
t_{CHZ}	Clock to High-Z[12, 13, 14]		2.6		2.6		2.8		3.5		4.0	ns
t_{CLZ}	Clock to Low-Z[12, 13, 14]	0		0		0		0		0		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[12, 13, 14]		2.6		2.6		2.8		3.5		4.0	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[12, 13, 14]	0		0		0		0		0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		2.6		2.6		2.8		3.5		4.5	ns

Notes:

11. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially before a read or write operation can be initiated.
12. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
13. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
14. This parameter is sampled and not 100% tested.
15. Timing references level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ} = 2.5V on all data sheets.
16. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

Switching Waveforms

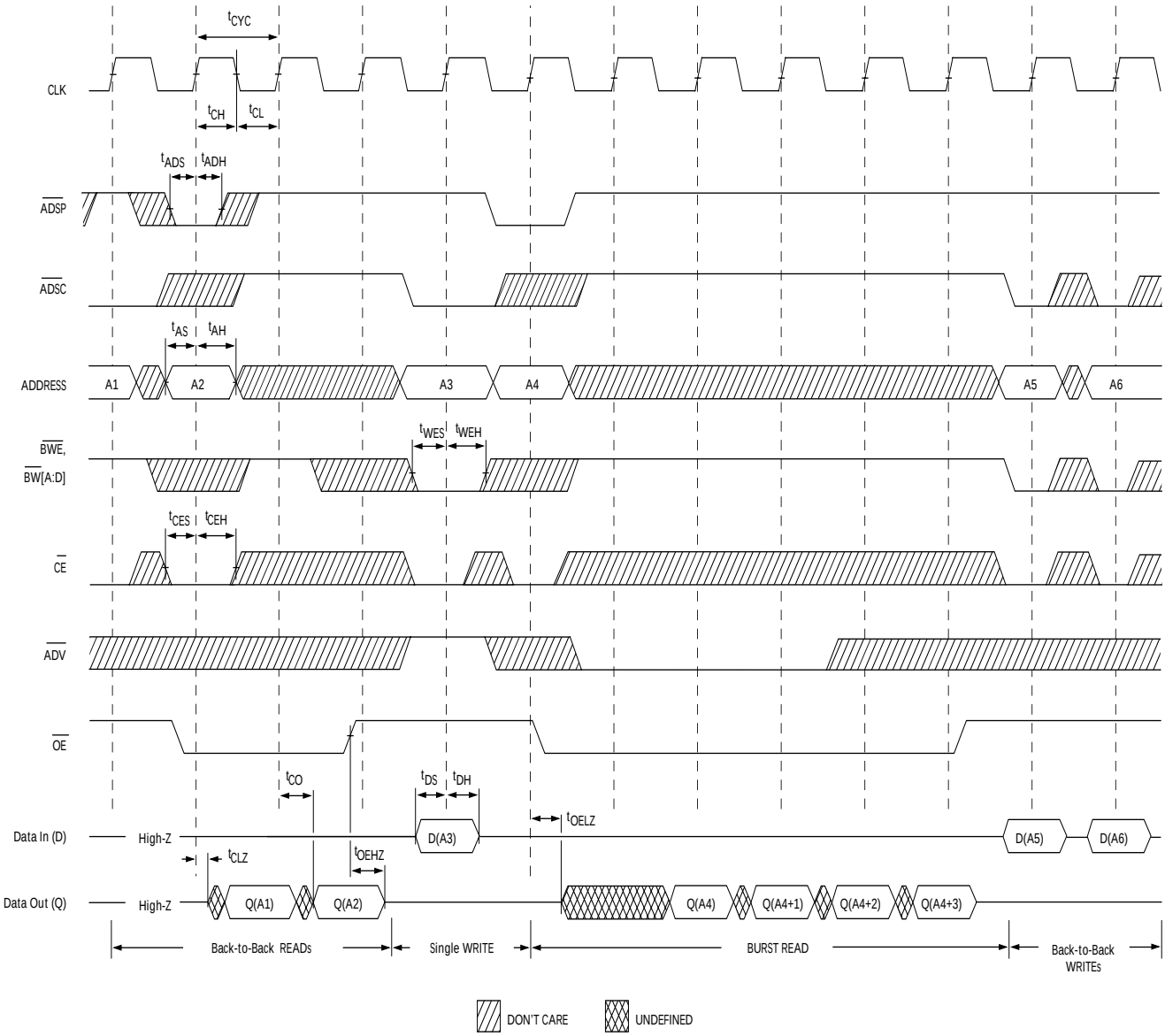
Read Cycle Timing[17]



Notes:
17. On this diagram when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
18. Full width write can be initiated by either $\overline{GW}$ LOW, or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $BW_{[A:D]}$ LOW.

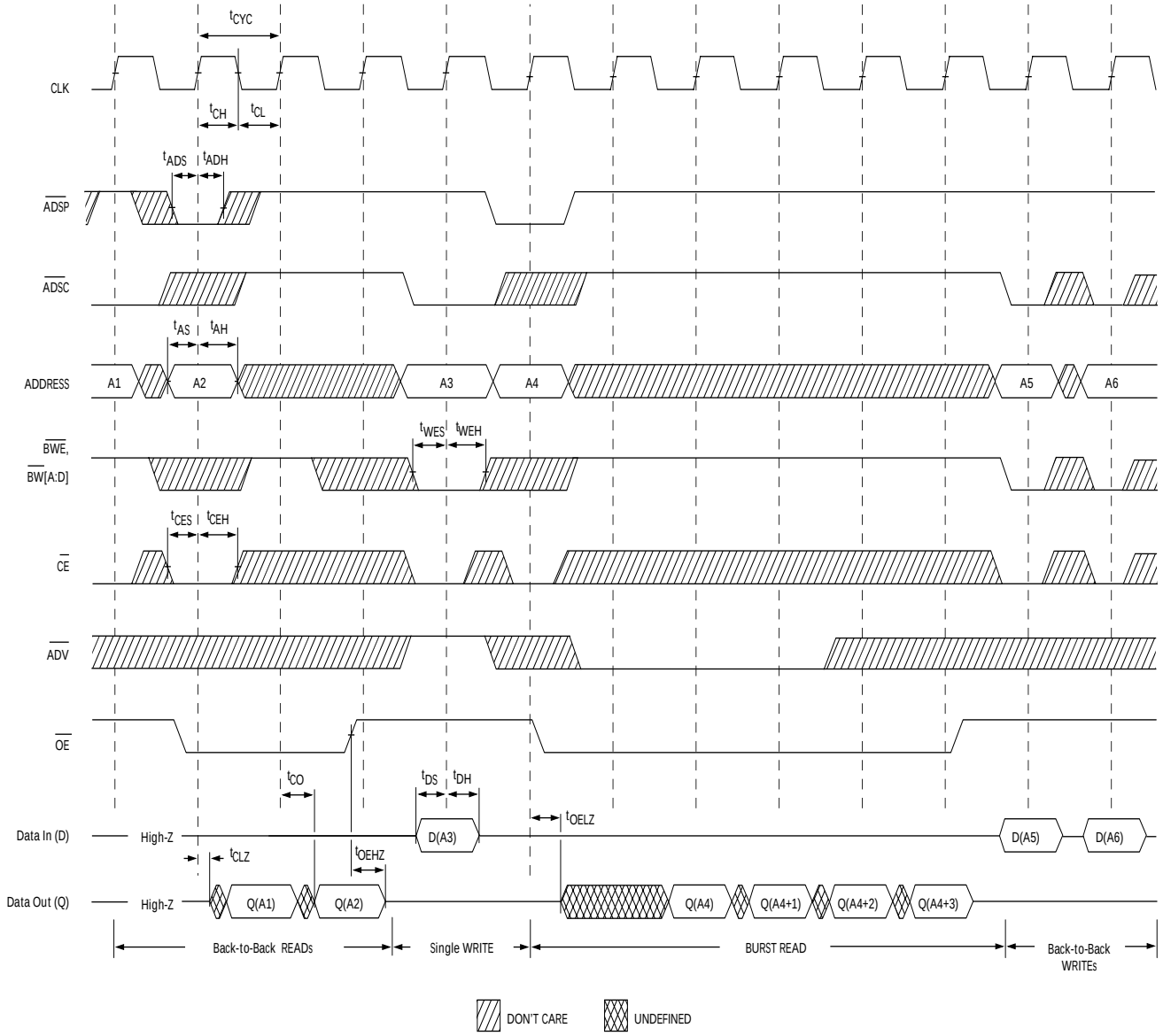
Switching Waveforms (continued)

Write Cycle Timing[17, 18]



Switching Waveforms (continued)

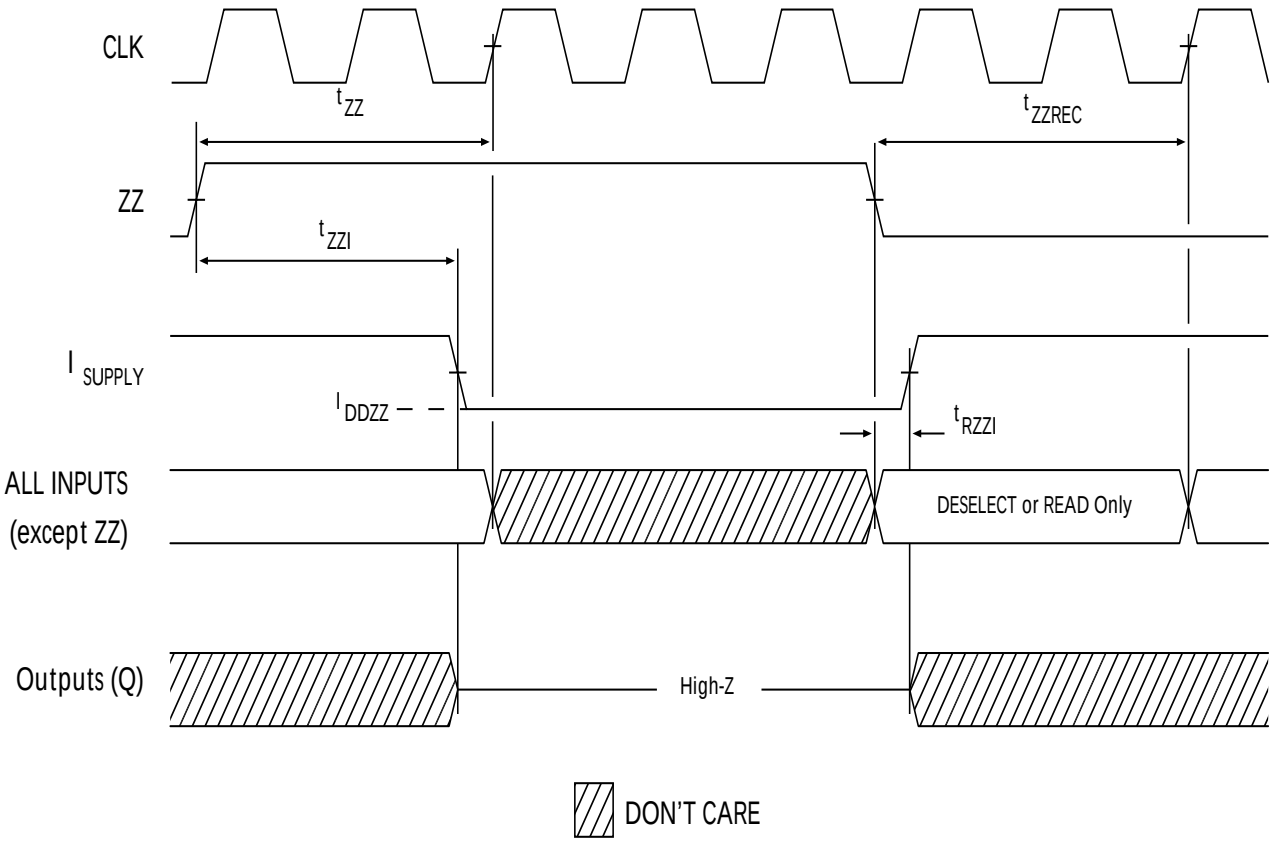
Read/Write Cycle Timing[17, 19, 20]



Note:
19. The data bus (Q)remains in high-Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
20. $\overline{GW}$ is HIGH

Switching Waveforms (continued)

ZZ Mode Timing [21, 22]



Notes:
21. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
22. DQs are in high-Z when exiting ZZ sleep mode.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CY7C1347F-250AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	CY7C1347F-250BGC	BG119	119-Ball BGA	
225	CY7C1347F-225AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	CY7C1347F-225BGC	BG119	119-Ball BGA	
200	CY7C1347F-200AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	CY7C1347F-200BGC	BG119	119-Ball BGA	
	CY7C1347F-200BZC	BB165C	165-Ball FBGA	
	CY7C1347F-200AI	A101	100-Lead Thin Quad Flat Pack	Industrial
	CY7C1347F-200BGI	BG119	119-Ball BGA	
166	CY7C1347F-166AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	CY7C1347F-166BGC	BG119	119-Ball BGA	
	CY7C1347F-166BZC	BB165C	165-Ball FBGA	
	CY7C1347F-166AI	A101	100-Lead Thin Quad Flat Pack	Industrial
	CY7C1347F-166BGI	BG119	119-Ball BGA	
133	CY7C1347F-133AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	CY7C1347F-133BGC	BG119	119-Ball BGA	
	CY7C1347F-133BZC	BB165C	165-Ball FBGA	
	CY7C1347F-133AI	A101	100-Lead Thin Quad Flat Pack	Industrial
	CY7C1347F-133BGI	BG119	119-Ball BGA	

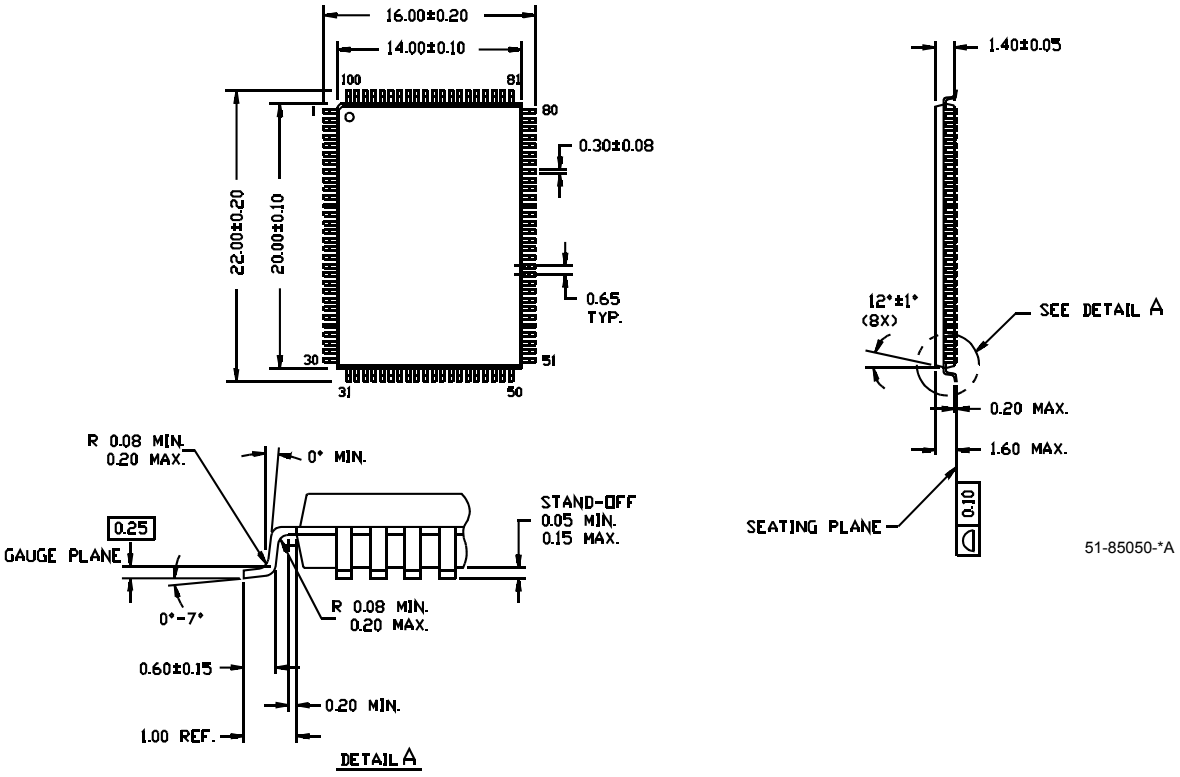
Shaded areas contain advance information.

Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

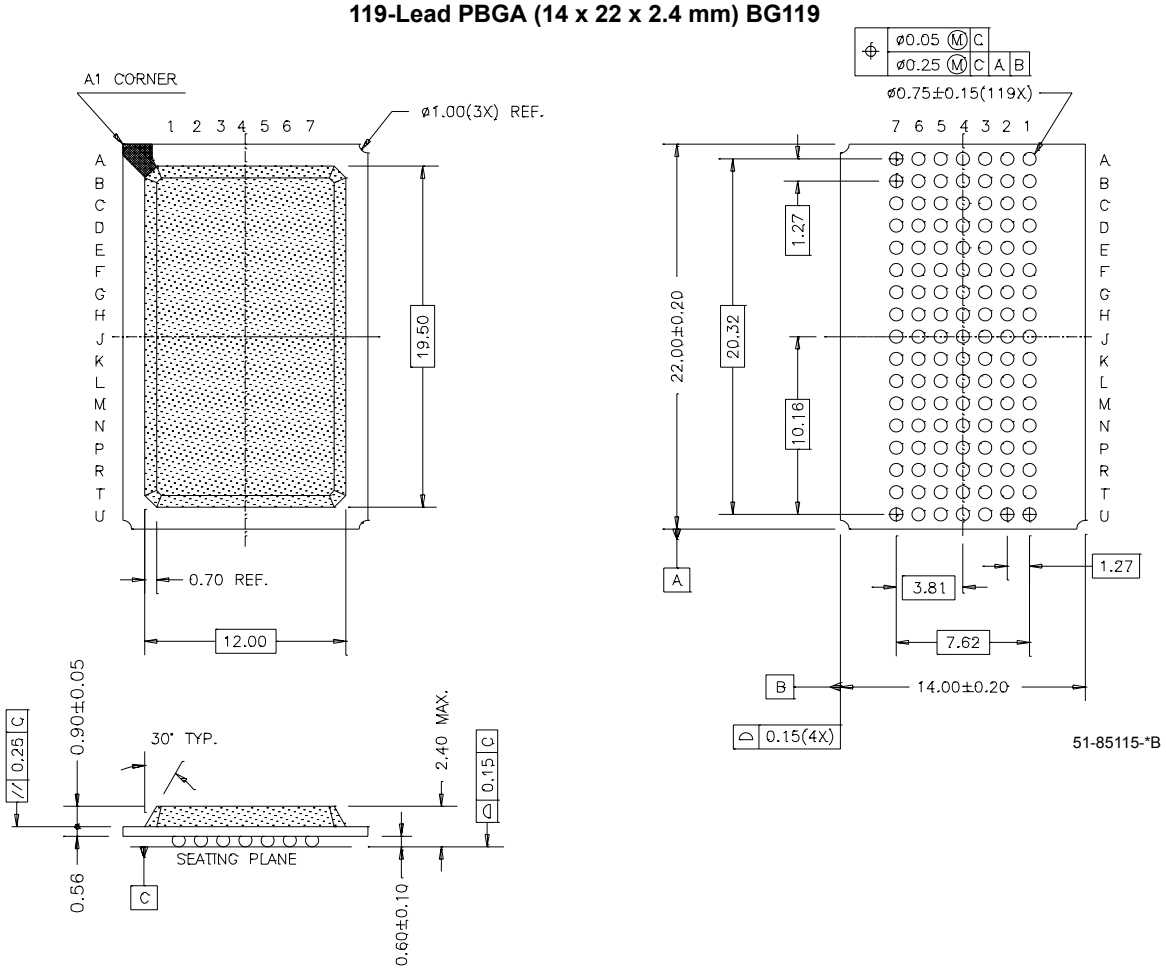
100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

DIMENSIONS ARE IN MILLIMETERS.



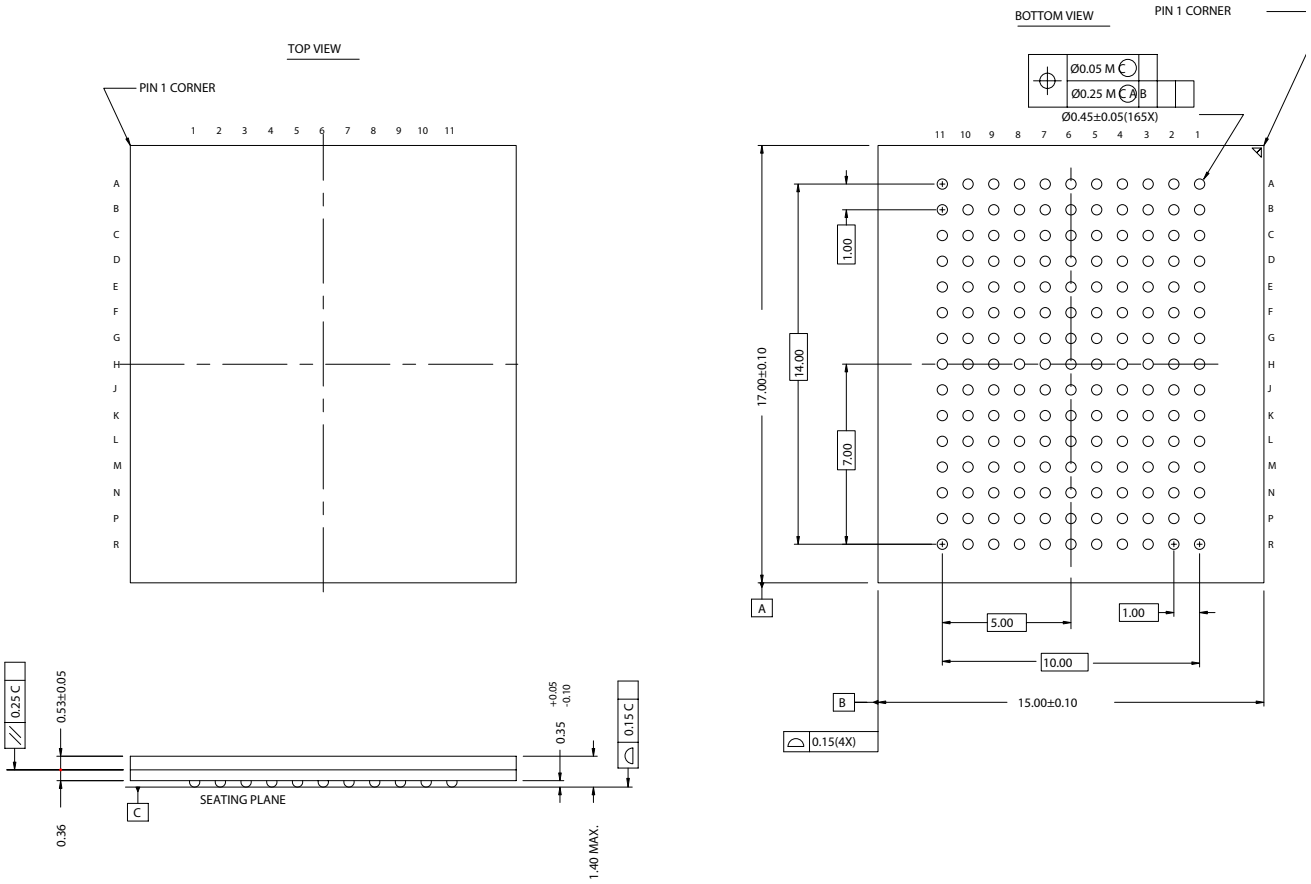
Package Diagrams (continued)

119-Lead PBGA (14 x 22 x 2.4 mm) BG119



Package Diagrams (continued)

165-Ball FBGA (15 x 17 x 1.20 mm) BB165C



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Document History Page

Document Title: CY7C1347F 4-Mbit (128K x 36) Pipelined Sync SRAM Document Number: 38-05213				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	119829	12/16/02	HGK	New Data Sheet
*A	123117	01/18/03	RBI	Added power-up requirements to AC test loads and waveforms information
*B	127632	06/13/03	DPM	Final Data Sheet
*C	200660	See ECN	SWI	Improvements: Updated thermal resistance and capacitance Updated R5 pin of 119-Ball BGA from V_{DD} to NC Updated all switching waveforms Clarifications: Updated footnotes Updated ZZ mode electrical characteristics
*D	213342	See ECN	VBL	Update Ordering Info section: Delete -100, shade -250, -225 Delete -100, Shade -250, -225 data from selection guide and characteristics