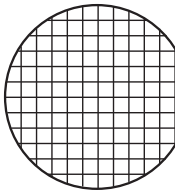
ST7LCRE4U1
ST7LCRDIE6

Full-speed USB MCU with smartcard interface

Features

- Clock, reset and supply management
  - Low voltage reset
  - Halt power saving mode
  - PLL for generating 48 MHz USB clock using a 4 MHz crystal
- USB (Universal Serial Bus) host interface
  - USB 2.0 compliant
  - CCID v1.0
  - Full speed, hubless
  - Bus-powered, low consumption
- ISO7816-3 UART Interface
  - 4 MHz clock generation
  - Synchronous/asynchronous protocols (T=0, T=1)
  - Automatic retry on parity error
  - Programmable baud rate from 372 to 11.625 clock pulses (D=32/F=372)
  - Card insertion/removal detection
- Smartcard power supply (V_{CRDVCC})
  - Fixed supply voltage: 1.8 V or 3 V



DIE

VFQFPN24(Y1)

- Development tools
  - Full hardware/software development package.
  - Fully compatible with Flash ST7FSCR family for development purposes
- ECOPACK® package

Description

ST7LCRE4U1 and ST7LCRDIE6 are 8-bit microcontrollers dedicated to smartcard reading applications. They have been developed to be the core of smartcard readers communicating through USB link. Optimized for mass-market applications, it offers a single integrated circuit solution with very few external components.

Table 1. Device summary

Features	Order codes	
	ST7LCRE4U1	ST7LCRDIE6
Program memory	16 Kbyte of ROM	
User RAM + USB data buffer	512 + 256 bytes	
Peripherals	USB full-speed (7 Ep), TBU, watchdog timer, ISO7816-3 interface	
Operating Supply	4.0 to 5.5 V	
Package	VFQFPN24	Die format (Refer to Die Specifications)
CPU Frequency	4 or 8 MHz	
Operating temperature	0°C to +70 °C	

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1 Device overview

The ST7LCRE4U1 and ST7LCRDIE6 devices are members of the ST7 microcontroller family designed for USB applications. All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

ST7LCRE4U1 and ST7LCRDIE6 are factory-programmed ROM devices.

They operate at a 4 MHz external oscillator frequency.

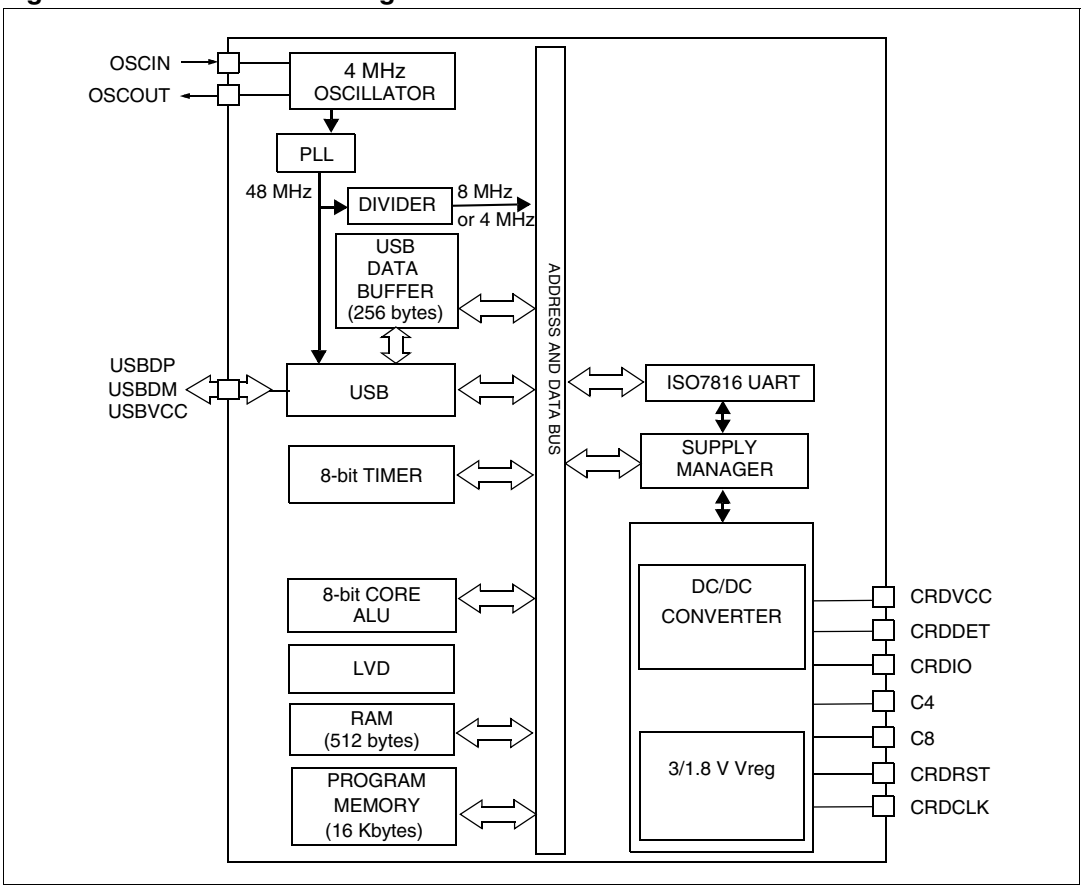
Under software control, all devices can be placed in Halt mode, to reduce power consumption when the application is in idle or standby state.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

The devices include an ST7 Core, up to 16 Kbytes of program memory, up to 512 bytes of user RAM and the following on-chip peripherals:

- USB full speed interface with 7 endpoints, programmable in/out configuration and embedded 3.3 V voltage regulator and transceivers (no external components are needed)
- ISO7816-3 UART interface with programmable baud rate from 372 clock pulses up to 11.625 clock pulses
- Internal voltage regulator able to provide a fixed supply voltage (V_{CRDVCC}) to smartcards. The voltage is selectable by option between 1.8 V and 3 V.
- Low voltage reset ensuring proper power-on or power-off of the device (selectable by option)
- 8-bit Timer (TBU)

Figure 1. ST7LCR block diagram



2 Pin description

Figure 2. 24-lead VFQFPN package pinout

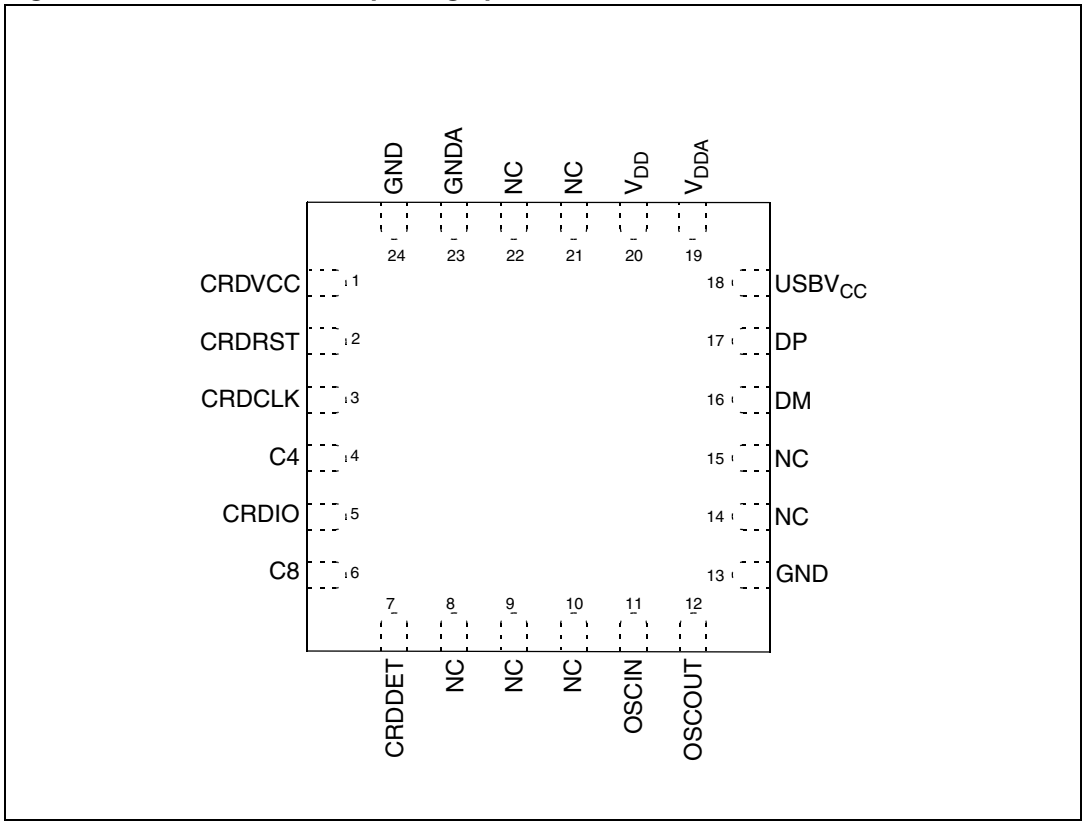


Table 2. Pin description

Pin number	Pin name	Type	Level		V_{CARD} supplied	Port/control				Main function (after reset)	Alternate function
						Input		Output			
VFQFPN24			Input	Output		wpu	int	OD	PP		
1	CRDVCC	O		C_T	X					Smartcard supply pin	
2	CRDRST	O		C_T	X				X	Smartcard reset	
3	CRDCLK	O		C_T	X				X	Smartcard clock	
4	C4	O		C_T	X				X	Smartcard C4	
5	CRDIO	I/O	C_T		X	X		X		Smartcard I/O	
6	C8	O		C_T	X				X	Smartcard C8	
7	CRDDET	I	C_T			X				Smartcard detection	
8	NC									Not used(1)	
9	NC									Not used(1)	
10	NC									Not used(1)	

Table 2. Pin description (continued)

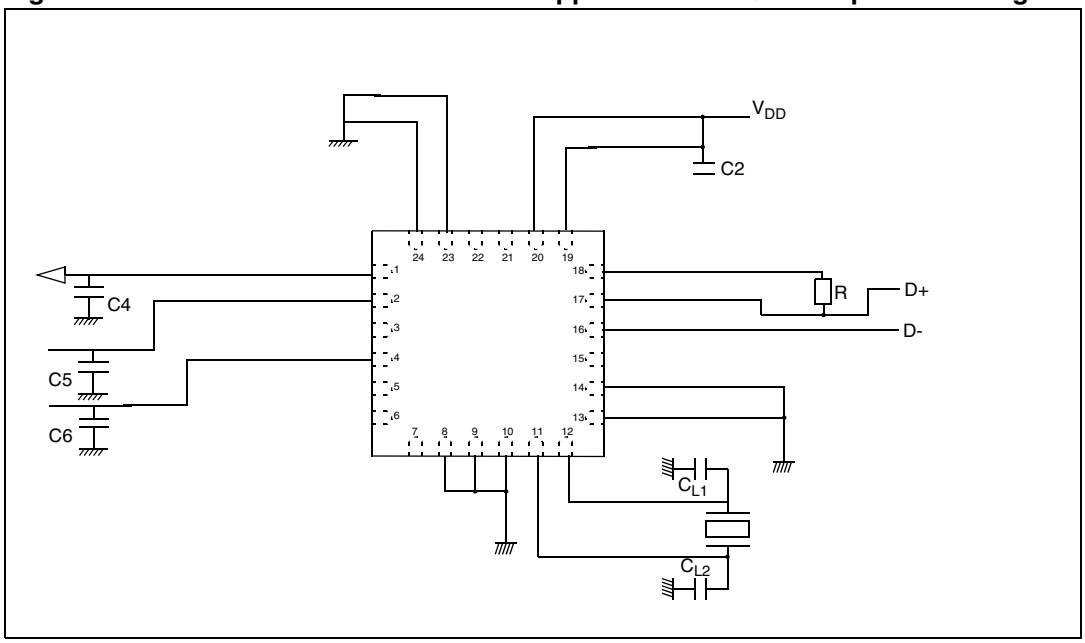
Pin number	Pin name	Type	Level		V_{CARD} supplied	Port/control				Main function (after reset)	Alternate function
						Input		Output			
VFQFPN24			Input	Output		wpu	int	OD	PP		
11	OSCIN		C_T							Input/Output oscillator pins. These pins connect a 4 MHz parallel-resonant crystal, or an external source to the on-chip oscillator.	
12	OSCOUT			C_T							
13	GND	S								Must be held low in normal operating mode.	
14	NC									Not used(1)	
15	NC									Not used	
16	DM	I/O	C_T							USB Data Minus line	
17	DP	I/O	C_T							USB Data Plus line	
18	USBVCC	O		C_T						3.3 V Output for USB	
19	V_{DDA}	S								Power supply voltage 4-5.5 V	
20	V_{DD}	S								Power supply voltage 4-5.5 V	
21	NC									Not used	
22	NC									Not used	
23	GNDA	S								Ground	
24	GND	S									

1. Pins 8,9,10, and 14 must be connected to ground.

Legend/abbreviations

- Type: I = input, O = output, S = supply
- In/Output level: C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
- Output level: HS = 10 mA high sink (on N-buffer only)
- Port and control configuration:
  - Input: float = floating, wpu = weak pull-up, int = interrupt, ana = analog
  - Output: OD = open drain, PP = push-pull

Figure 3. Smartcard interface reference application - VFQFPN24 pin block diagram



1. Mandatory values for the external components:
   C1 = 4.7 µF, C2 = 100 nF. C1 and C2 must be located close to the chip.
   C3 = 1 nF
   C4 = 4.7 µF, ESR = 0.5Ω
   C5 = 470 pF
   C6 =100 pF
   R = 1.5 kΩ
   L1 = 10 µH, 2 Ω
   Crystal 4.0 MHz, maximum impedance = 100 Ω
   Cl1, Cl2 (refer *Section 4.4.3: Crystal resonator oscillators*).
   D1: BAT42 Shottky

3 ST7LCR implementation

ST7LCRE4U1 and ST7LCRDIE6 offer single IC solutions and simplifies the integration of smartcard interfaces into smartcard readers.

3.1 Functionality

A dedicated analog block provides the power supply necessary to interface with the smartcards available on the market. The supply voltage can be selected by option between 1.8 V and 3 V (see *Section 6: Device configuration and ordering information*). A dedicated UART interface provides an IS07816 communication port for connection with the smartcard connector. A full-speed USB interface port allows external connection to a host computer.

3.2 Smartcard interface features

The ST7LCRE4U1 and ST7LCRDIE6 include the following features:

- Compatibility with asynchronous cards
- Compatibility with T=0 and T=1 protocols
- Compatibility with EMV and PC/SC modes.
- Compliance with ISO 7816-3 and 4 and ability to supply the cards with 1.8 V or 3 V (class A, B or C cards, respectively)
- Resume/wake-up mode upon smartcard insertion/removal

The reader is able to communicate with smartcards up to the maximum baud rate allowed, namely 344 086 bps (TA1=16) for a clock frequency of 4 MHz. Because the size of the smartcard buffer is 261 bytes, care must be taken not to exceed this size during APDU exchanges when the protocol in use is T=1.

4 Electrical characteristics

4.1 Absolute maximum ratings

This product contains devices for protecting the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid applying any voltage higher than the specified maximum rated voltages. For proper operation it is recommended that V_I and V_O be higher than V_{SS} and lower than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriate logic voltage level (V_{DD} or V_{SS}).

Power considerations

The average chip-junction temperature, T_J, in Celsius can be obtained from:

$$T_J = T_A + PD \times RthJA$$

where:

T_A = Ambient temperature

RthJA = Package thermal resistance (junction-to ambient)

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{DD} \times V_{DD}$ (chip internal power)

P_{PORT} = Port power dissipation determined by the user

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Ratings	Value	Unit
V_{DD} - V_{SS}	Supply voltage	6.0	V
V_{IN}	Input voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
V_{OUT}	Output voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
ESD	ESD susceptibility	2000	V
ESDCard	ESD susceptibility for card pads	4000	V
I_{VDD_I}	Total current into V_{DD_I} (source)	250	mA
I_{VSS_I}	Total current out of V_{SS_I} (sink)	250	

Warning: Direct connection to V_{DD} or V_{SS} of the I/O pins could damage the device in case of program counter corruption (due to unwanted change of the I/O configuration). To guarantee safe conditions, this connection has to be done through a typical 10kΩ pull-up or pull-down resistor.

Table 4. Thermal characteristics

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance VFQFPN24	42	°C/W
T_{Jmax}	Max. junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
PD_{max}	Power dissipation VFQFPN24	600	mW

4.2 Recommended operating conditions

Operating conditions are given for T_A = 0 to +70 °C unless otherwise specified.

4.2.1 General operating conditions

Table 5. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		4.0		5.5	V
f_{OSC}	External clock source				16	MHz
T_A	Ambient temperature range		0		70	°C

4.2.2 Current injection

Positive injection

The positive injection current, I_{INJ+}, is **applied** through protection diodes insulated from the substrate of the die.

Negative injection

The negative injection current, I_{INJ-}, is **applied** through protection diodes NOT INSULATED from the substrate of the die. The drawback is a small leakage of few µA induced inside the die when a negative injection is performed. This leakage is tolerated by the digital structure. The effect depends on the pin which is submitted to the injection. Of course, external digital signals applied to the component must have a maximum impedance close to 50 kΩ.

Pure digital pins can tolerate a negative current injection of 1.6 mA. In addition, the best choice is to inject the current as far as possible from the analog input pins.

Note: When several inputs are submitted to a current injection, the maximum injection current is the sum of the positive (respectively negative) currents (instantaneous values).

Refer to *Table 6* for the values of I_{INJ-} and I_{INJ+}.

Table 6. Current injection on I/O port and control pins

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{INJ+}	Total positive injected current(1)	$V_{EXTERNAL} > V_{DD}$ (standard I/Os)				20	mA
		$V_{EXTERNAL} > V_{CRDVCC}$ (smartcard I/Os)				20	mA
I_{INJ-}	Total negative injected current	$V_{EXTERNAL} < V_{SS}$	Digital pins			20	mA
			Analog pins			20	mA

1. For smartcard I/Os, V_{CRDVCC} has to be considered.

4.2.3 Current consumption

Table 7 are measured at TA=0 to +70°C, and VDD-VSS=5.5 V unless otherwise specified.

Table 7. Current consumption(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current in Run mode(2)	f_{OSC} = 4 MHz		10	15	mA
	Supply current in suspend mode	External I_{LOAD} = 0 mA (USB transceiver enabled)			500	µA
	Supply current in Halt mode	External I_{LOAD} = 0 mA (USB transceiver disabled)		50	100	

1. All I/O pins are in input mode with a static value at V_{DD} or V_{SS}. Clock input (OSCIN) is driven by external square wave.
2. CPU running with memory access, all I/O pins in input mode with a static value at V_{DD} or V_{SS}; clock input (OSCIN) driven by external square wave.

4.2.4 I/O port pin characteristics

Table 8 characteristics are measured at TA=0 to +70°C. Voltages are referred to V_{SS} unless otherwise specified.

Table 8. I/O port pins characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5 V			$0.3V_{DD}$	V
V_{IH}	Input high level voltage	V_{DD} = 5 V	$0.7V_{DD}$			
V_{HYS}	Schmidt trigger voltage hysteresis(1)			400		mV
V_{OL}	Output low level voltage for Standard I/O port pins	I=-5 mA			1.3	V
		I=-2 mA			0.4	
V_{OH}	Output high level voltage	I=3 mA	V_{DD}-0.8			
I_L	Input leakage current	$V_{SS}<V_{PIN}<V_{DD}$			1	µA
R_{PU}	Pull-up equivalent resistor		50	90	170	kΩ

Table 8. I/O port pins characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{OHL}	Output high to low level fall time for high sink I/O port pins (Port D)(2)	C_l=50 pF	6	8	13	ns
t_{OHL}	Output high to low level fall time for standard I/O port pins (Port A, B or C)(2)		18		23	
t_{OLH}	Output low-high rise time (Port D)(2)		7	9	14	
t_{OLH}	Output low-high rise time for standard I/O port pins (Port A, B or C)(2)		19		28	
t_{ITEXT}	External interrupt pulse time		1			t_{CPU}

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
2. Guaranteed by design, not tested in production.

4.3 Supply and reset characteristics

Table 9 characteristics are measured for T_A = 0 to +70 °C, and V_{DD} - V_{SS} = 5.5 V unless otherwise specified.

Table 9. Low voltage detector and supervisor (LVDs)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IT+}	Reset release threshold (V_{DD} rising)			3.7	3.9	V
V_{IT-}	Reset generation threshold (V_{DD} falling)		3.3	3.5		V
V_{hys}	Hysteresis V_{IT+} - V_{IT-}(1)			200		mV
V_{tPOR}	V_{DD} rise time rate(1)		20			ms/V

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.

4.4 Clock and timing characteristics

4.4.1 General timings

Table 10 are measured at TA=0 to +70 °C unless otherwise specified.

Table 10. General timings

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
$t_{c(INST)}$	Instruction cycle time		2	3	12	t_{CPU}
		f_{CPU}=4 MHz	500	750	3000	ns
$t_{v(IT)}$	Interrupt reaction time $t_{v(IT)} = \Delta t_{c(INST)} + 10$ (2)		10		22	t_{CPU}
		f_{CPU}=4 MHz	2.5		5.5	µs

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

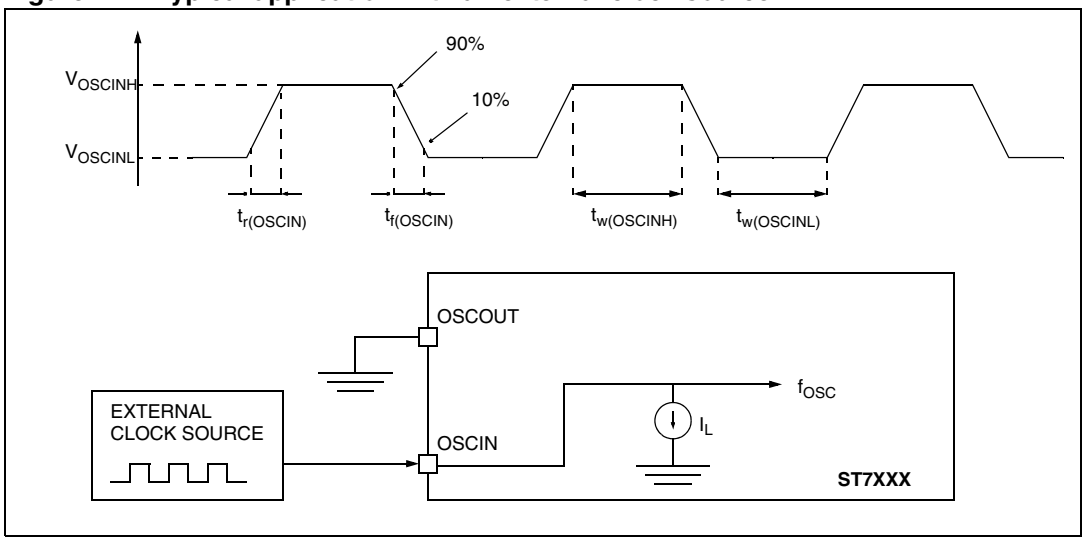
4.4.2 External clock source

Table 11. External clock source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OSCINH}	OSCIN input pin high level voltage	see *Figure 4*	$0.7V_{DD}$		V_{DD}	V
V_{OSCINL}	OSCIN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(OSCINH)}$ $t_{w(OSCINL)}$	OSCIN high or low time(1)		15			ns
$t_{r(OSCIN)}$ $t_{f(OSCIN)}$	OSCIN rise or fall time				15	
I_L	OSCx Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 4. Typical application with an external clock source



4.4.3 Crystal resonator oscillators

The ST7 internal clock is supplied with one Crystal resonator oscillator. All the information given in this paragraph are based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 12. Crystal resonator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{OSC}	Oscillator Frequency(1)	MP: Medium power oscillator			4		MHz
R_F	Feedback resistor			90		150	kΩ
C_{L1} C_{L2}	Recommended load capacitances versus equivalent serial resistance of the crystal resonator (R_S)	See *Table 14*	(MP oscillator)	22		56	pF
i_2	OSCOUT driving current	V_{DD}=5 V V_{IN}=V_{SS}	(MP oscillator)	1.5		3.5	mA

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value. Contact crystal resonator manufacturer for more details.

Table 13. Typical crystal resonator characteristics

Oscillator		Reference		Freq.	Characteristic(1)	C_{L1} (pF)	C_{L2} (pF)	$t_{SU(osc)}$ (ms)(2)
Crystal	MP	JAUCH	SS3-400-30-30/30	4 MHz	Δf_{OSC}=[±30ppm$_{25°C}$,±30ppm$_{\Delta Ta}$] (Typ) R_S=60 Ω	33	33	7~10

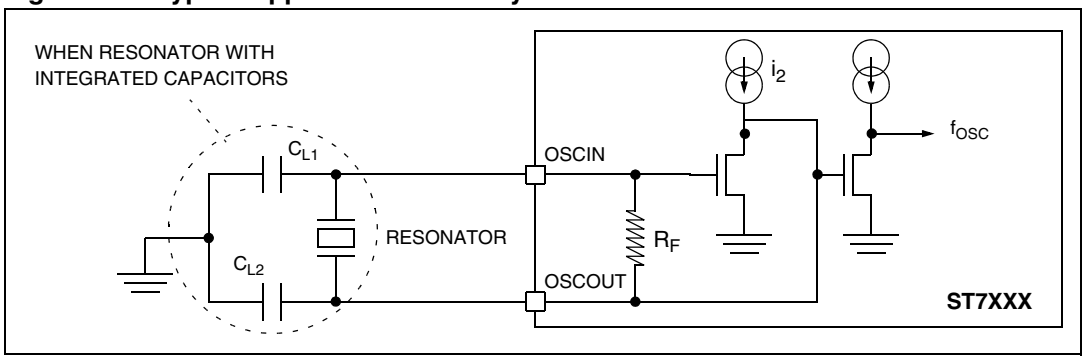
1. Resonator characteristics given by the crystal resonator manufacturer.
2. $t_{SU(OSC)}$ is the typical oscillator start-up time measured between V_{DD} = 2.8 V and the fetch of the first instruction (with a quick V_{DD} ramp-up from 0 to 5 V (<50 µs).

Table 14. Recommended values for 4 MHz crystal resonator

Symbol	Min	Typ	Max
R_{SMAX}(1)	20 Ω	25 Ω	70 Ω
C_{OSCIN}	56 pF	47 pF	22 pF
C_{OSCOUT}	56 pF	47 pF	22 pF

1. R_{SMAX} is the equivalent serial resistor of the crystal (see crystal specification).

Figure 5. Typical application with a crystal resonator



4.5 Memory characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 15. RAM and hardware registers characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or Reset)	2			V

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Not tested in production.

4.6 Smartcard supply supervisor electrical characteristics

Table 16 characteristics are measured for T_A = 0 to +70 °C, and 4.0 < V_{DD} - V_{SS} < 5.5 V unless otherwise specified.

Table 16. Smartcard supply supervisor electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
3 V regulator output (for IEC7816-3 class B cards)						
V_{CRDVCC}	Smartcard power supply voltage		2.7	3.0	3.3	V
I_{SC}	Smartcard supply current				50	mA
I_{OVDET}	Current overload detection				100(1)	mA
t_{IDET}	Detection time on current overload		170(1)		1400(1)	µs
t_{OFF}	V_{CRDVCC} turn off time	$C_{LOADmax}$≤4.7 µF			750	µs
t_{ON}	V_{CRDVCC} turn on time	$C_{LOADmax}$ ≤ 4.7 µF		150	500	µs
1.8 V regulator output (for IEC7816-3 Class C cards)						
V_{CRDVCC}	Smartcard power supply voltage		1.65	1.8	1.95	V
I_{SC}	Smartcard supply current				20	mA
I_{OVDET}	Current overload detection				100(1)	mA
t_{IDET}	Detection time on current overload		170(1)		1400(1)	µs
t_{OFF}	V_{CRDVCC} turn off time	$C_{LOADmax}$ ≤ 4.7 µF			750	µs

Table 16. Smartcard supply supervisor electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ON}	V_{CRDVCC} turn on time	$C_{LOADmax} \leq 4.7$ µF		150	500	µs
Smartcard CLKpin						
V_{OL}	Output low level voltage	I=-50 µA	-	-	0.4(1)	V
V_{OH}	Output high level voltage	I=50 µA	V_{CRDVCC}-0.5(1)	-	-	V
T_{OHL}	Output high-low fall time(1)	C_l=30 pF	-		20	ns
T_{OLH}	Output low-high rise time(1)	C_l=30 pF	-		20	ns
F_{VAR}	Frequency variation(1)		-		1	%
F_{DUTY}	Duty cycle(1)		45		55	%
P_{OL}	Signal low perturbation(1)		-0.25		0.4	V
P_{OH}	Signal high perturbation(1)		V_{CRDVCC}-0.5		V_{CRDVCC}+0.25	V
I_{SGND}	Short-circuit to ground(1)			15		mA
Smartcard I/O pin						
V_{IL}	Input low level voltage		-	-	0.5(1)	V
V_{IH}	Input high level voltage		0.6V_{CRDVCC}(1)	-	-	V
V_{OL}	Output low level voltage	I=-0.5 mA	-	-	0.4 (1)	V
V_{OH}	Output high level voltage	I=20 µA	0.8V_{CRDVCC}(1)	-	V_{CRDVCC}(1)	V
I_L	Input leakage current (1)	$V_{SS}<V_{IN}<V_{SC\_PWR}$	-10	-	10	µA
I_{RPU}	Pull-up equivalent resistance	$V_{IN}=V_{SS}$		24	30	kΩ
T_{OHL}	Output high-low fall time(1)	C_l=30 pF	-		0.8	µs
T_{OLH}	Output low-high rise time(1)	C_l=30 pF	-		0.8	µs
I_{SGND}	Short-circuit to ground(1)			15		mA
Smartcard RST C4 and C8 pin						
V_{OL}	Output low level voltage	I=-0.5 mA	-	-	0.4(1)	V
V_{OH}	Output high level voltage	I=20 µA	V_{CRDVCC}-0.5(1)	-	V_{CRDVCC}(1)	V
T_{OHL}	Output high-low fall time(1)	C_l=30 pF	-		0.8	µs
T_{OLH}	Output low-high rise time(1)	C_l=30 pF	-		0.8	µs
I_{SGND}	Short-circuit to ground(1)			15		mA

1. Data based on characterization results, not tested in production.

4.7 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.7.1 Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre-qualification tests in relation with the EMC level requested for his application.

- Software recommendations

  The software flowchart must include the management of runaway conditions such as:

  – Corrupted program counter
  – Unexpected reset
  – Critical Data corruption (control registers...)

- Pre-qualification trials

  Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the Reset pin or the Oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 17. EMS characteristics

Symbol	Parameter	Conditions	Level/ class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5 V, T_A=+25 °C, f_{OSC}=8 MHz conforms to IEC 1000-4-2	2B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5 V, T_A=+25 °C, f_{OSC}=8 MHz conforms to IEC 1000-4-4	4B

4.7.2 Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 18. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. $[f_{OSC}/f_{CPU}]$(1)		Unit
				4/8MHz	4/4MHz	
S_{EMI}	Peak level	V_{DD}=5 V, T_A=+25 °C, conforming to SAE J 1752/3	0.1 MHz to 30 MHz	19	18	dBµV
			30 MHz to 130 MHz	32	27	
			130 MHz to 1 GHz	31	26	
			SAE EMI Level	4	3.5	-

1. Data based on characterization results, not tested in production.

4.7.3 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). The Human Body Model is simulated. This test conforms to the JESD22-A114A standard.

Table 19. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A=+25 °C	2000	V

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply over-voltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electrostatic discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected

as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 20. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A=+25 °C	A
DLU	Dynamic latch-up class	V_{DD}=5.5 V, f_{OSC}=4 MHz,T_A=+25 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

4.8 Communication interface characteristics

Table 21. USB DC electrical characteristics

Parameter	Symbol	Conditions	Min.	Max.	Unit
Input levels					
Differential input sensitivity	VDI	I(D+, D-)	0.2		V
Differential common mode range	VCM	Includes VDI range	0.8	2.5	V
Single ended receiver threshold	VSE		1.3	2.0	V
Output levels					
Static output low	VOL	RL of 1.5 kΩ to 3.6 V(1)		0.3	V
Static output high	VOH	RL of 15 kΩ to V_{SS}(1)	2.8	3.6	V
USBVCC: voltage level	USBV	V_{DD}=5 V	3.00	3.60	V

1. R_L is the load connected on the USB drivers. All the voltages are measured from the local ground potential.

Figure 6. USB data signal rise and fall time

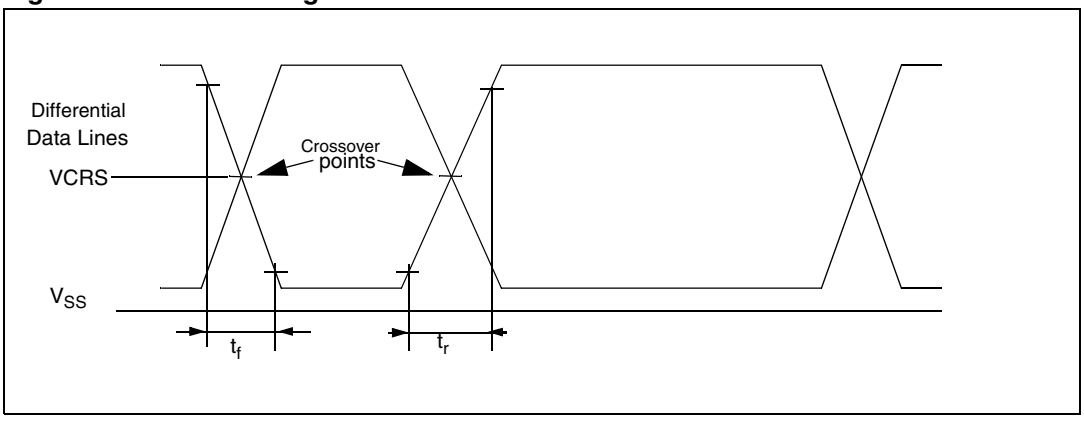


Table 22. USB full-speed electrical characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Driver characteristics					
Rise time(1)	t_r	CL=50 pF	4	20	ns
Fall time(1)	t_f	CL=50 pF	4	20	ns
Rise/ fall time matching	t_{rfm}	t_r/t_f	90	110	%
Output signal crossover voltage	VCRS		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to Chapter 7 (Electrical) of the USB specification (version 1.1).

5 Package characteristics

In order to meet environmental requirements, ST offers this device in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 Package mechanical data

Figure 7. 24-lead very thin fine pitch quad flat no-lead 5x5 mm 0.65 mm pitch, package outline

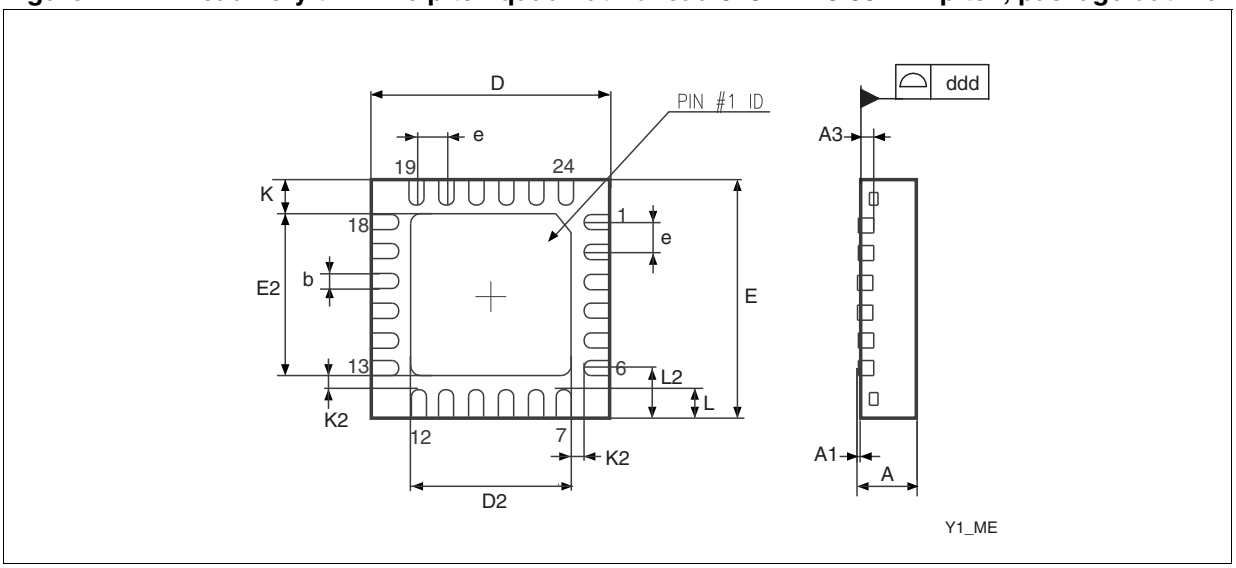


Table 23. 24-lead very thin fine pitch quad flat no-lead 5x5mm,0.65mm pitch, mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0.000	0.020	0.050	0.0000	0.0010	0.0020
A3		0.020			0.0008	
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D		5.000			0.1969	
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
E		5.000			0.1969	
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
e		0.650			0.0256	
L	0.350	0.450	0.550	0.0138	0.0177	0.0217
L2	0.870	0.875	0.880	0.0343	0.0344	0.0346
ddd		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5.2 Recommended reflow oven profile

Refer to JEDEC specification JSTD020D for a description of the recommended reflow oven profile for these packages.

6 Device configuration and ordering information

Device ordering information and transfer of customer code

Customer code is made up of the ROM contents and the list of the selected options (if any). The ROM contents are to be sent on diskette, or by electronic means, with the hexadecimal file in .S19 format generated by the development tool. All unused bytes must be set to FFh.

The selected options are communicated to STMicroelectronics using the correctly completed option list appended. See *Figure 8: ST7LCR option list*.

Refer to application note AN1635 for information on the counter listing returned by ST after code has been transferred.

The STMicroelectronics Sales Organization will be pleased to provide detailed information on contractual points.

Table 24. Ordering information

Sales type	Program memory (bytes)	RAM (bytes)	Package
ST7LCRE4U1/xxx(1)	16K ROM	768	VFQFPN24
ST7LCRDIE6/xxx(1)	16K ROM	768	Die

1. Customer ROM code name is assigned by STMicroelectronics.

Figure 8. ST7LCR option list

```
                        ST7LCR MICROCONTROLLER OPTION LIST
                            (Last update: October 2007)


Customer: . . . . . .
Address:  . . . . . .
          . . . . . .
Contact:  . . . . . .
Phone No: . . . . . .

Reference/ROM Code* :
*The ROM code name is assigned by STMicroelectronics.
ROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device Type/Memory Size/Package (check only one option)

-------------------------------------------------
ROM Device:       |     16K
-------------------------------------------------
VFQFPN24:         |     [ ] ST7LCRE4U1
DIE24:            |     [ ] ST7LCRDIE6


Conditioning (check only one option)      :

-------------------------------------------------
Packaged Product:             |     Die Product
-------------------------------------------------
[ ] Tray (VFQFPN package only)|     [ ] Tape & Reel
                              |     [ ] Waffle pack
                              |     [ ] Sawn wafer on sticky foil
                              |     [ ] Inked wafer

Special Marking:  [ ] No      [ ] Yes "_ _ _ _ _ _ _ _ _ _ "
Authorized characters are letters, digits, '.', '-', '/' and spaces only.

Maximum character count: VFQFPN24 (7 char. max)   : _ _ _ _ _ _ _

Vcc Card:               CRDVCC      [ ] 1.8V
                                    [ ] 3.0V

Watchdog:               WDGSW       [ ] Software Activation
                                    [ ] Hardware Activation
Nested Interrupts       NEST        [ ] Nested Interrupts
                                    [ ] Non Nested Interrupts
ISO Clock Source        ISOCLK      [ ] Oscillator
                                    [ ] Divider
No. of Retries          RETRY       [ ] 5
                                    [ ] 4
Readout Protection:     FMP_R       [ ] Disabled
                                    [ ] Enabled

Date      . . . . . .    Signature . . . . . .
```

7 Revision history

Table 25. Document revision history

Date	Revision	Changes
26-Aug-06	0.1	Initial release
26-Mar-07	0.2	QFN24 package added Option List added External clock source frequency modified (to maximum value), *Section 4.2* Die sales type added to *Table* Note added to *Table 2* (NC pins must be connected to ground)
23-Oct-2007	1	Document reformatted. Replaced ST7LCR by ST7LCRE4U1and ST7LCRDIE6. ECOPACK text added. Changed “selectable card V_{CC}” into “fixed card V_{CC}”. 5 V removed in *Section : Features*, *Section 3: ST7LCR implementation* and *Table 16: Smartcard supply supervisor electrical characteristics*. Changed QFN24 into VFQFPN24. Added *Figure 6: Device configuration and ordering information*. CRDC4 and CRDC8 renamed C4 and C8 respectively in *Figure 1: ST7LCR block diagram*. Removed LED functional block and LEDO pin from *Figure 1: ST7LCR block diagram*. LEDO pin left unconnected in *Figure 2: 24-lead VFQFPN package pinout* and *Table 2: Pin description*, and *Figure 3: Smartcard interface reference application - VFQFPN24 pin block diagram*. Removed mention of external LEDS in *Section 3.1: Functionality*. SLEF and DIODE pins removed from *Figure 1: ST7LCR block diagram*, and left unconnected in *Figure 2: 24-lead VFQFPN package pinout*,*Table 2: Pin description*, and *Figure 3: Smartcard interface reference application - VFQFPN24 pin block diagram*. Removed LED pin characteristics table. Added *Figure 6: Device configuration and ordering information*. Updated *Figure 8: ST7LCR option list*.
23-Jun-2008	2	Updated smartcard power supply in *Section : Features* to removed step-up converter.
19-Feb-2009	3	Updated smartcard supply voltage description in *Features*, *Section 1: Device overview*, and *Section 3.1: Functionality*. Removed recommended reflow oven profile in *Section 5: Package characteristics*.

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