PRELIMINARY DATA SHEET

General Description

The ICS844441I is a low jitter, high performance clock generator and a member of the FemtoClock™ family of silicon timing products. The ICS844441I is designed for use in applications using the SAS and SATA interconnect. The ICS844441I uses an external, 25MHz, parallel resonant crystal to generate four selectable output frequencies: 75MHz, 100MHz, 150MHz, and 300MHz. This silicon based approach provides excellent frequency stability and reliability. The ICS844441I features down and center spread spectrum (SSC) clocking techniques.

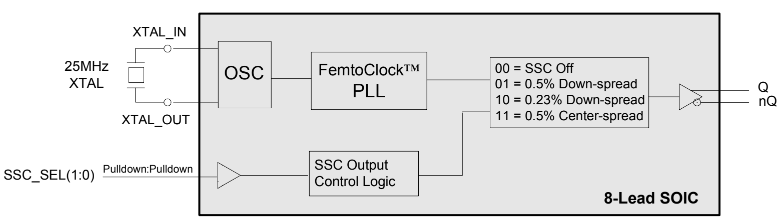
Applications

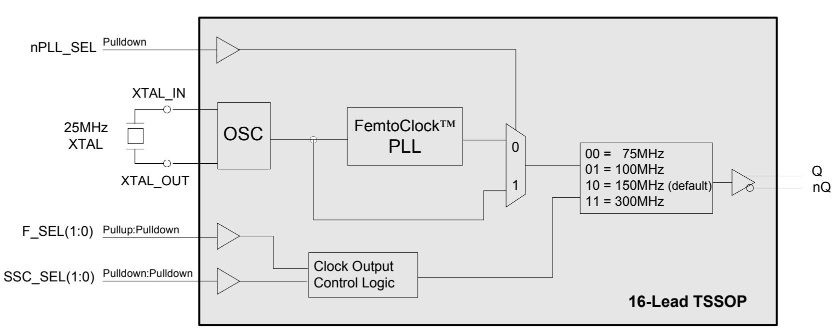
- SAS/SATA Host Bus Adapters
- SATA Port Multipliers
- SAS I/O Controllers
- TapeDrive and HDD Array Controllers
- SAS Edge and Fanout Expanders
- HDDs and TapeDrives
- Disk Storage Enterprise

Features

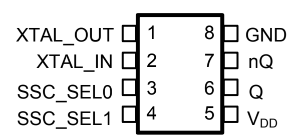
- Designed for use in SAS, SAS-2, and SATA systems
- Center (±0.25%) Spread Spectrum Clocking (SSC)
- Down (-0.23% or -0.5%) SSC
- Better frequency stability than SAW oscillators
- One differential 2.5V LVDS output
- Crystal oscillator interface designed for 25MHz (C_L = 18pF) frequency
- External fundamental crystal frequency ensures high reliability and low aging
- Selectable output frequencies: 75MHz, 100MHz, 150MHz, 300MHz
- Output frequency is tunable with external capacitors
- RMS phase jitter @ 100MHz, using a 25MHz crystal (12kHz – 20MHz): 1.1936ps (typical)
- 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

Block Diagrams

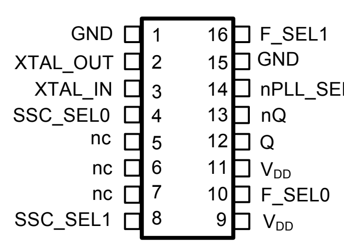




Pin Assignment



ICS844441I
8-Lead SOIC, 150 mil
3.90mm x 4.90mm x 1.375mm package body
M Package
Top View



ICS844441I
16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 1. Pin Descriptions

Name	Type		Description
XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
SSC_SEL0, SSC_SEL1	Input	Pulldown	SSC select pins. See Table 3A. LVCMOS/LVTTL interface levels.
F_SEL0	Input	Pulldown	Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.
F_SEL1	Input	Pullup	Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.
nPLL_SEL	Input	Pulldown	PLL Bypass pin. LVCMOS/LVTTL interface levels.
Q, nQ	Output		Differential clock outputs. LVDS interface levels.
GND	Power		Power supply ground.
V_{DD}	Power		Power supply pin.
nc	Unused		No connect.

NOTE: *Pullup/Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A. SSC_SEL[1:0] Function Table

Inputs		
SSC_SEL1	SSC_SEL0	Mode
0 (default)	0 (default)	SSC Off
0	1	0.5% Down-spread
1	0	0.23% Down-spread
1	1	0.5% Center-spread

Table 3B. F_SEL[1:0] Function Table

Inputs		Output Frequency (MHz)
F_SEL1	F_SEL0	
0	0	75
0	1	100
1 (default)	0 (default)	150
1	1	300

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA} 16 Lead TSSOP 8 Lead SOIC	 92.4°C/W (0 mps) 96.0°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			45		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	F_SEL1	$V_{DD} = V_{IN}$ = 2.5V			5	µA
		SSC_SEL[0:1], F_SEL0, nPLL_SEL	$V_{DD} = V_{IN}$ = 2.5V			150	µA
I_{IL}	Input Low Current	F_SEL1	V_{DD} = 2.5V, V_{IN} = 0V	-150			µA
		SSC_SEL[0:1], F_SEL0, nPLL_SEL	V_{DD} = 2.5V, V_{IN} = 0V	-5			µA

Table 4C. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4D. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ohm
Shunt Capacitance				7	pF

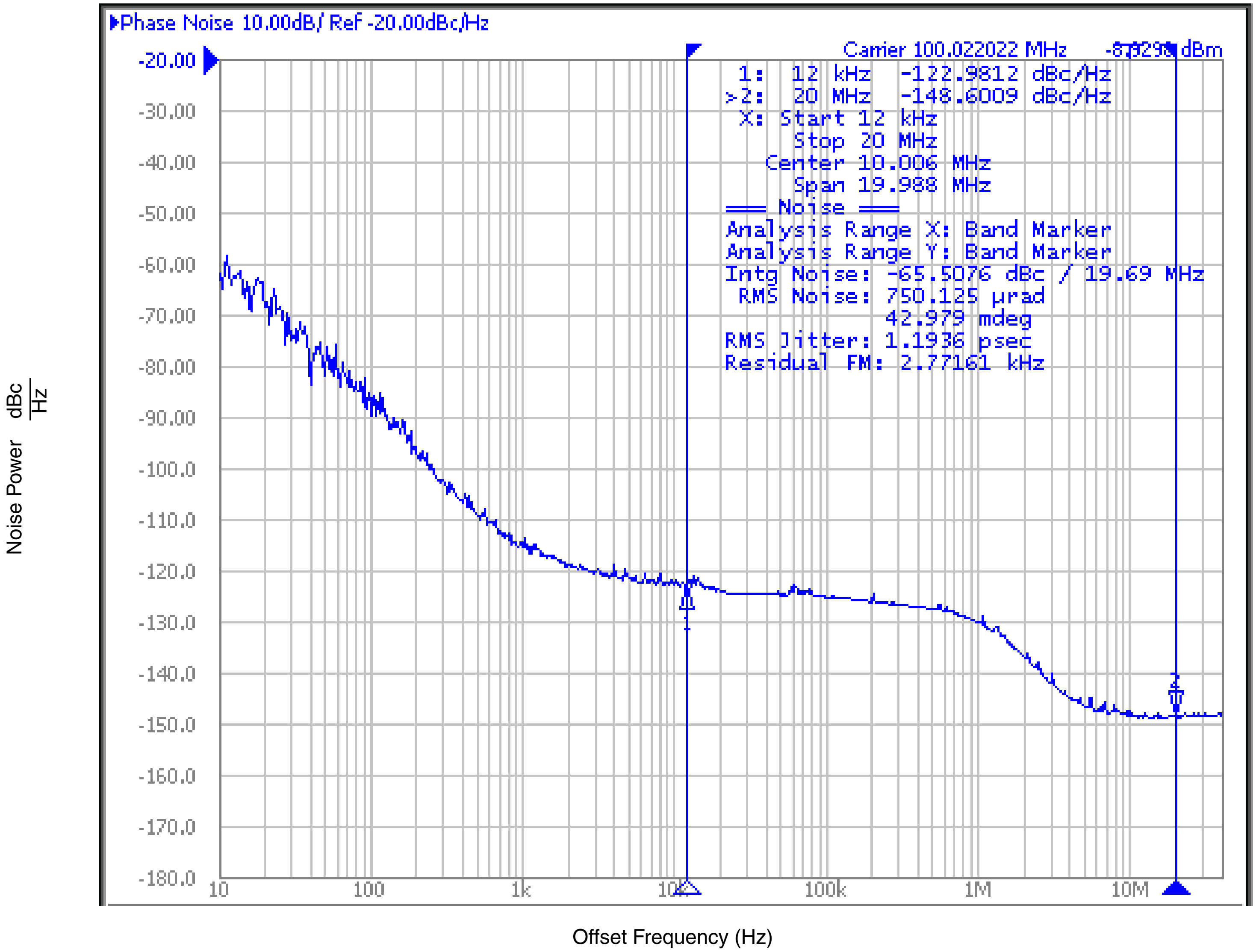
AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

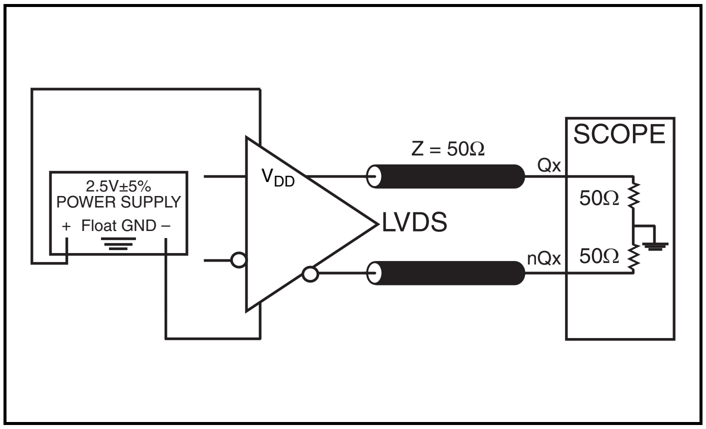
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL(1:0) = 00		75		MHz
		F_SEL(1:0) = 01		100		MHz
		F_SEL(1:0) = 10		150		MHz
		F_SEL(1:0) = 11		300		MHz
ƫjit(Ø)	RMS Phase Jitter (Random); NOTE 1	75MHz, Integration Range: 12kHz – 20MHz		1.19602		ps
		100MHz, Integration Range: 12kHz – 20MHz		1.1936		ps
		150MHz, Integration Range: 12kHz – 20MHz		1.22743		ps
		300MHz, Integration Range: 12kHz – 20MHz		1.15011		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Using a 25MHz, 18pF quartz crystal.
NOTE 1: Please refer to the Phase Noise plot.

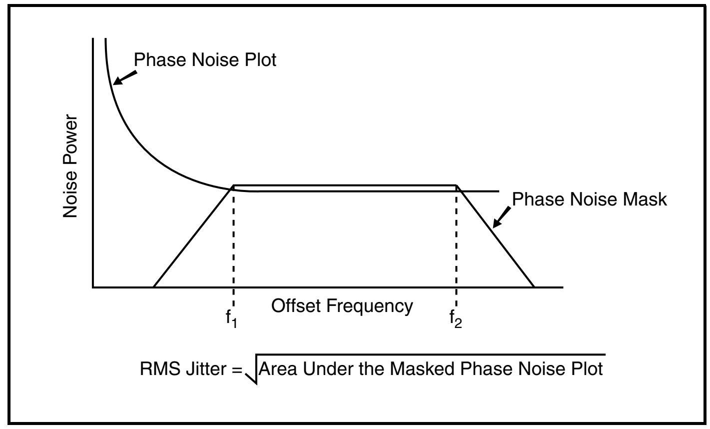
Typical Phase Noise at 100MHz



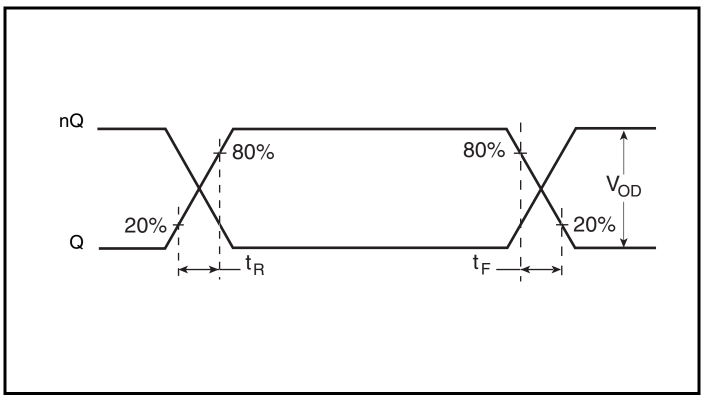
Parameter Measurement Information



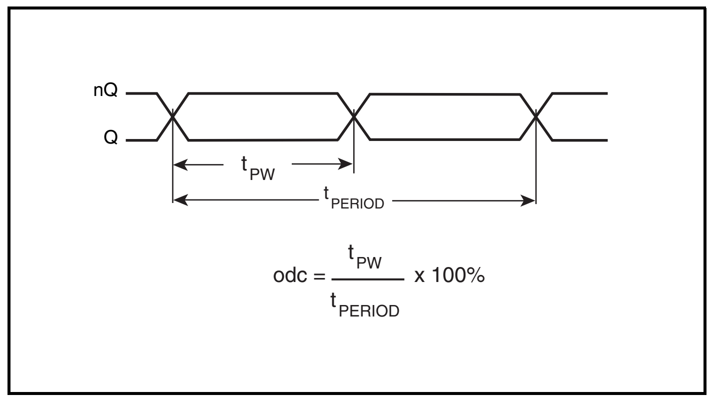
2.5V LVDS Output Load AC Test Circuit



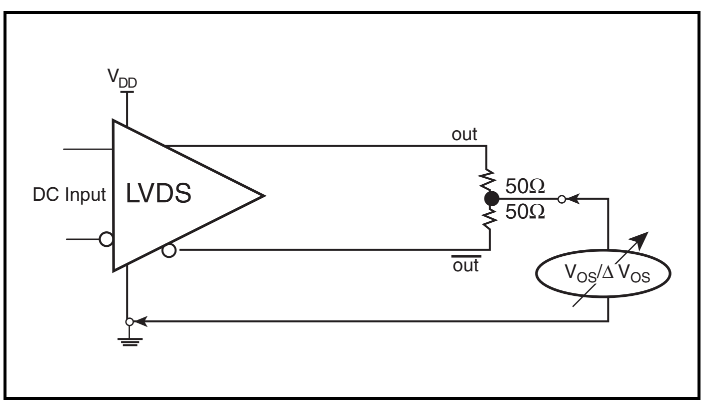
RMS Phase Jitter



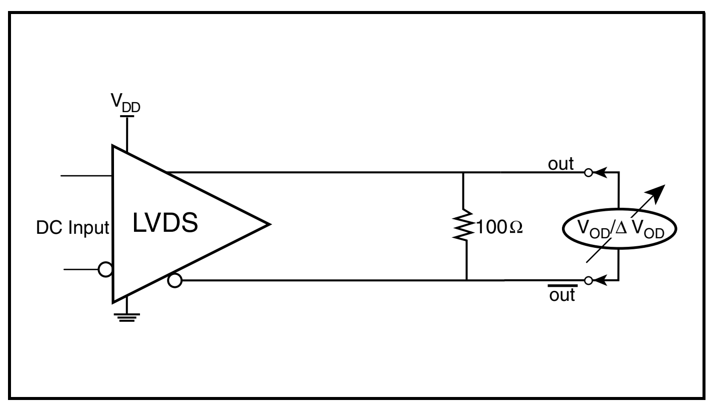
Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Crystal Input Interface

The ICS844441I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

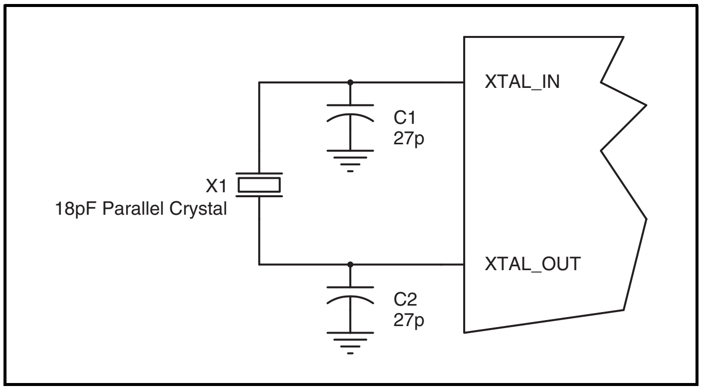


Figure 1. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

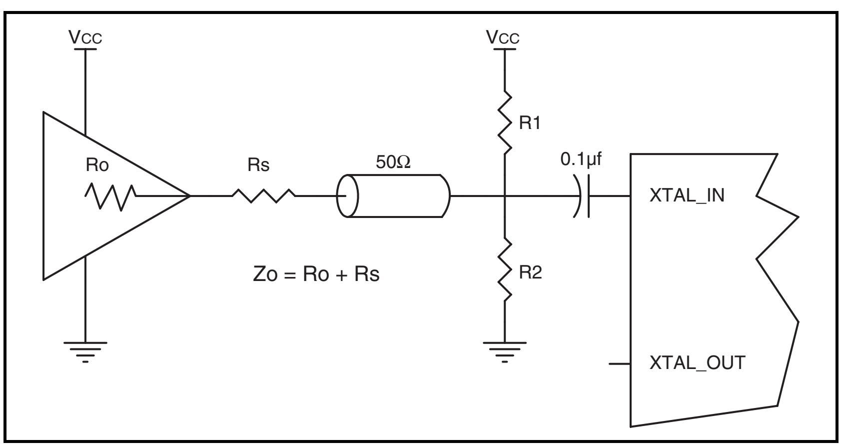


Figure 2. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

2.5V LVDS Driver Termination

Figure 3 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LVDS driver, it is recommended to terminate the unused outputs.

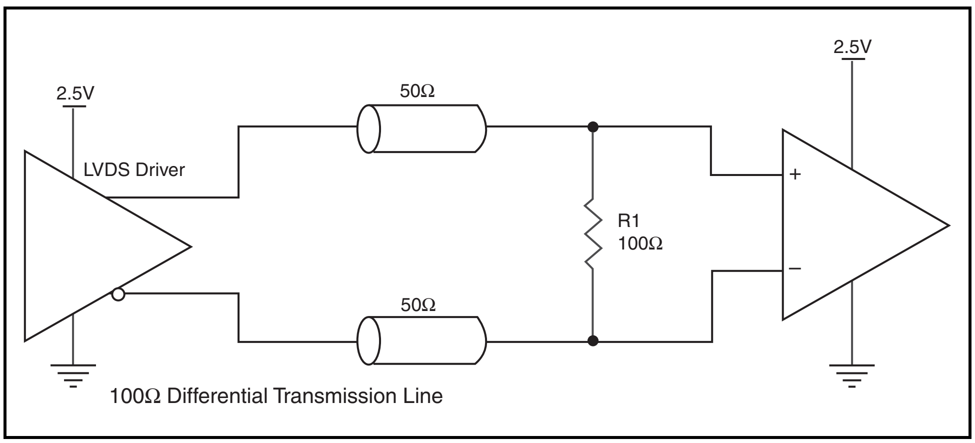


Figure 3. Typical LVDS Driver Termination

Schematic Example

Figure 4 shows an example of the ICS844441I application schematic. In this ecample, the device is operated at V_{DD} = 2.5V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. for different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS for receiver without built-in termination are shown in this schematic.

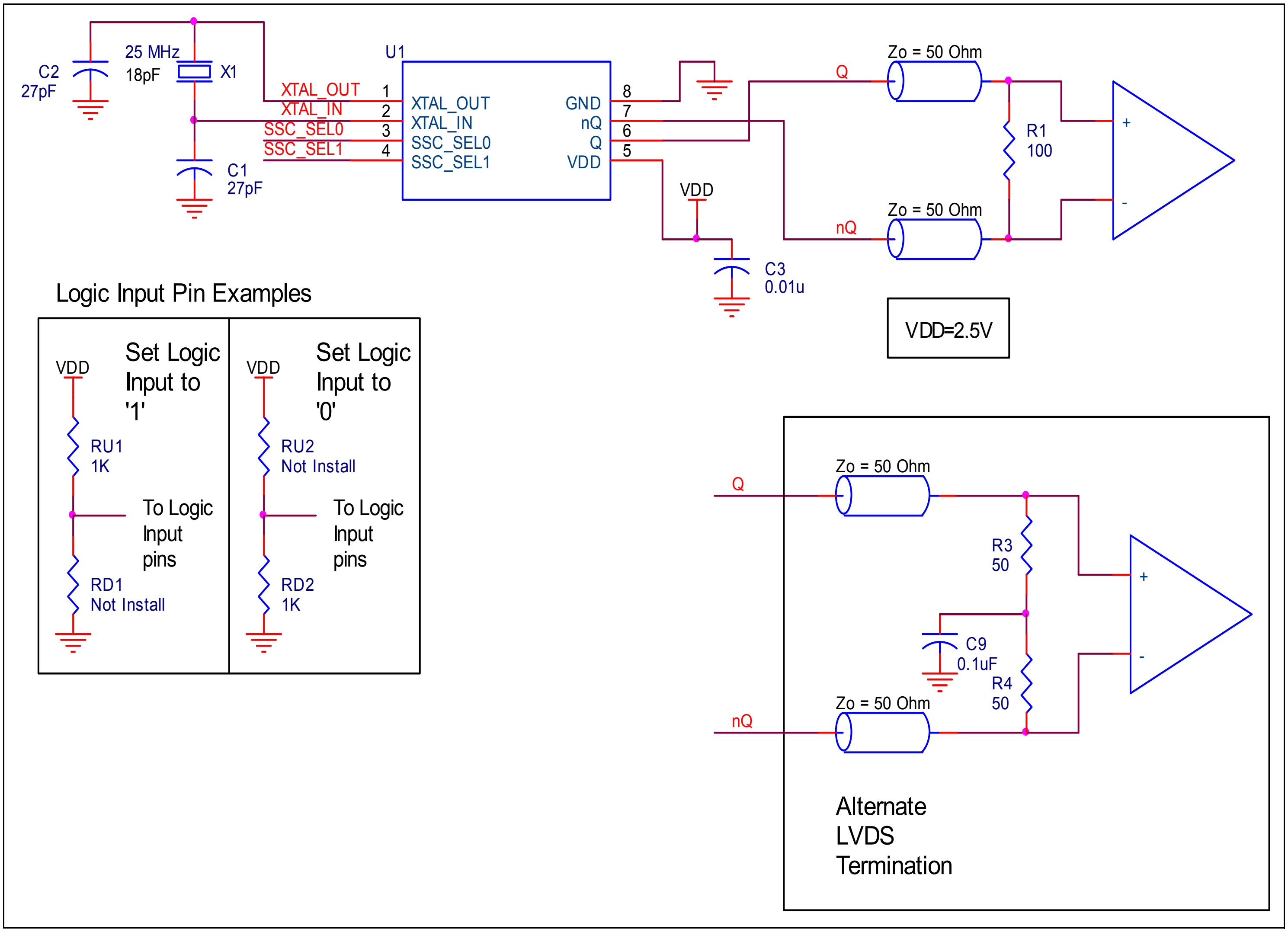


Figure 4. ICS844441I Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844441I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844441I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

Total Power $_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 45mA = **118.125mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 96°C/W per Table 6B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.118W * 96°C/W = 96.3°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the supply voltage, air flow and the type of board (multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

Table 6B. Thermal Resistance θ_{JA} for 8 Lead SOIC, Forced Convection

θ_{JA} vs. Air Flow			
Linear Feet per Second	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	96°C/W	87°C/W	82°C/W

Reliability Information

Table 7A. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

Table 7B. θ_{JA} vs. Air Flow Table for a 8 Lead SOIC

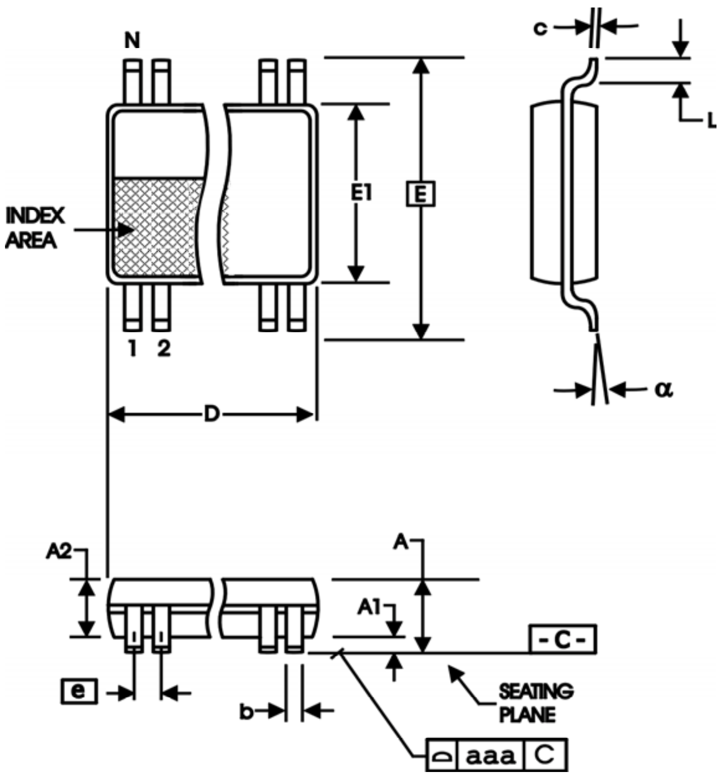
θ_{JA} vs. Air Flow			
Linear Feet per Second	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	96°C/W	87°C/W	82°C/W

Transistor Count

The transistor count for ICS844441I is: 6431

Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP



Package Outline - M Suffix for 8 Lead SOIC

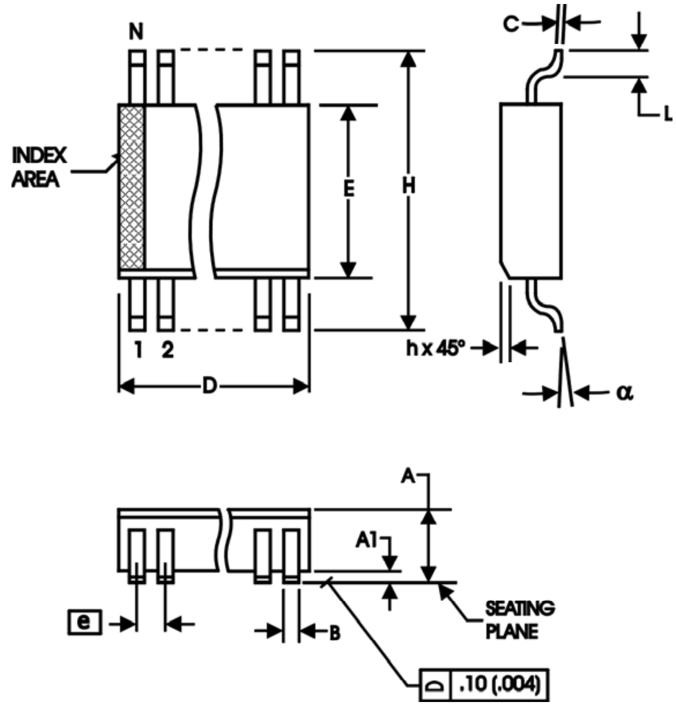


Table 8A. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 8B. Package Dimensions for 8 Lead SOIC

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844441DGILF	44441DIL	16 Lead “Lead-Free” TSSOP	Tube	-40°C to 85°C
844441DGILFT	44441DIL	16 Lead “Lead-Free” TSSOP	2500 Tape & Reel	-40°C to 85°C
844441DMI-75LF	TBD	8 Lead “Lead-Free” SOIC	Tube	-40°C to 85°C
844441DMI-75LFT	TBD	8 Lead “Lead-Free” SOIC	2500 Tape & Reel	-40°C to 85°C
844441DMI-100LF	TBD	8 Lead “Lead-Free” SOIC	Tube	-40°C to 85°C
844441DMI-100LFT	TBD	8 Lead “Lead-Free” SOIC	2500 Tape & Reel	-40°C to 85°C
844441DMI-150LF	41DI150L	8 Lead “Lead-Free” SOIC	Tube	-40°C to 85°C
844441DMI-150LFT	41DI150L	8 Lead “Lead-Free” SOIC	2500 Tape & Reel	-40°C to 85°C
844441DMI-300LF	41DI300L	8 Lead “Lead-Free” SOIC	Tube	-40°C to 85°C
844441DMI-300LFT	41DI300L	8 Lead “Lead-Free” SOIC	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Table 10. Additional Ordering Information

Part/Order Number	Package	Output Frequency (MHz)
844441DGI	16 TSSOP	75, 100, 150, 300
844441DMI-75	8 SOIC	75
844441DMI-100	8 SOIC	100
844441DMI-150	8 SOIC	150
844441DMI-300	8 SOIC	300

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