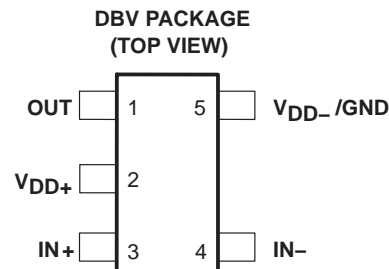


**TLV2721, TLV2721Y**  
**Advanced LinCMOS™ RAIL-TO-RAIL**  
**VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS**  
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- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Single-Supply 3-V and 5-V Operation**
- **Very Low Power . . . 110 μA Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Wide Supply Voltage Range 2.7 V to 10 V**
- **Macromodel Included**



## description

The TLV2721 is a single low-voltage operational amplifier available in the SOT-23 package. It offers a compromise between the ac performance and output drive of the TLV2731 and the micropower TLV2711.

It consumes only 150 μA (max) of supply current and is ideal for battery-powered applications. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV2721 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2721, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

With a total area of 5.6mm<sup>2</sup>, the SOT-23 package only requires one third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

## AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES	SYMBOL	CHIP FORM‡ (Y)
		SOT-23 (DBV)†		
0°C to 70°C	3 mV	TLV2721CDBV	VAKC	TLV2721Y
–40°C to 85°C	3 mV	TLV2721IDBV	VAKI	

† The DBV package available in tape and reel only.

‡ Chip forms are tested at T<sub>A</sub> = 25°C only.



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# TLV2721, TLV2721Y

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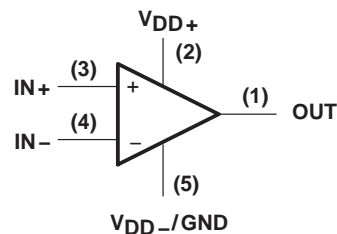
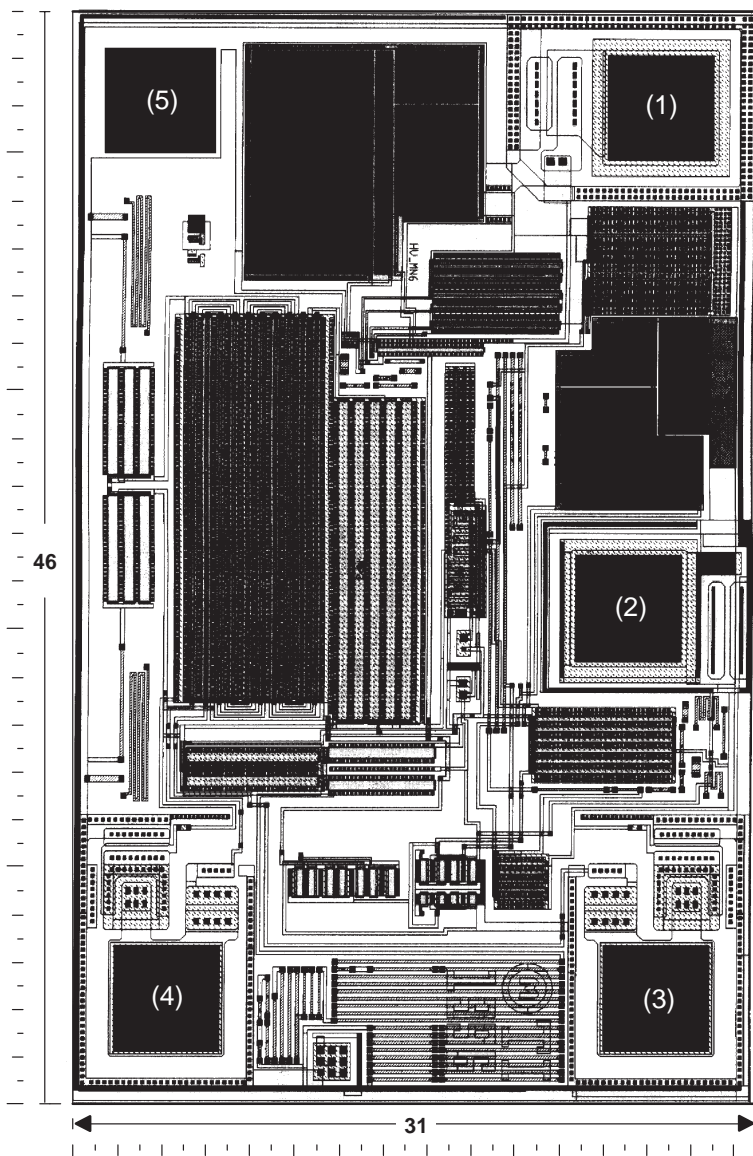
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#### TLV2721Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2721C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

#### BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS:  $4 \times 4$  MILS MINIMUM

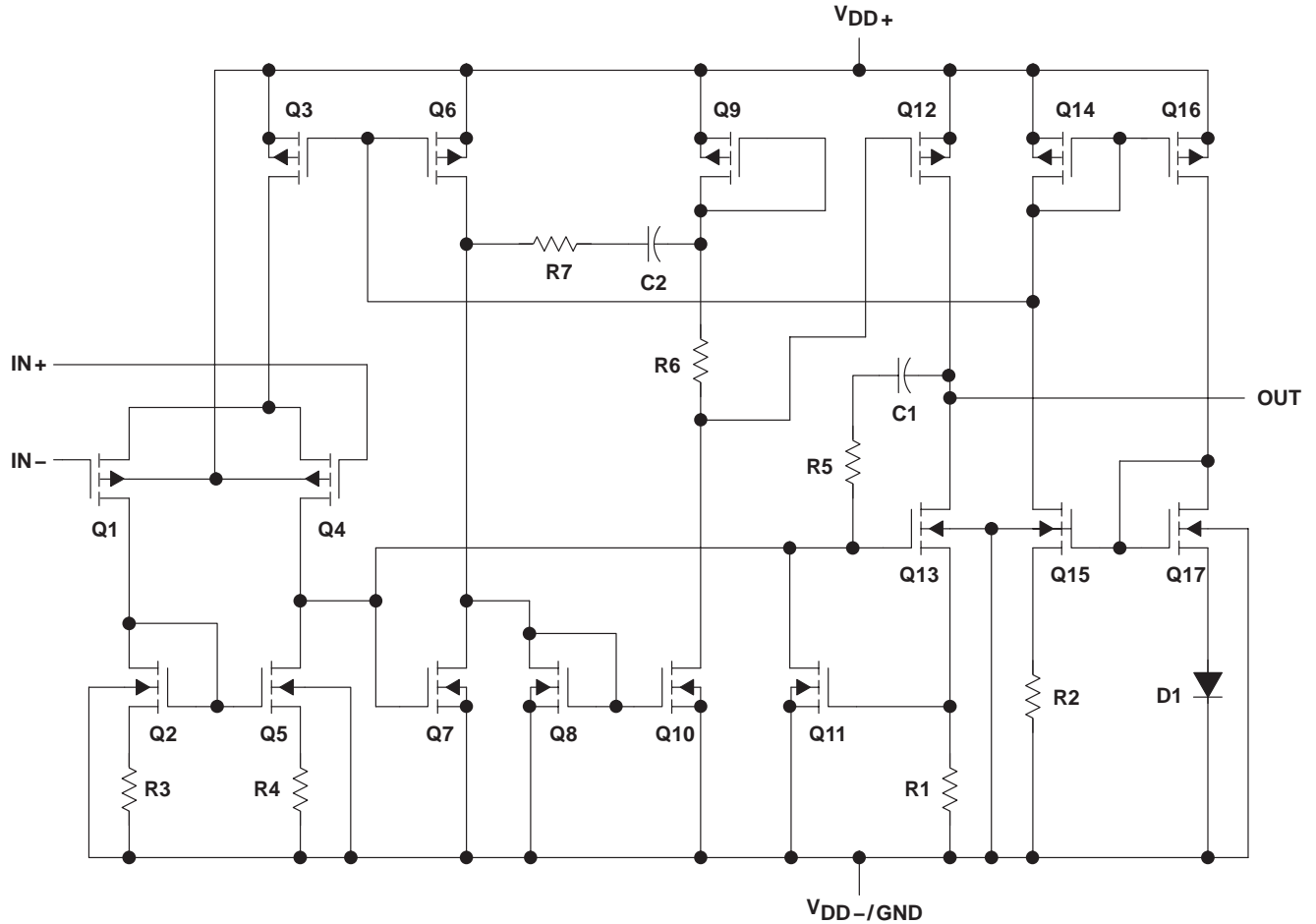
$T_{jmax} = 150^{\circ}\text{C}$

TOLERANCES ARE  $\pm 10\%$ .

ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



COMPONENT COUNT†	
Transistors	23
Diodes	5
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

# TLV2721, TLV2721Y

## Advanced LinCMOS™ RAIL-TO-RAIL

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{DD}$ (see Note 1)	12 V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm V_{DD}$
Input voltage range, $V_I$ (any input, see Note 1)	-0.3 V to $V_{DD}$
Input current, $I_I$ (each input)	$\pm 5$ mA
Output current, $I_O$	$\pm 50$ mA
Total current into $V_{DD+}$	$\pm 50$ mA
Total current out of $V_{DD-}$	$\pm 50$ mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : TLV2721C	0°C to 70°C
TLV2721I	-40°C to 85°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to  $V_{DD-}$ .
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below  $V_{DD-} - 0.3$  V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

#### recommended operating conditions

	TLV2721C		TLV2721I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD}$ (see Note 1)	2.7	10	2.7	10	V
Input voltage range, $V_I$	$V_{DD-}$	$V_{DD+} - 1.3$	$V_{DD-}$	$V_{DD+} - 1.3$	V
Common-mode input voltage, $V_{IC}$	$V_{DD-}$	$V_{DD+} - 1.3$	$V_{DD-}$	$V_{DD+} - 1.3$	V
Operating free-air temperature, $T_A$	0	70	-40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to  $V_{DD-}$ .



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**electrical characteristics at specified free-air temperature,  $V_{DD} = 3\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		T <sub>A</sub> †	TLV2721C			TLV2721I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>DD±</sub> = ±1.5 V, V <sub>IC</sub> = 0, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		Full range	0.5 3			0.5 3			mV
α <sub>VIO</sub>	Temperature coefficient of input offset voltage				1			1			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003			μV/mo
I <sub>IO</sub>	Input offset current			25°C	0.5 60			0.5 60			pA
				Full range	150			150			
I <sub>IB</sub>	Input bias current			25°C	1 60			1 60			pA
				Full range	150			150			
V <sub>ICR</sub>	Common-mode input voltage range	R <sub>S</sub> = 50 Ω,  V <sub>IO</sub>   ≤5 mV		25°C	0 to 2 −0.3 to 2.2		0 to 2 −0.3 to 2.2		V		
				Full range	0 to 1.7		0 to 1.7				
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = −100 μA		25°C	2.97		2.97		V		
		I <sub>OH</sub> = −400 μA		25°C	2.88		2.88				
				Full range	2.6		2.6				
V <sub>OL</sub>	Low-level output voltage	V <sub>IC</sub> = 1.5 V, I <sub>OL</sub> = 50 μA		25°C	15		15		mV		
		V <sub>IC</sub> = 1.5 V, I <sub>OL</sub> = 500 μA		25°C	150		150				
				Full range	500		500				
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>IC</sub> = 1.5 V, V <sub>O</sub> = 1 V to 2 V	R <sub>L</sub> = 2 kΩ‡	25°C	2 3		2 3		V/mV		
				Full range	1		1				
			R <sub>L</sub> = 1 MΩ‡	25°C	250		250				
r <sub>id</sub>	Differential input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
r <sub>ic</sub>	Common-mode input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>ic</sub>	Common-mode input capacitance	f = 10 kHz		25°C	6		6		pF		
z <sub>o</sub>	Closed-loop output impedance	f = 10 kHz, A <sub>V</sub> = 10		25°C	90		90		Ω		
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = 0 to 1.7 V, V <sub>O</sub> = 1.5 V, R <sub>S</sub> = 50 Ω		25°C	70 82		70 82		dB		
				Full range	65		65				
k <sub>SVR</sub>	Supply voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 2.7 V to 8 V, V <sub>IC</sub> = V <sub>DD</sub> /2, No load		25°C	80 95		80 95		dB		
				Full range	80		80				
I <sub>DD</sub>	Supply current	V <sub>O</sub> = 1.5 V, No load		25°C	100 150		100 150		μA		
				Full range	200		200				

$^\dagger$  Full range for the TLV2721C is 0°C to 70°C. Full range for the TLV2721I is -40°C to 85°C.

$^\ddagger$  Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature,  $V_{DD} = 3\text{ V}$

PARAMETER		TEST CONDITIONS	$T_A$ †	TLV2721C			TLV2721I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.1\text{ V to }1.9\text{ V}, R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	0.1	0.25		0.1	0.25		V/ $\mu\text{s}$
			Full range	0.05			0.05			
$V_n$	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		120			120		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	25°C		20			20		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		680			680		mV
		$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		860			860		
$I_n$	Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion plus noise	$V_O = 1\text{ V to }2\text{ V}, f = 20\text{ kHz}, R_L = 2\text{ k}\Omega^\ddagger$	25°C		$A_V = 1$	2.52%		$A_V = 1$	2.52%	
					$A_V = 10$	7.01%		$A_V = 10$	7.01%	
		$V_O = 1\text{ V to }2\text{ V}, f = 20\text{ kHz}, R_L = 2\text{ k}\Omega^\S$	25°C		$A_V = 1$	0.076%		$A_V = 1$	0.076%	
					$A_V = 10$	0.147%		$A_V = 10$	0.147%	
	Gain-bandwidth product	$f = 1\text{ kHz}, R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C		480			480		kHz
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}, R_L = 2\text{ k}\Omega^\ddagger, A_V = 1, C_L = 100\text{ pF}^\ddagger$	25°C		30			30		kHz
$t_s$	Settling time	$A_V = -1, \text{Step} = 1\text{ V to }2\text{ V}, R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C		To 0.1%	4.5		To 0.1%	4.5	$\mu\text{s}$
			25°C		To 0.01%	6.8		To 0.01%	6.8	$\mu\text{s}$
$\phi_m$	Phase margin at unity gain	$R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C		53°			53°		
	Gain margin		25°C		12			12		dB

† Full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

‡ Referenced to 1.5 V

§ Referenced to 0 V

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**electrical characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		T <sub>A</sub> <sup>†</sup>	TLV2721C			TLV2721I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>DD±</sub> = ±2.5 V, V <sub>IC</sub> = 0, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		Full range	0.5 3			0.5 3			mV
α <sub>VIO</sub>	Temperature coefficient of input offset voltage				1			1			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003			μV/mo
I <sub>IO</sub>	Input offset current			25°C	0.5 60			0.5 60			pA
				Full range	150			150			
I <sub>IB</sub>	Input bias current			25°C	1 60			1 60			pA
				Full range	150			150			
V <sub>ICR</sub>	Common-mode input voltage range	R <sub>S</sub> = 50 Ω,  V <sub>IO</sub>   ≤ 5 mV		25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2	V	
				Full range	0 to 3.5			0 to 3.5			
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –500 μA I <sub>OH</sub> = –1 mA		25°C	4.75	4.88		4.75	4.88	V	
					4.6	4.76		4.6	4.76		
V <sub>OL</sub>	Low-level output voltage	V <sub>IC</sub> = 2.5 V, I <sub>OL</sub> = 50 μA		25°C	12			12			mV
		V <sub>IC</sub> = 2.5 V, I <sub>OL</sub> = 500 μA		25°C	120			120			
				Full range	500			500			
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>IC</sub> = 2.5 V, V <sub>O</sub> = 1 V to 4 V	R <sub>L</sub> = 2 kΩ‡	25°C	3	5		3	5	V/mV	
				Full range	1			1			
			R <sub>L</sub> = 1 MΩ‡	25°C	800			800			
r <sub>id</sub>	Differential input resistance			25°C	10 <sup>12</sup>			10 <sup>12</sup>			Ω
r <sub>ic</sub>	Common-mode input resistance			25°C	10 <sup>12</sup>			10 <sup>12</sup>			Ω
c <sub>ic</sub>	Common-mode input capacitance	f = 10 kHz		25°C	6			6			pF
z <sub>o</sub>	Closed-loop output impedance	f = 10 kHz, A <sub>V</sub> = 10		25°C	70			70			Ω
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = 0 to 2.7 V, V <sub>O</sub> = 1.5 V, R <sub>S</sub> = 50 Ω		25°C	70	85		70	85	dB	
				Full range	65			65			
k <sub>SVR</sub>	Supply voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 4.4 V to 8 V, V <sub>IC</sub> = V <sub>DD</sub> /2, No load		25°C	80	95		80	95	dB	
				Full range	80			80			
I <sub>DD</sub>	Supply current	V <sub>O</sub> = 2.5 V, No load		25°C	110	150		110	150	μA	
				Full range	200			200			

$^\dagger$  Full range for the TLV2721C is 0°C to 70°C. Full range for the TLV2721I is –40°C to 85°C.

$^\ddagger$  Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T <sub>A</sub> †	TLV2721C			TLV2721I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V <sub>O</sub> = 1.5 V to 3.5 V, R <sub>L</sub> = 2 kΩ‡, C <sub>L</sub> = 100 pF‡		25°C	0.1	0.25		0.1	0.25		V/μs
				Full range	0.05			0.05			
V <sub>n</sub>	Equivalent input noise voltage	f = 10 Hz f = 1 kHz		25°C	90			90			nV/√Hz
				25°C	19			19			
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz f = 0.1 Hz to 10 Hz		25°C	800			800			mV
				25°C	960			960			
I <sub>n</sub>	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD+N	Total harmonic distortion plus noise	V <sub>O</sub> = 1.5 V to 3.5 V, f = 20 kHz, R <sub>L</sub> = 2 kΩ‡	A <sub>V</sub> = 1	25°C	2.45%			2.45%			
			A <sub>V</sub> = 10		5.54%			5.54%			
		V <sub>O</sub> = 1.5 V to 3.5 V, f = 20 kHz, R <sub>L</sub> = 2 kΩ§	A <sub>V</sub> = 1	25°C	0.142%			0.142%			
			A <sub>V</sub> = 10		0.257%			0.257%			
	Gain-bandwidth product	f = 1 kHz, R <sub>L</sub> = 2 kΩ‡, C <sub>L</sub> = 100 pF‡		25°C	510			510			kHz
B <sub>OM</sub>	Maximum output-swing bandwidth	V <sub>O(PP)</sub> = 1 V, R <sub>L</sub> = 2 kΩ‡, A <sub>V</sub> = 1, C <sub>L</sub> = 100 pF‡		25°C	40			40			kHz
t <sub>s</sub>	Settling time	A <sub>V</sub> = –1, Step = 1.5 V to 3.5 V, R <sub>L</sub> = 2 kΩ‡, C <sub>L</sub> = 100 pF‡	To 0.1%	25°C	6.8			6.8			μs
			To 0.01%	25°C	9.2			9.2			
φ <sub>m</sub>	Phase margin at unity gain	R <sub>L</sub> = 2 kΩ‡, C <sub>L</sub> = 100 pF‡		25°C	53°			53°			
	Gain margin			25°C	12			12			dB

† Full range is  $-40^\circ\text{C to }85^\circ\text{C}$ .

‡ Referenced to  $2.5\text{ V}$

§ Referenced to  $0\text{ V}$



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**electrical characteristics at  $V_{DD} = 3\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TLV2721Y			UNIT
		MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{DD} \pm \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		620		$\mu\text{V}$
$I_{IO}$ Input offset current			0.5	60	$\text{pA}$
$I_{IB}$ Input bias current			1	60	$\text{pA}$
$V_{ICR}$ Common-mode input voltage range	$ V_{IO}  \leq 5\text{ mV}$ , $R_S = 50\ \Omega$		–0.3 to 2.2		$\text{V}$
$V_{OH}$ High-level output voltage	$I_{OH} = -100\ \mu\text{A}$		2.97		$\text{V}$
$V_{OL}$ Low-level output voltage	$V_{IC} = 1.5\text{ V}$ , $I_{OL} = 50\ \mu\text{A}$		15		$\text{mV}$
	$V_{IC} = 1.5\text{ V}$ , $I_{OL} = 500\ \mu\text{A}$		150		
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1\text{ V to } 2\text{ V}$	$R_L = 2\text{ k}\Omega^\dagger$	3		$\text{V/mV}$
		$R_L = 1\text{ M}\Omega^\dagger$	250		
$r_{id}$ Differential input resistance			$10^{12}$		$\Omega$
$r_{ic}$ Common-mode input resistance			$10^{12}$		$\Omega$
$c_{ic}$ Common-mode input capacitance	$f = 10\text{ kHz}$		6		$\text{pF}$
$z_o$ Closed-loop output impedance	$f = 10\text{ kHz}$ , $A_V = 10$		90		$\Omega$
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 1.7\text{ V}$ , $V_O = 0$ , $R_S = 50\ \Omega$		82		$\text{dB}$
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V to } 8\text{ V}$ , $V_{IC} = 0$ , No load		95		$\text{dB}$
$I_{DD}$ Supply current	$V_O = 0$ , No load		100		$\mu\text{A}$

$^\dagger$  Referenced to 1.5 V

**electrical characteristics at  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TLV2721Y			UNIT
		MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{DD} \pm \pm 1.5\text{ V}$ , $V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$		610		$\mu\text{V}$
$I_{IO}$ Input offset current			0.5	60	$\text{pA}$
$I_{IB}$ Input bias current			1	60	$\text{pA}$
$V_{ICR}$ Common-mode input voltage range	$ V_{IO}  \leq 5\text{ mV}$ , $R_S = 50\ \Omega$		–0.3 to 4.2		$\text{V}$
$V_{OH}$ High-level output voltage	$I_{OH} = -500\ \mu\text{A}$		4.88		$\text{V}$
$V_{OL}$ Low-level output voltage	$V_{IC} = 2.5\text{ V}$ , $I_{OL} = 50\ \mu\text{A}$		12		$\text{mV}$
	$V_{IC} = 2.5\text{ V}$ , $I_{OL} = 500\ \mu\text{A}$		120		
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1\text{ V to } 4\text{ V}$	$R_L = 2\text{ k}\Omega^\dagger$	5		$\text{V/mV}$
		$R_L = 1\text{ M}\Omega^\dagger$	800		
$r_{id}$ Differential input resistance			$10^{12}$		$\Omega$
$r_{ic}$ Common-mode input resistance			$10^{12}$		$\Omega$
$c_{ic}$ Common-mode input capacitance	$f = 10\text{ kHz}$		6		$\text{pF}$
$z_o$ Closed-loop output impedance	$f = 10\text{ kHz}$ , $A_V = 10$		70		$\Omega$
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 1.7\text{ V}$ , $V_O = 0$ , $R_S = 50\ \Omega$		85		$\text{dB}$
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V to } 8\text{ V}$ , $V_{IC} = 0$ , No load		95		$\text{dB}$
$I_{DD}$ Supply current	$V_O = 0$ , No load		110		$\mu\text{A}$

$^\dagger$  Referenced to 2.5 V

## TYPICAL CHARACTERISTICS

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## TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2721  
INPUT OFFSET VOLTAGE**

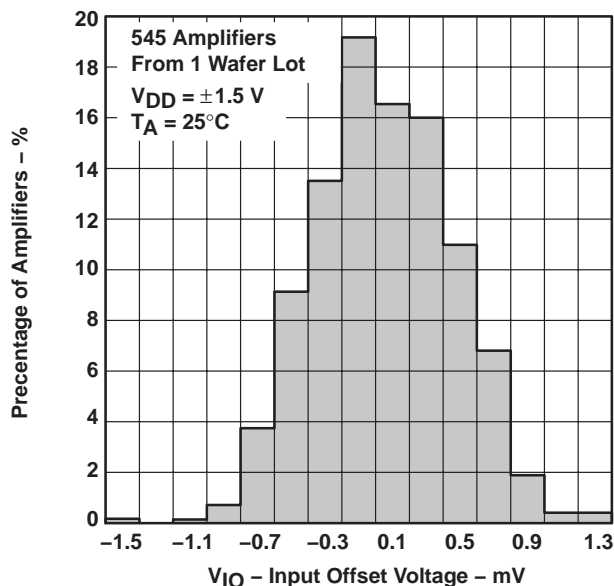


Figure 1

**DISTRIBUTION OF TLV2721  
INPUT OFFSET VOLTAGE**

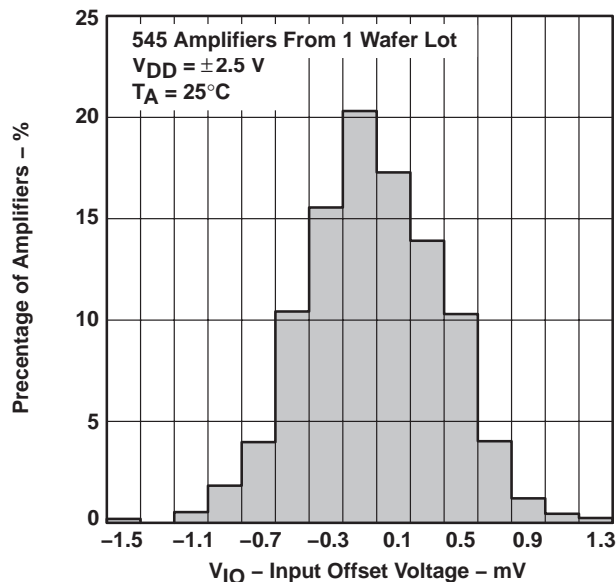


Figure 2

**INPUT OFFSET VOLTAGE†  
vs  
COMMON-MODE INPUT VOLTAGE**

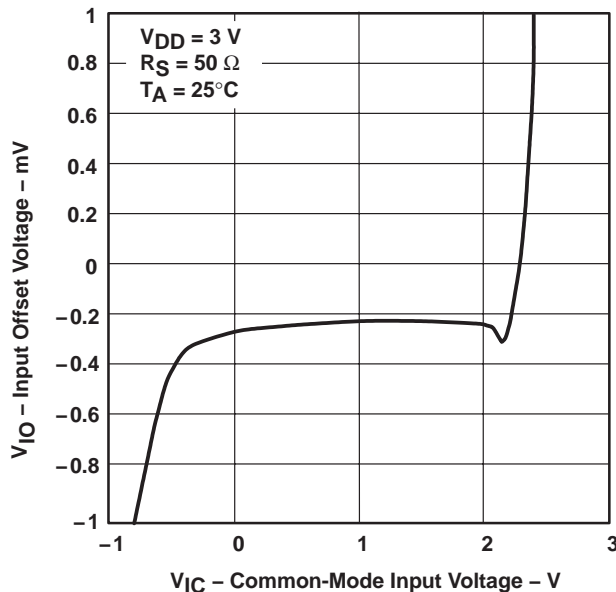


Figure 3

**INPUT OFFSET VOLTAGE†  
vs  
COMMON-MODE INPUT VOLTAGE**

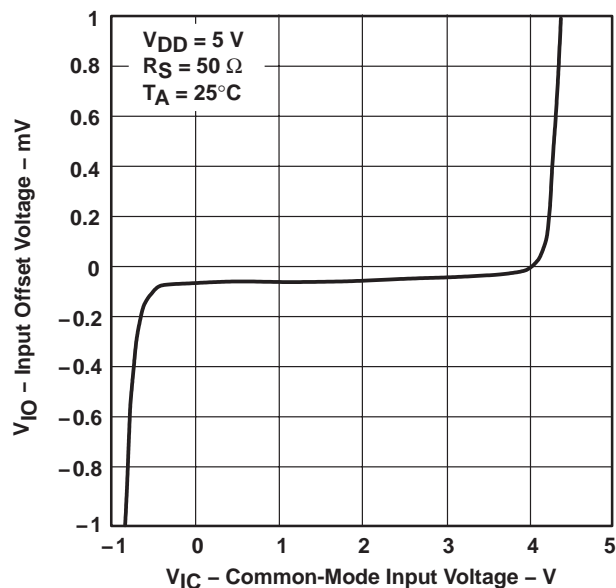


Figure 4

† For all curves where  $V_{DD} = 5 \text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3 \text{ V}$ , all loads are referenced to 1.5 V.

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#### TYPICAL CHARACTERISTICS

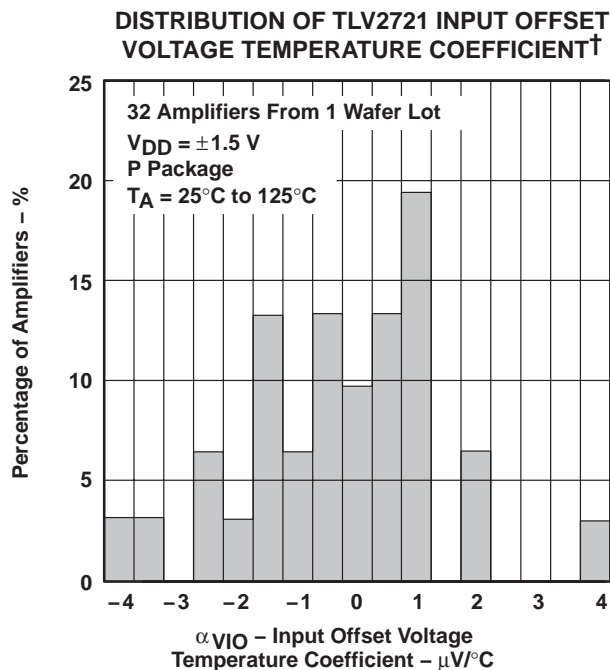


Figure 5

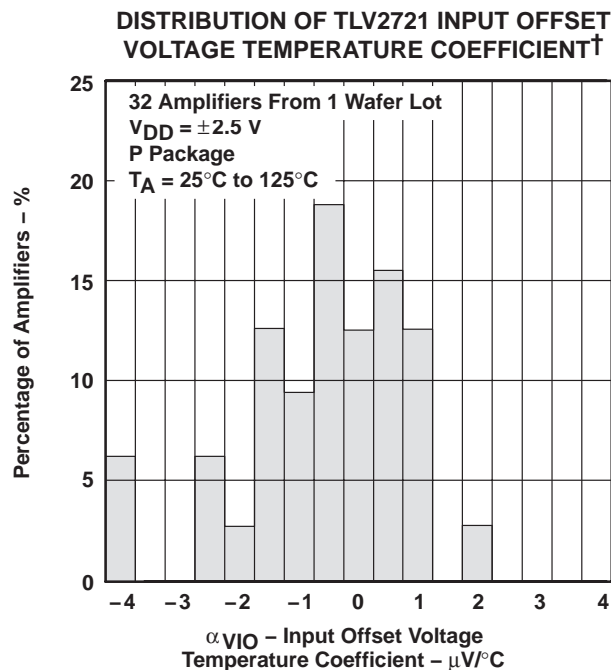


Figure 6

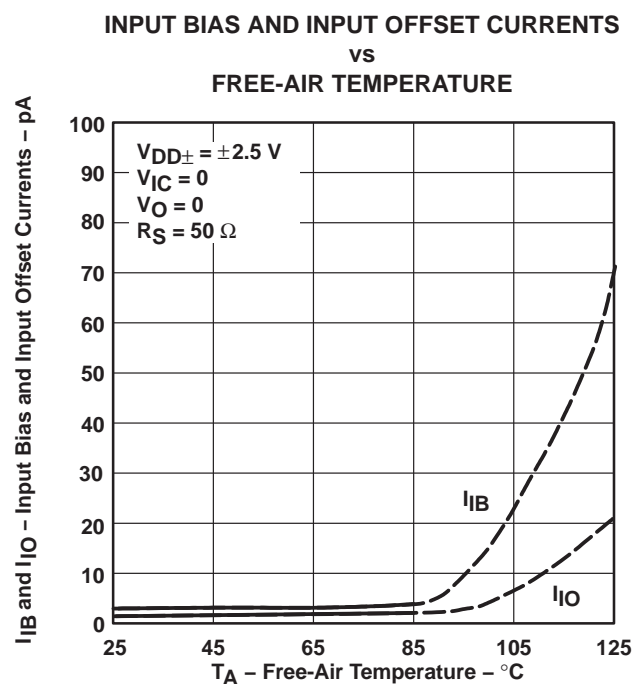


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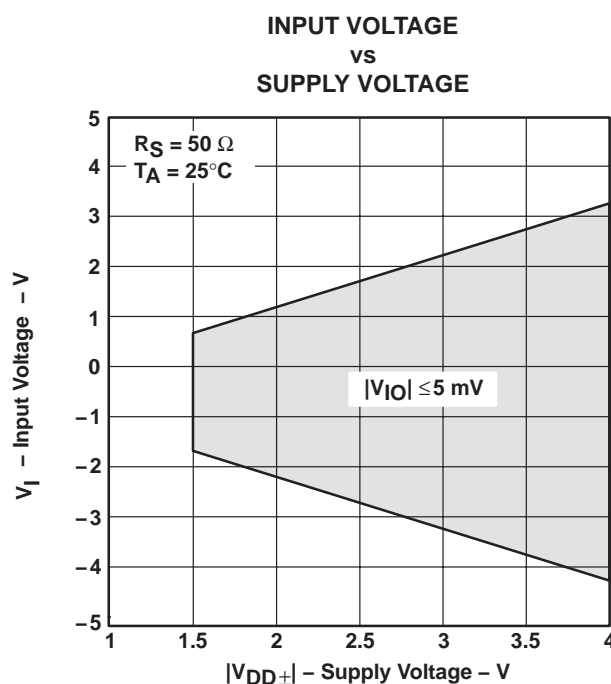


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS

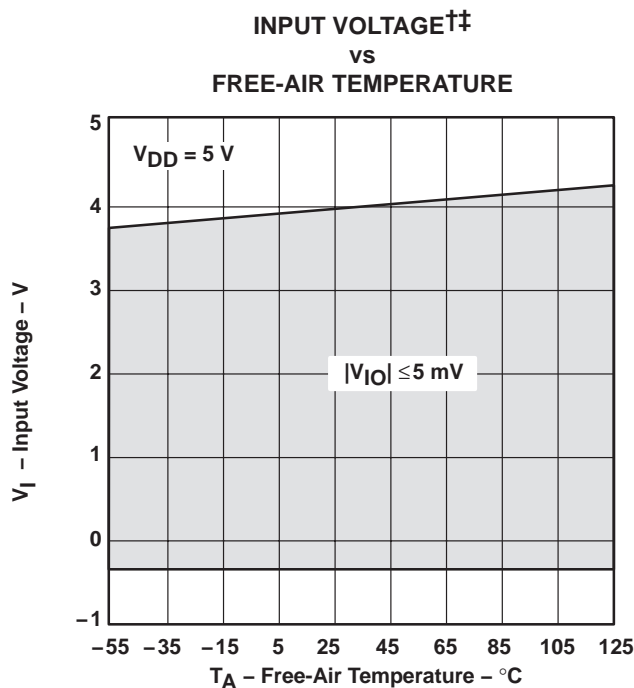


Figure 9

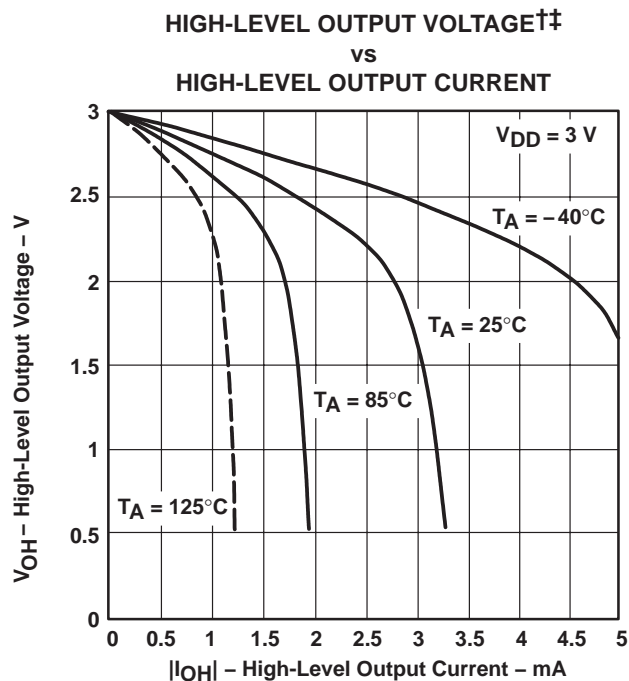


Figure 10

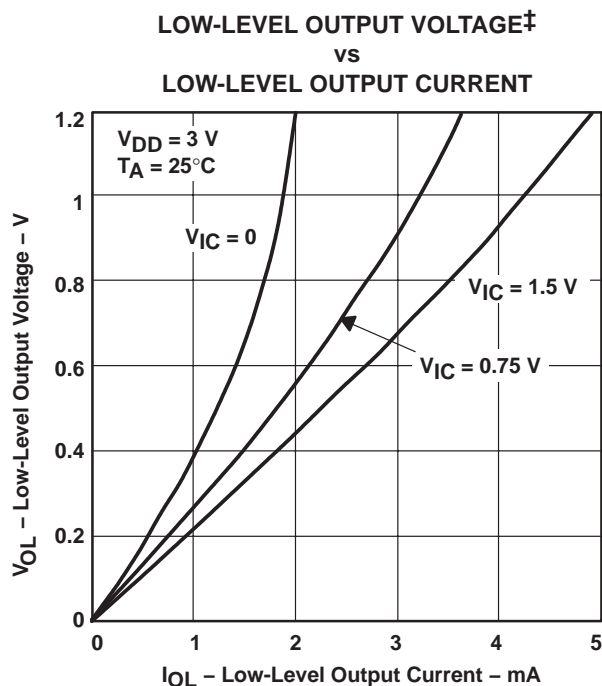


Figure 11

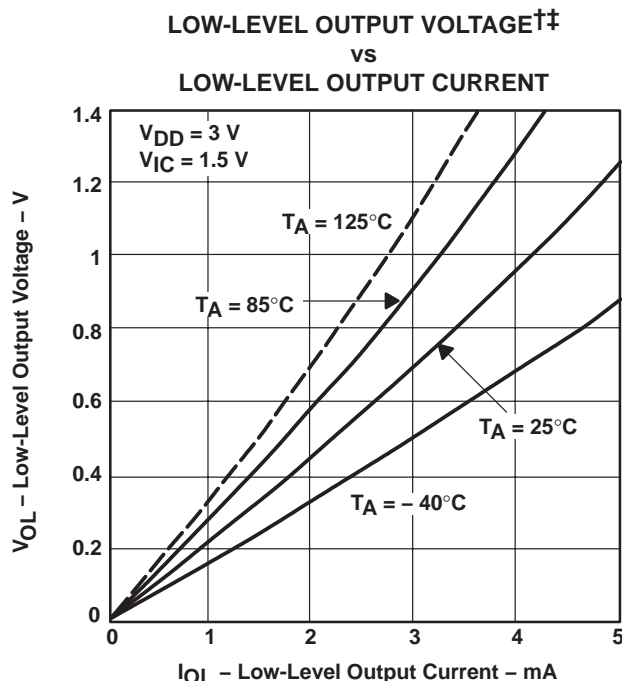


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

†† For all curves where  $V_{DD} = 5 \text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3 \text{ V}$ , all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

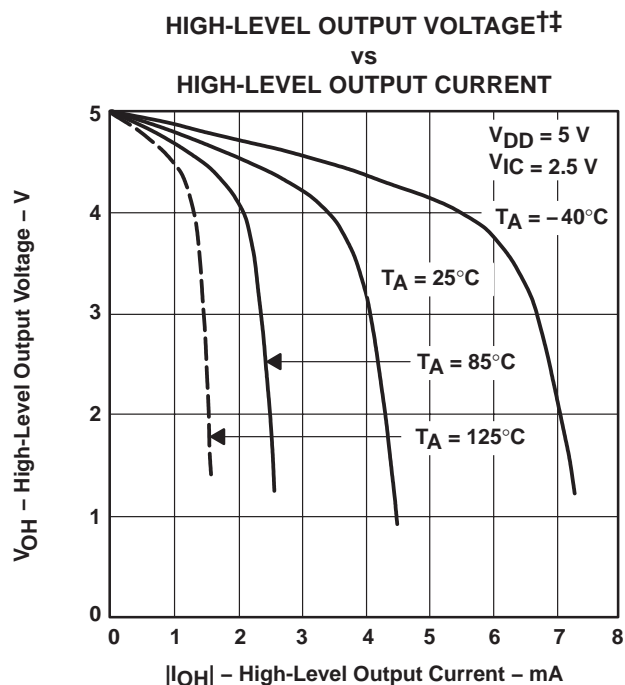


Figure 13

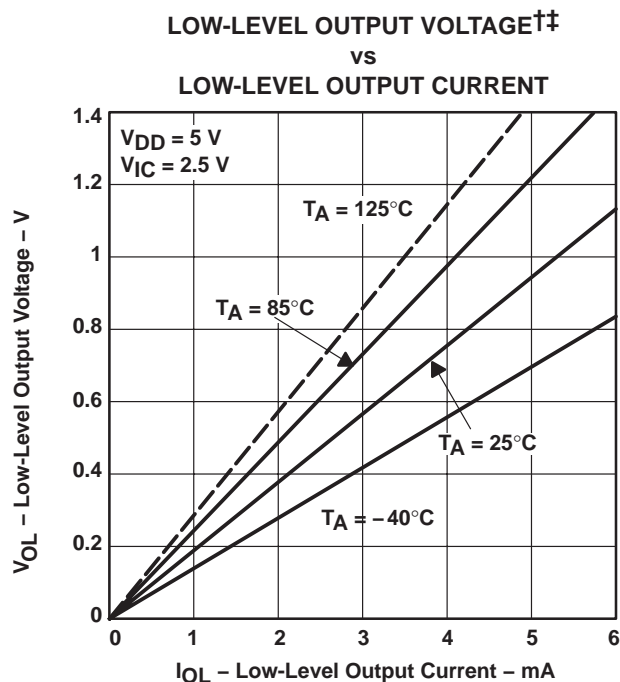


Figure 14

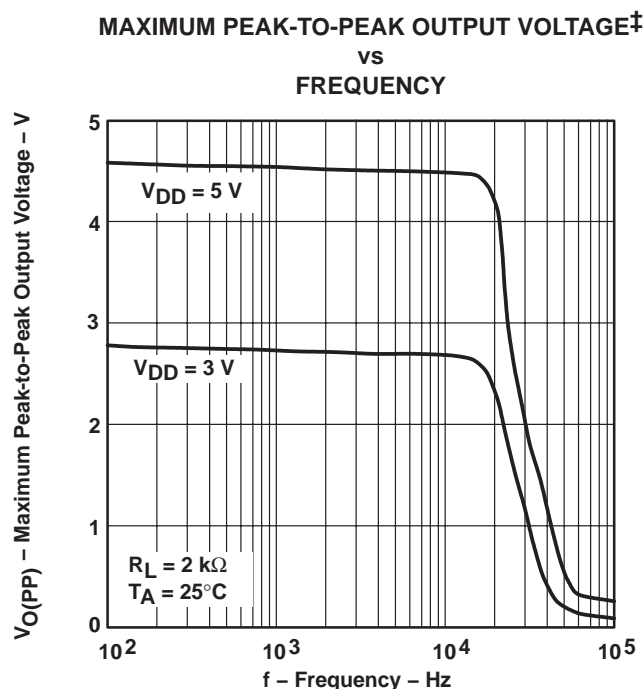


Figure 15

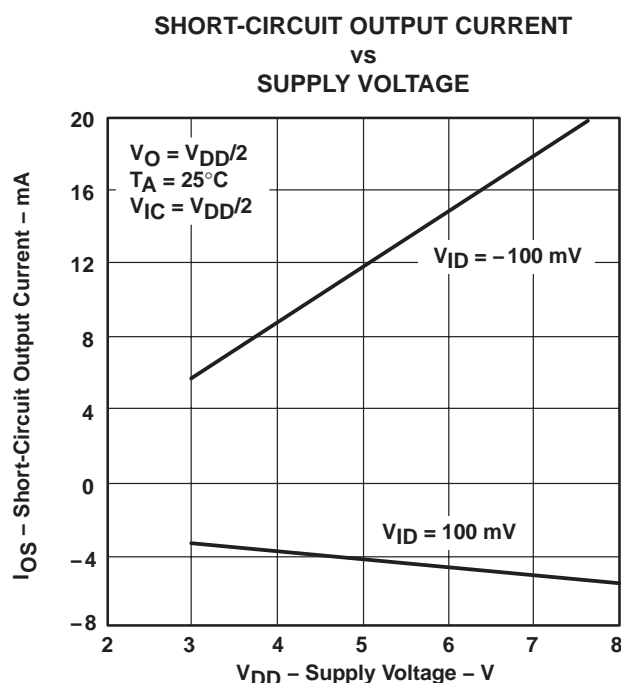
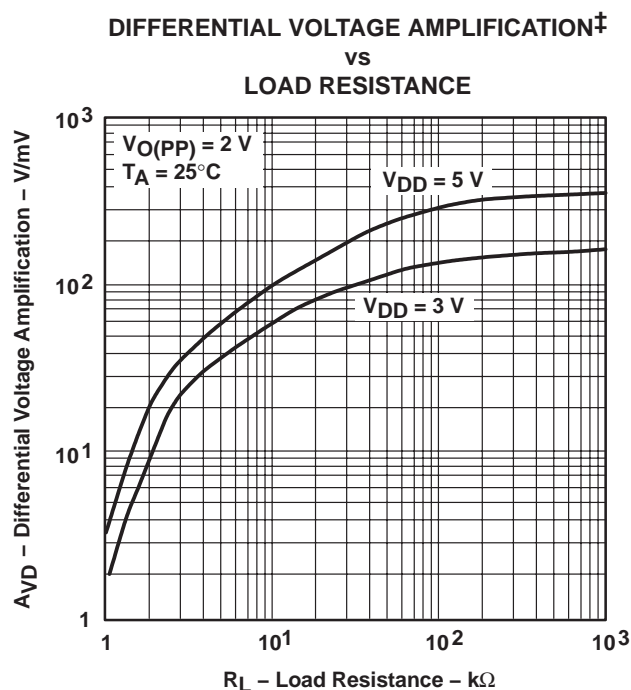
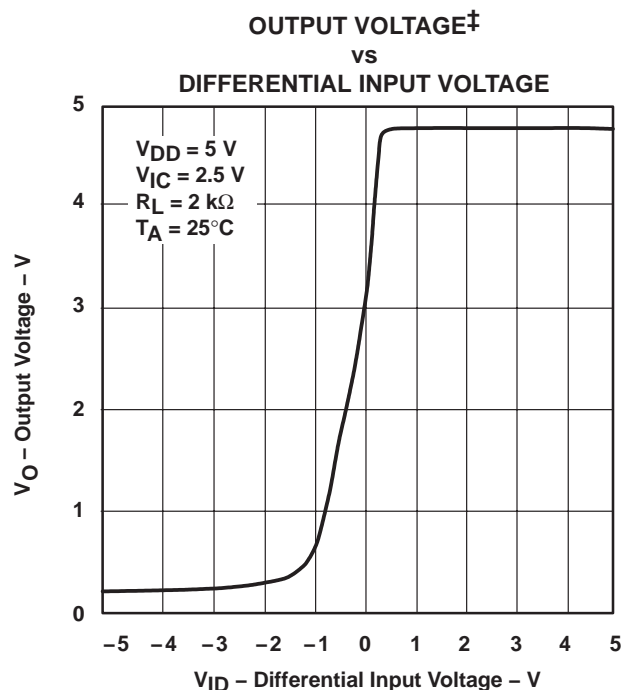
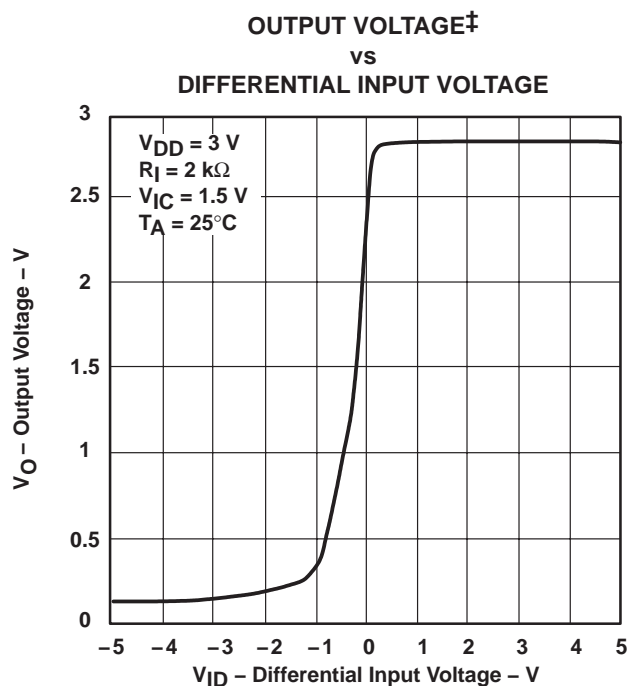
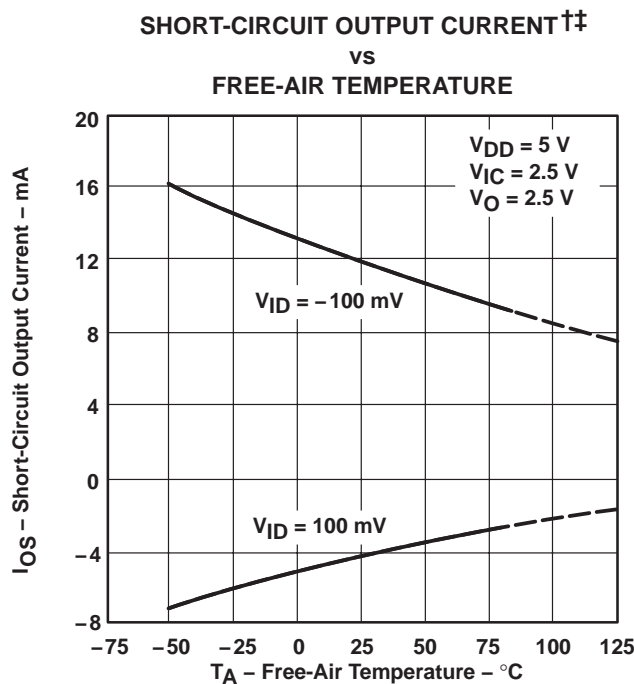


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.  
 ‡ For all curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3\text{ V}$ , all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where  $V_{DD} = 5$  V, all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3$  V, all loads are referenced to 1.5 V.

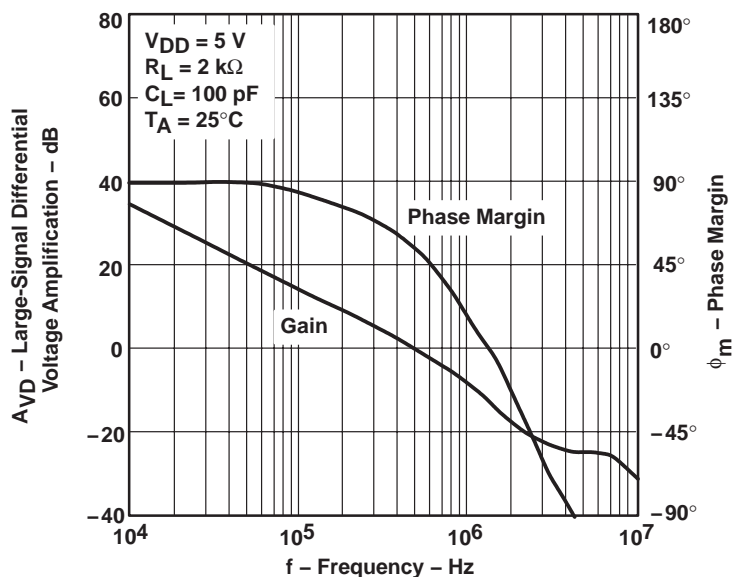
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**TYPICAL CHARACTERISTICS**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE†  
AMPLIFICATION AND PHASE MARGIN**

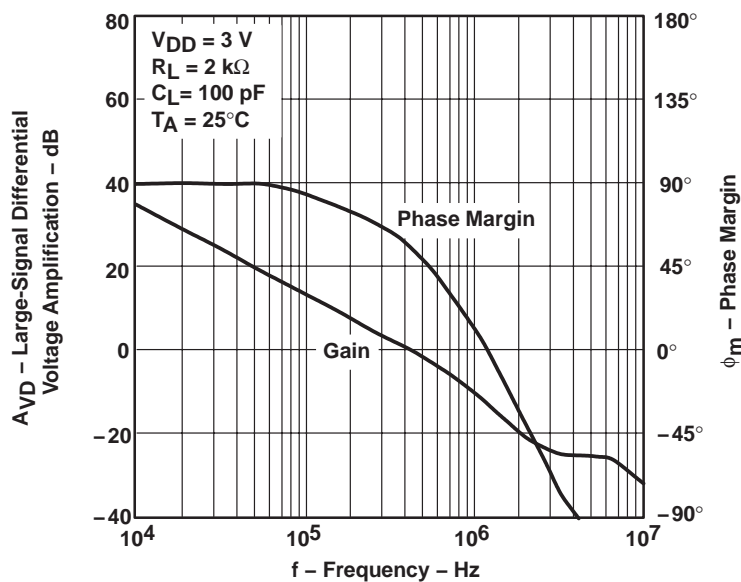
**VS  
FREQUENCY**



**Figure 21**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
AMPLIFICATION AND PHASE MARGIN†**

**VS  
FREQUENCY**



**Figure 22**

† For all curves where  $V_{DD} = 5$  V, all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3$  V, all loads are referenced to 1.5 V.



## TYPICAL CHARACTERISTICS

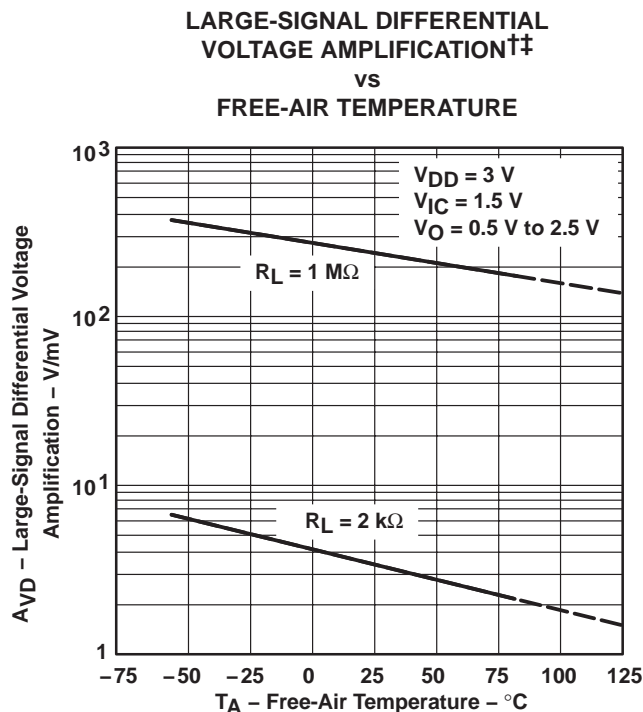


Figure 23

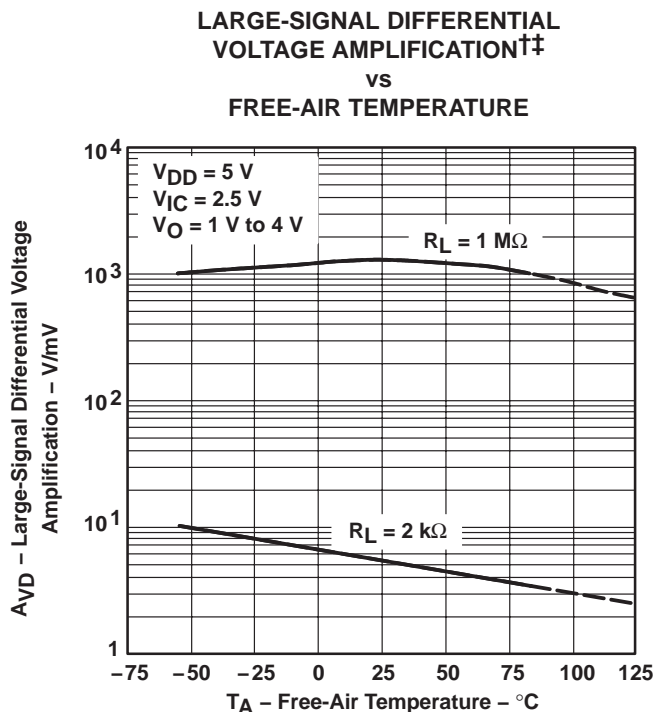


Figure 24

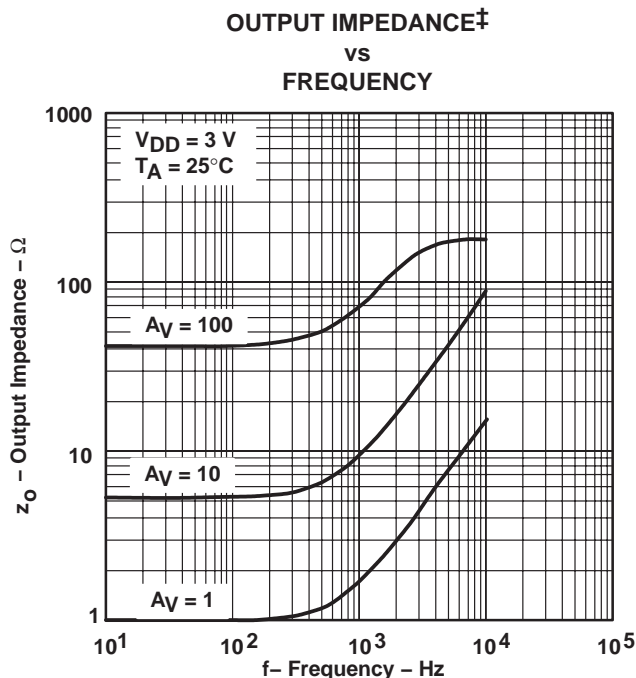


Figure 25

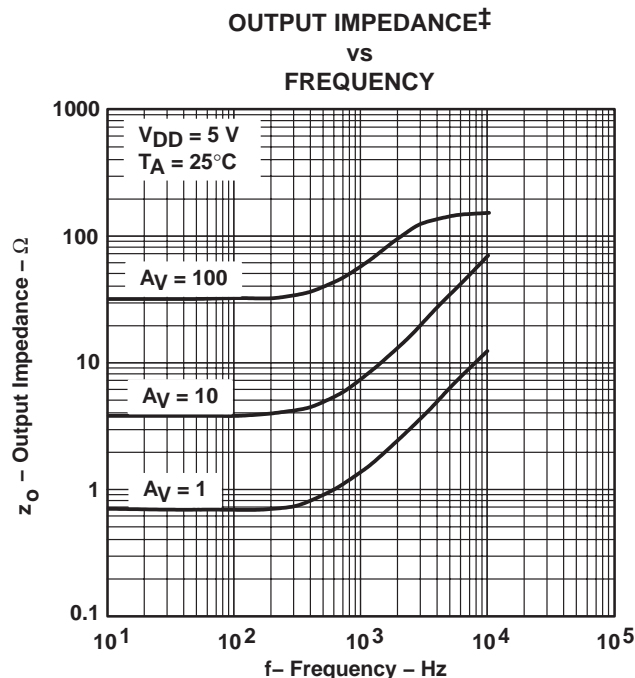


Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3\text{ V}$ , all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

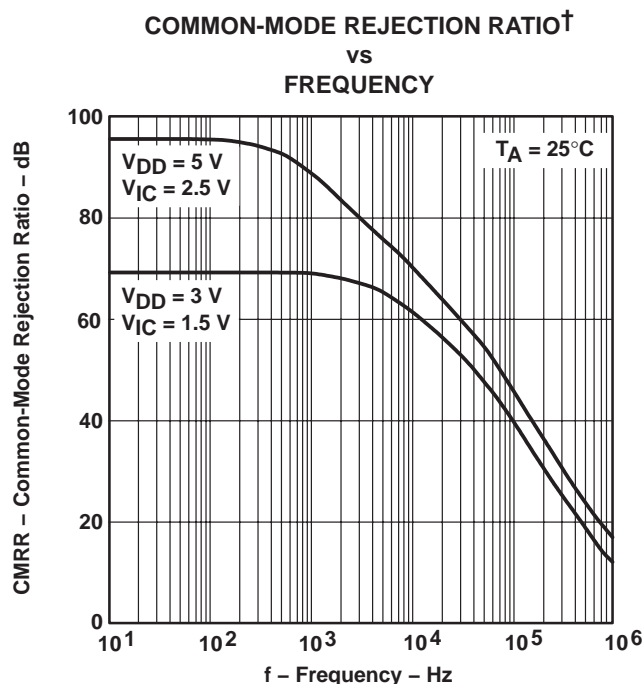


Figure 27

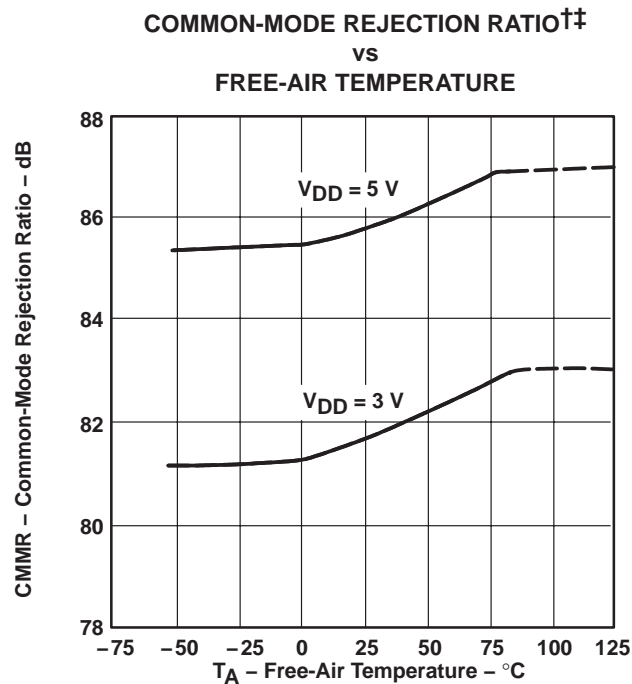


Figure 28

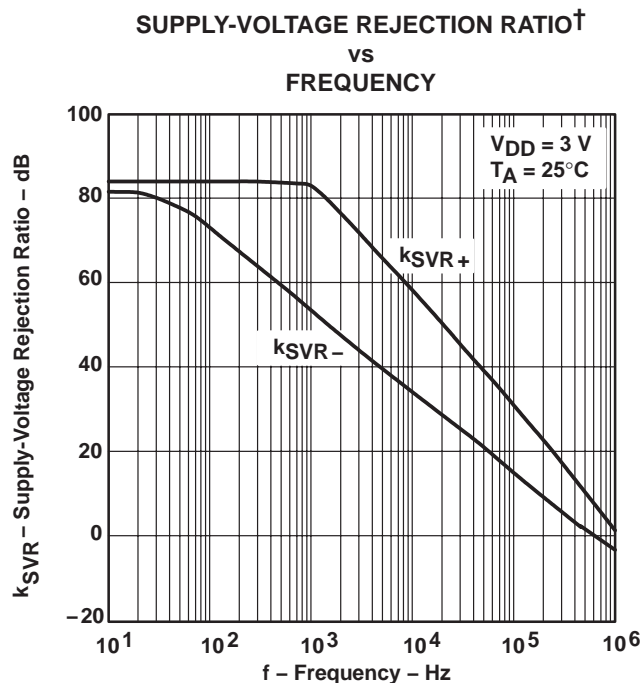


Figure 29

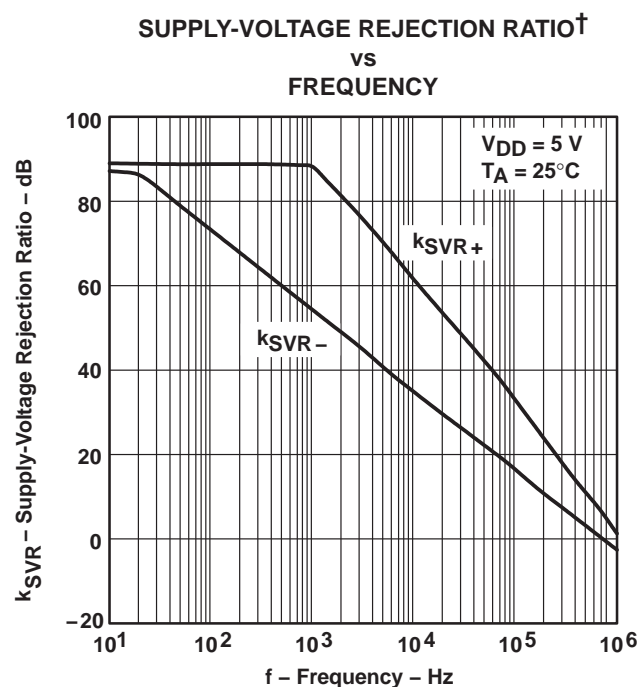


Figure 30

† For all curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3\text{ V}$ , all loads are referenced to 1.5 V.

‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS

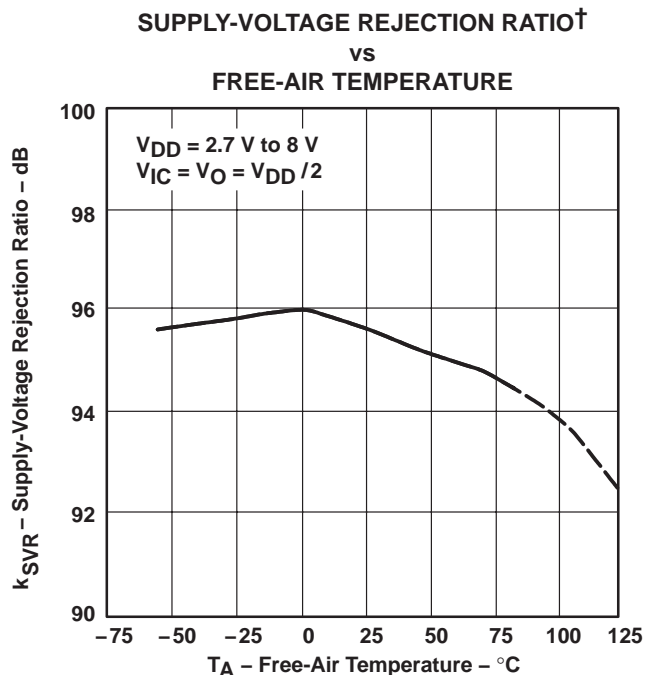


Figure 31

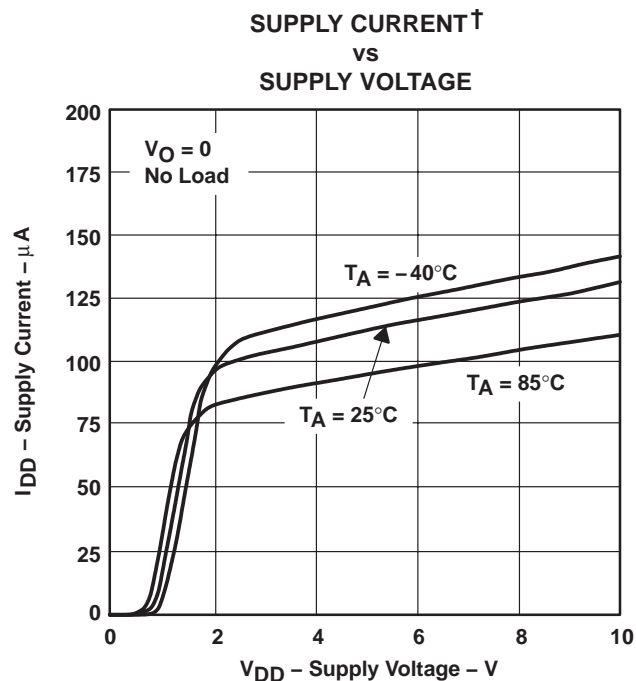


Figure 32

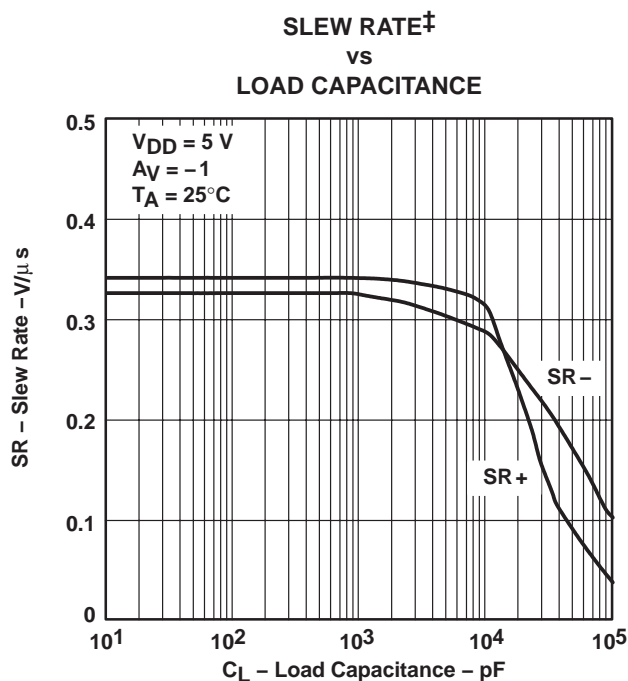


Figure 33

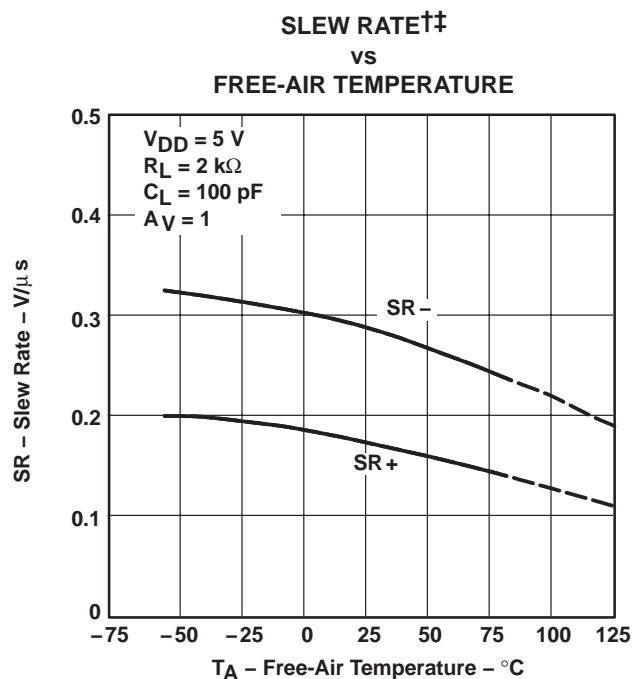


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

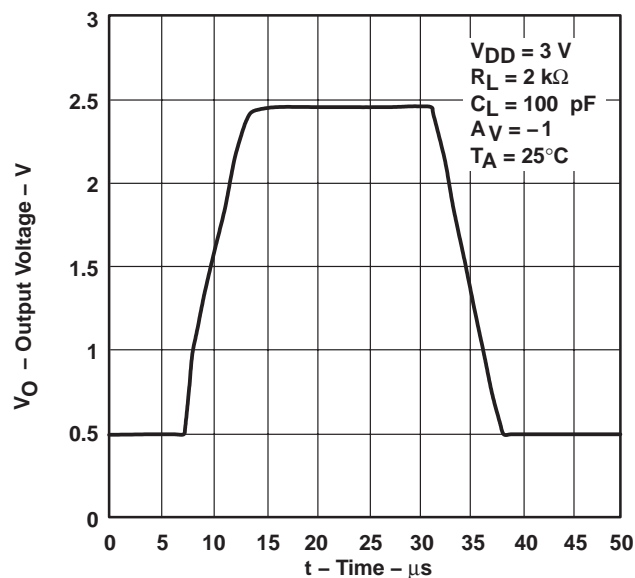
‡ For all curves where  $V_{DD} = 5 \text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3 \text{ V}$ , all loads are referenced to 1.5 V.

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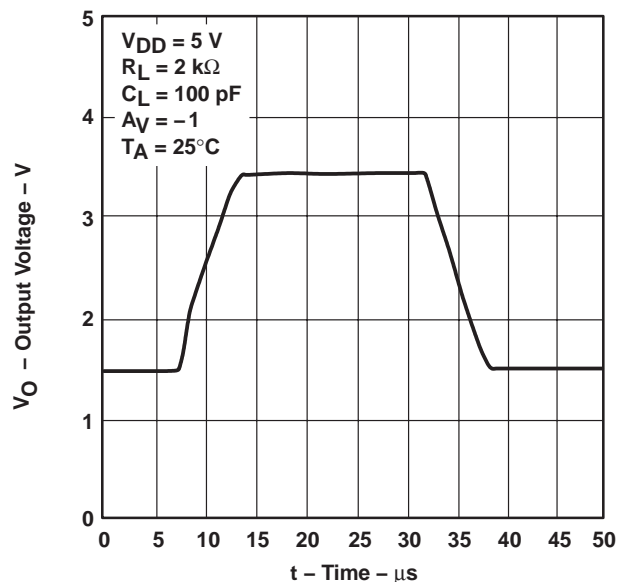
**TYPICAL CHARACTERISTICS**

**INVERTING LARGE-SIGNAL PULSE RESPONSE†**



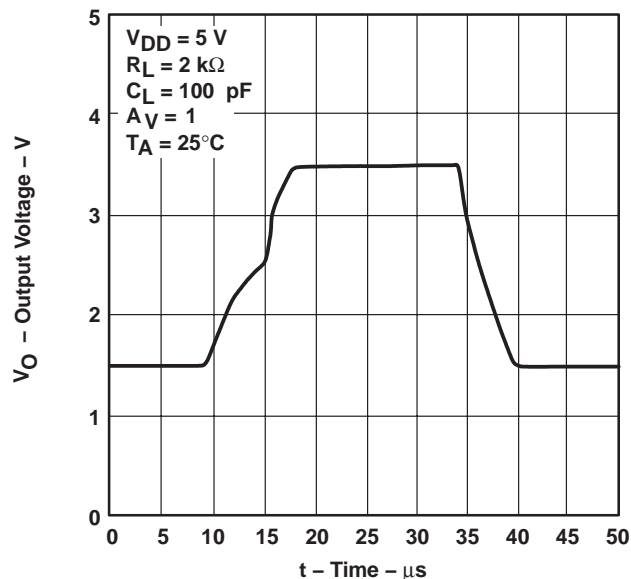
**Figure 35**

**INVERTING LARGE-SIGNAL PULSE RESPONSE†**



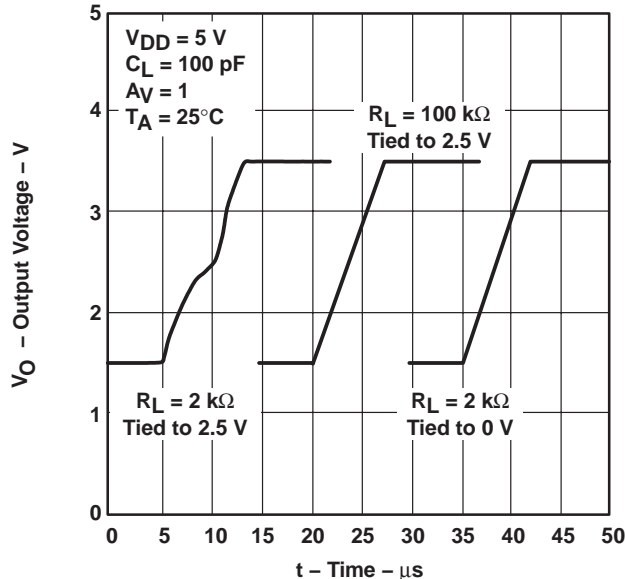
**Figure 36**

**VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†**



**Figure 37**

**VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†**



**Figure 38**

† For all curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3\text{ V}$ , all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

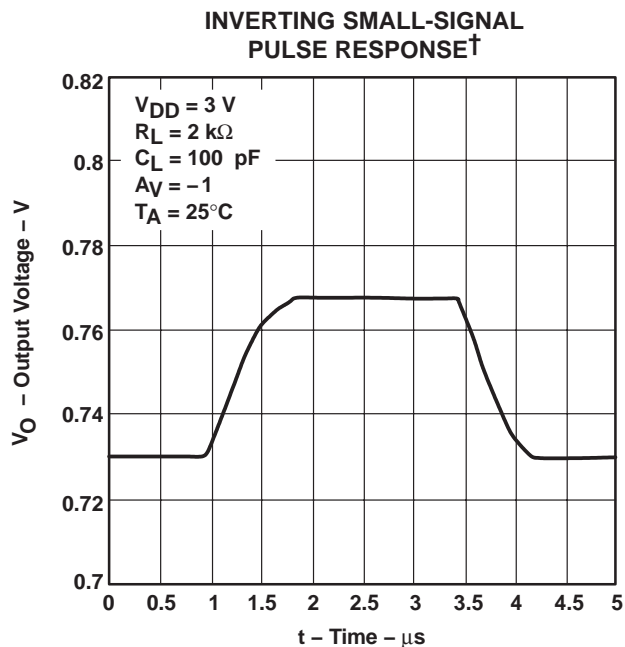


Figure 39

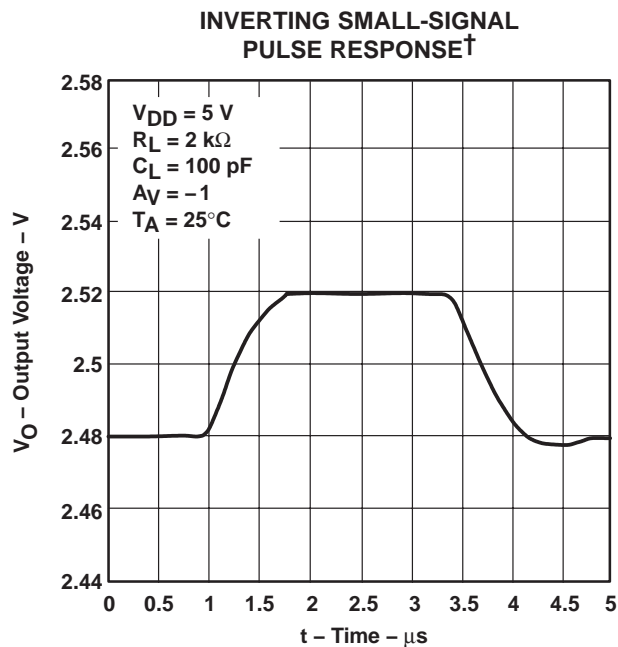


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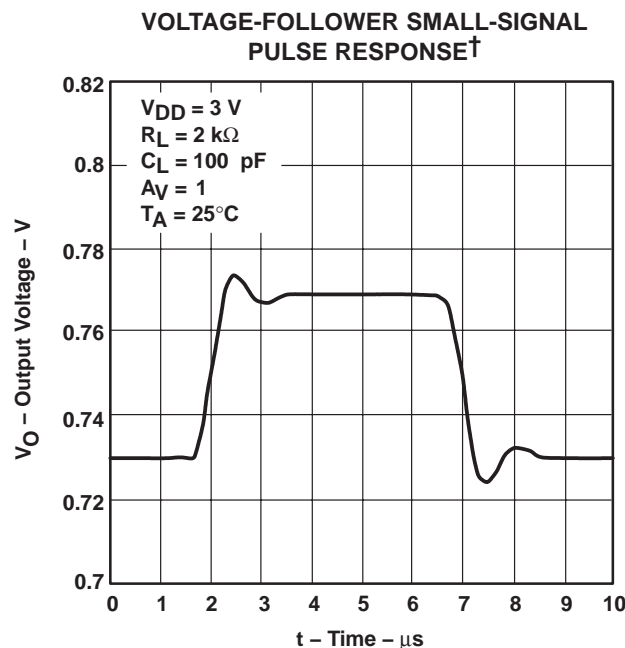


Figure 41

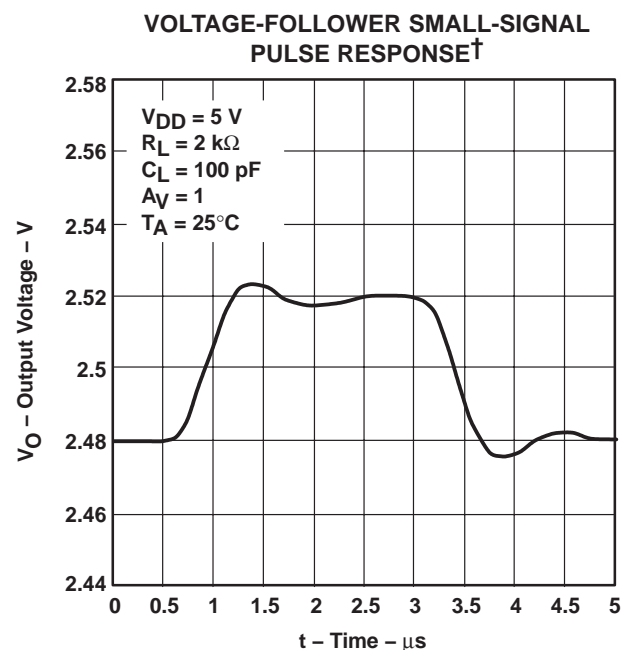


Figure 42

† For all curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3\text{ V}$ , all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

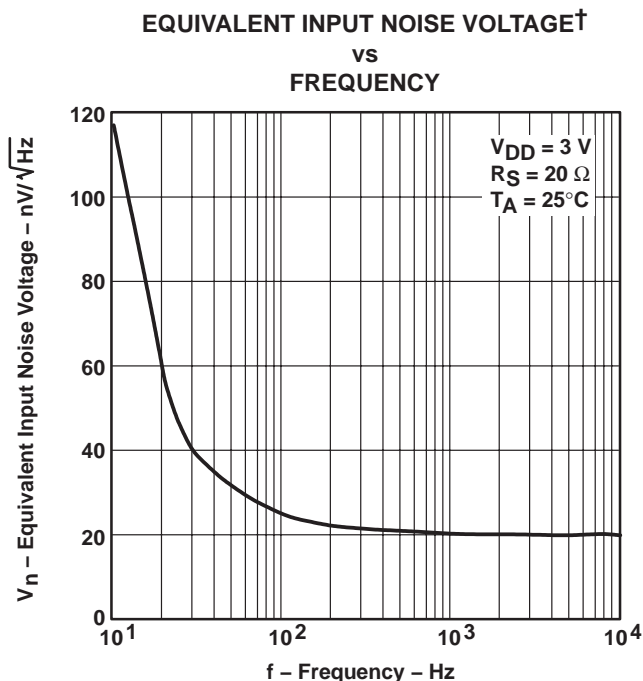


Figure 43

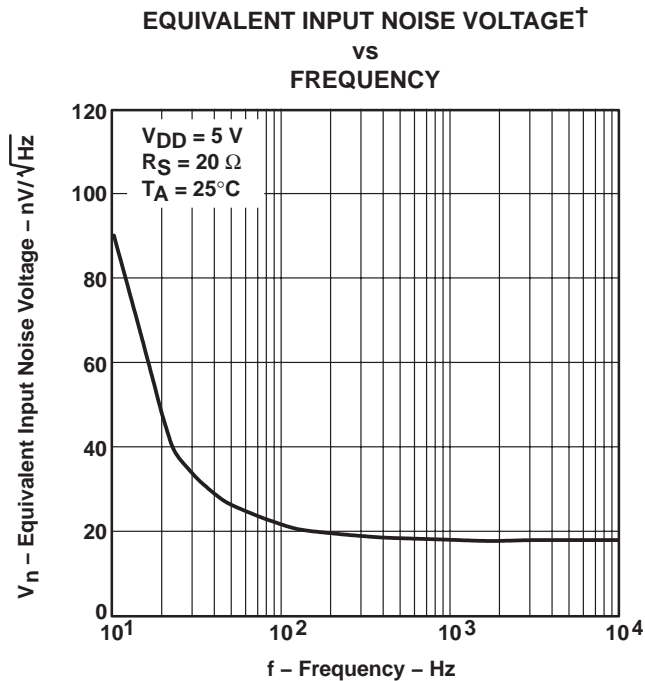


Figure 44

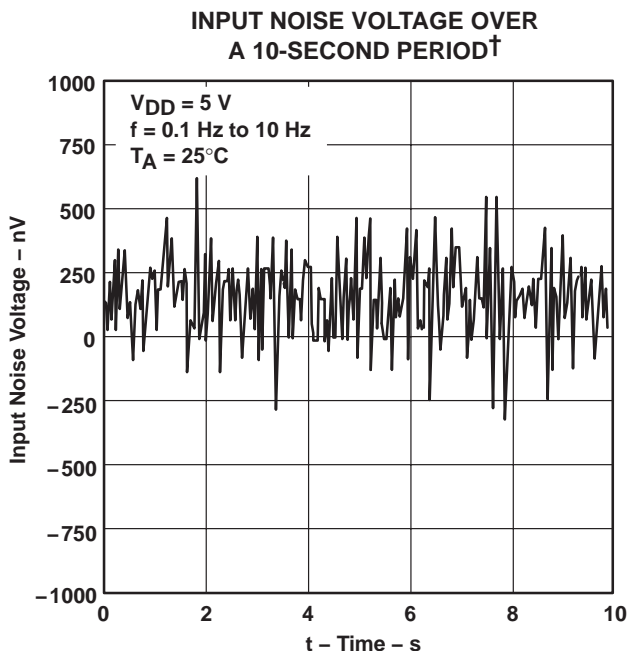


Figure 45

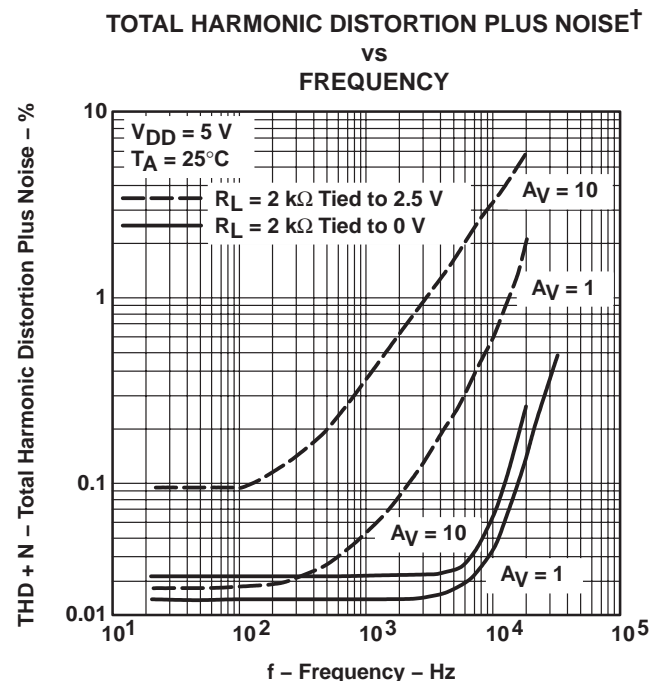


Figure 46

† For all curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to  $2.5\text{ V}$ . For all curves where  $V_{DD} = 3\text{ V}$ , all loads are referenced to  $1.5\text{ V}$ .

## TYPICAL CHARACTERISTICS

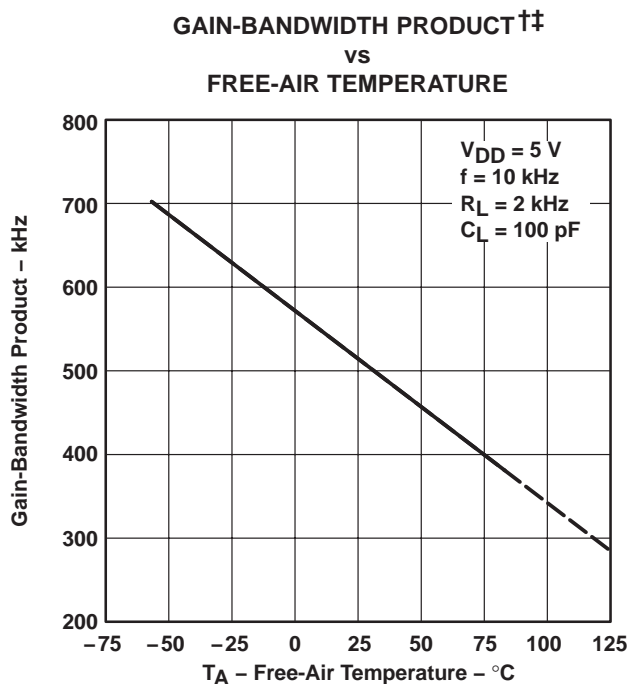


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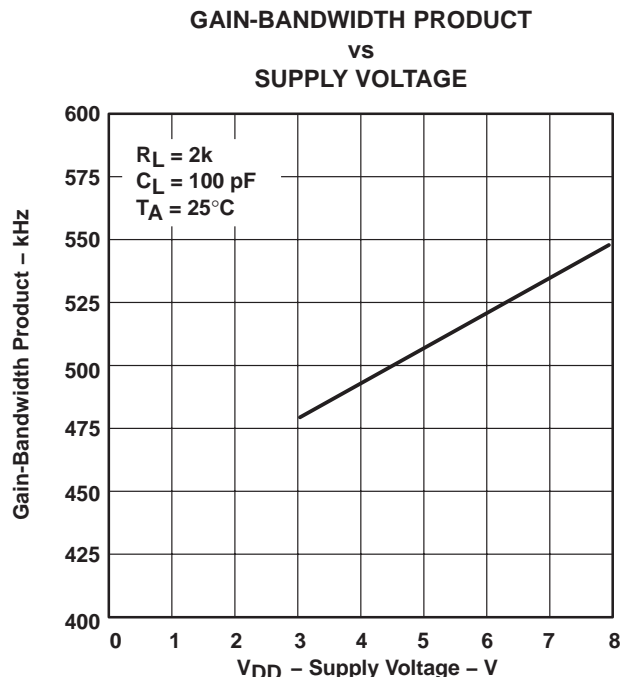


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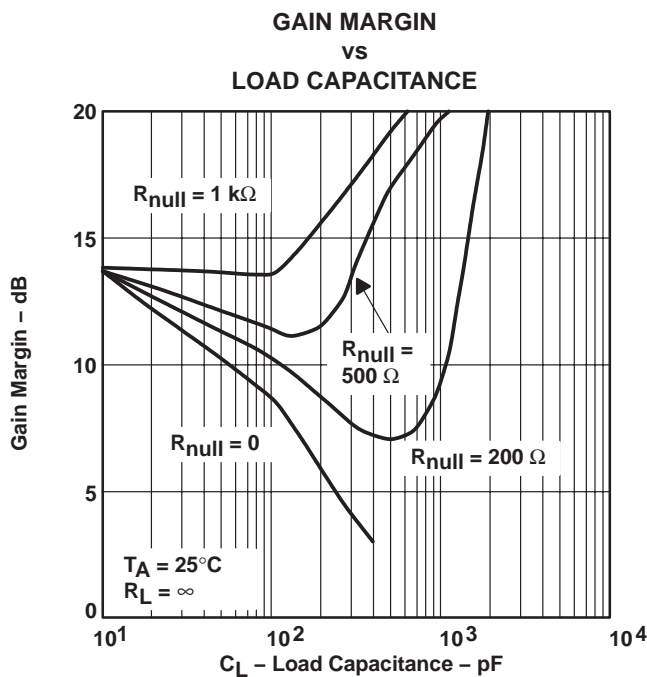


Figure 49

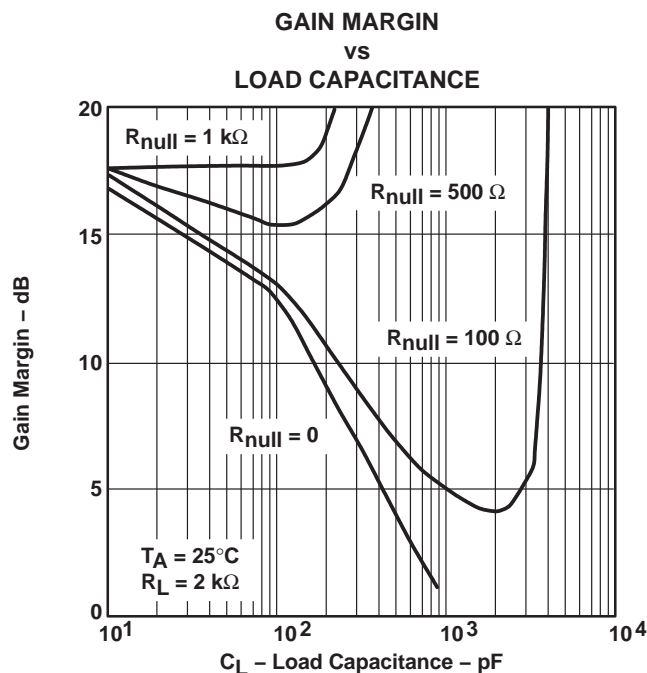


Figure 50

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where  $V_{DD} = 5\text{ V}$ , all loads are referenced to 2.5 V. For all curves where  $V_{DD} = 3\text{ V}$ , all loads are referenced to 1.5 V.

## TYPICAL CHARACTERISTICS

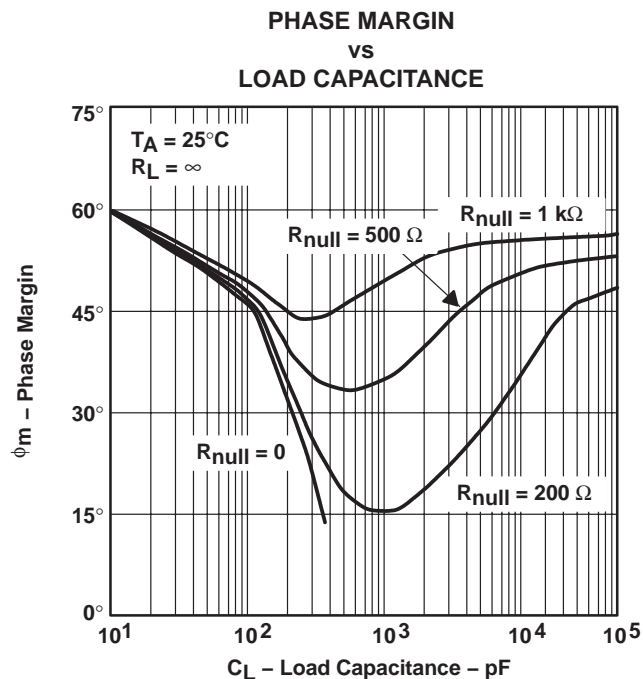


Figure 51

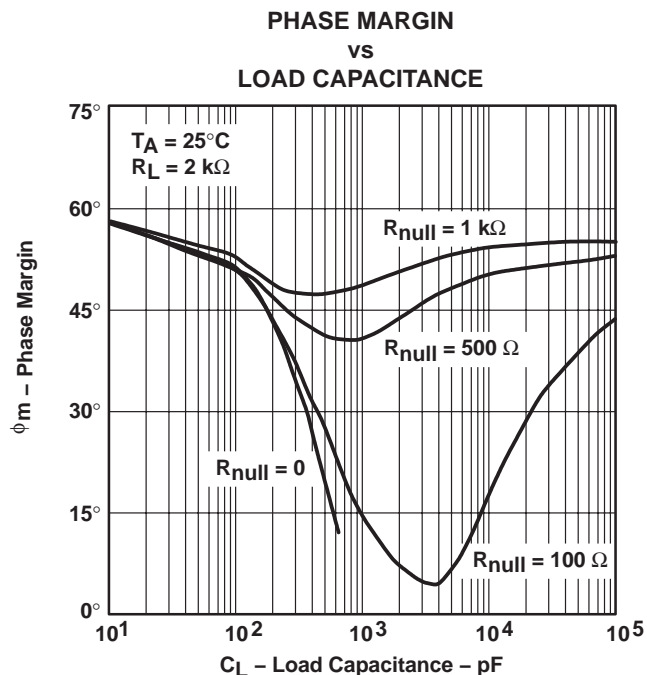


Figure 52

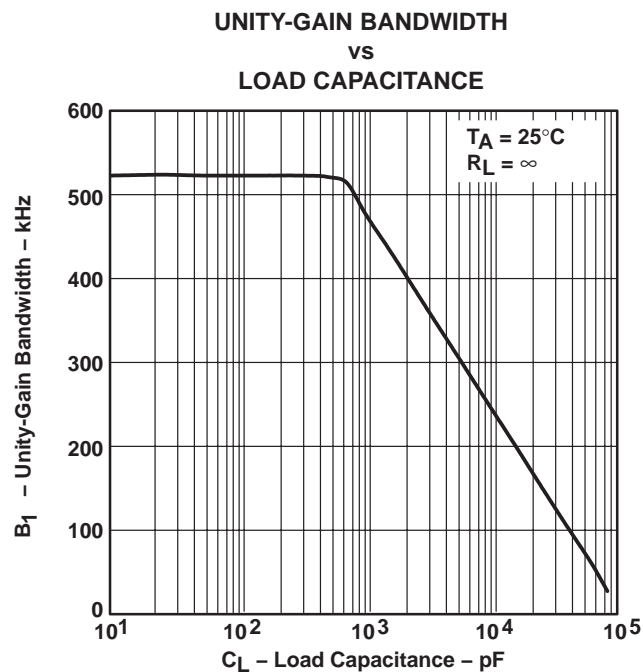


Figure 53

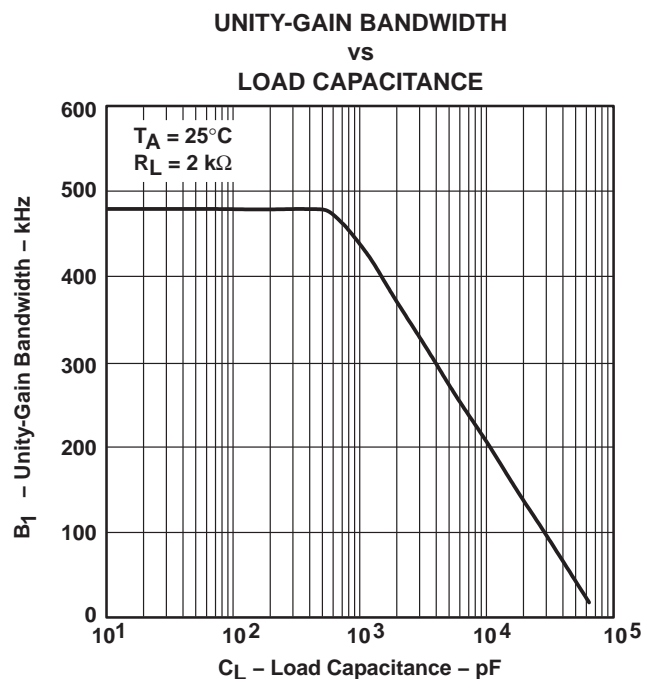


Figure 54



## APPLICATION INFORMATION

### driving large capacitive loads

The TLV2721 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 49 through Figure 54 illustrate its ability to drive loads greater than 100 pF while maintaining good gain and phase margins ( $R_{null} = 0$ ).

A small series resistor ( $R_{null}$ ) at the output of the device (Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 49 through Figure 52 show the effects of adding series resistances of 100  $\Omega$ , 200  $\Omega$ , 500  $\Omega$ , and 1 k $\Omega$ . The addition of this series resistor has two effects: the first effect is that it adds a zero to the transfer function and the second effect is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left( 2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

Where :

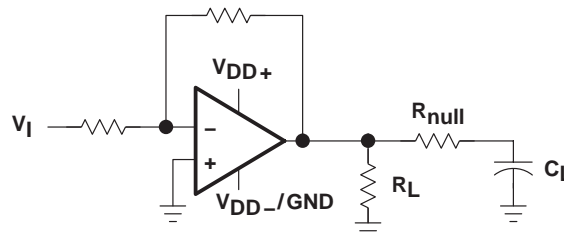
$\Delta\phi_{m1}$  = Improvement in phase margin

UGBW = Unity-gain bandwidth frequency

$R_{null}$  = Output series resistance

$C_L$  = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (Figure 53 and Figure 54). To use equation 1, UGBW must be approximated from Figure 54 and Figure 55.



**Figure 55. Series-Resistance Circuit**

The TLV2721 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500  $\mu\text{A}$  and source 1 mA at  $V_{DD} = 5\text{ V}$  at a maximum quiescent  $I_{DD}$  of 200  $\mu\text{A}$ . This provides a greater than 80% power efficiency.

When driving heavy dc loads, such as 2 k $\Omega$ , the positive edge under slewing conditions can experience some distortion. This condition can be seen in Figure 37. This condition is affected by three factors:

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 38 illustrates two 2-k $\Omega$  load conditions. The first load condition shows the distortion seen for a 2-k $\Omega$  load tied to 2.5 V. The third load condition in Figure 38 shows no distortion for a 2-k $\Omega$  load tied to 0 V.
- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 38 illustrates the difference seen on the output for a 2-k $\Omega$  load and a 100-k $\Omega$  load with both tied to 2.5 V.
- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

# TLV2721, TLV2721Y

## Advanced LinCMOS™ RAIL-TO-RAIL

### VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS197A – AUGUST 1997 – REVISED MARCH 2001

## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 56 are generated using the TLV2721 typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

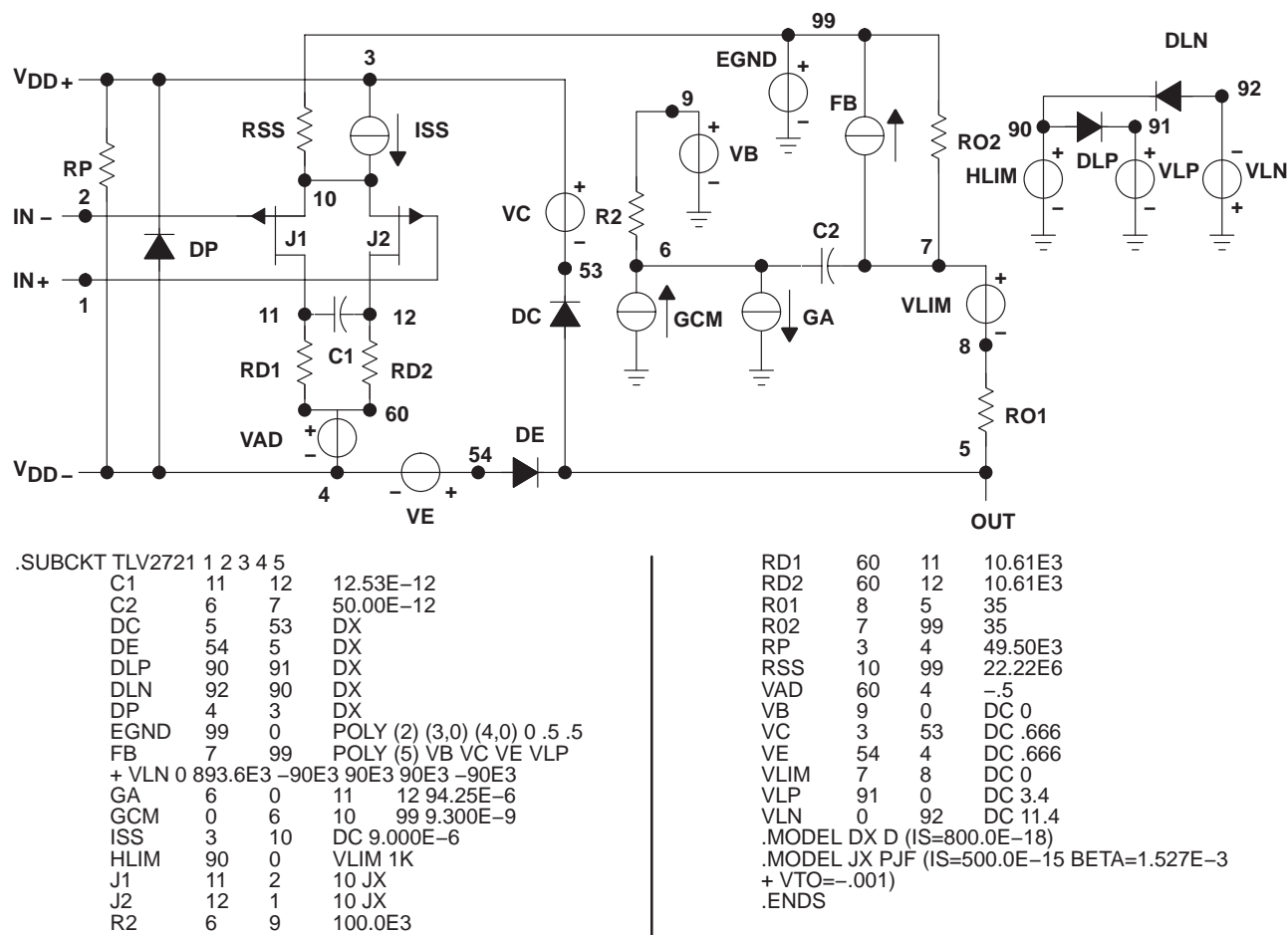


Figure 56. Boyle Macromodel and Subcircuit

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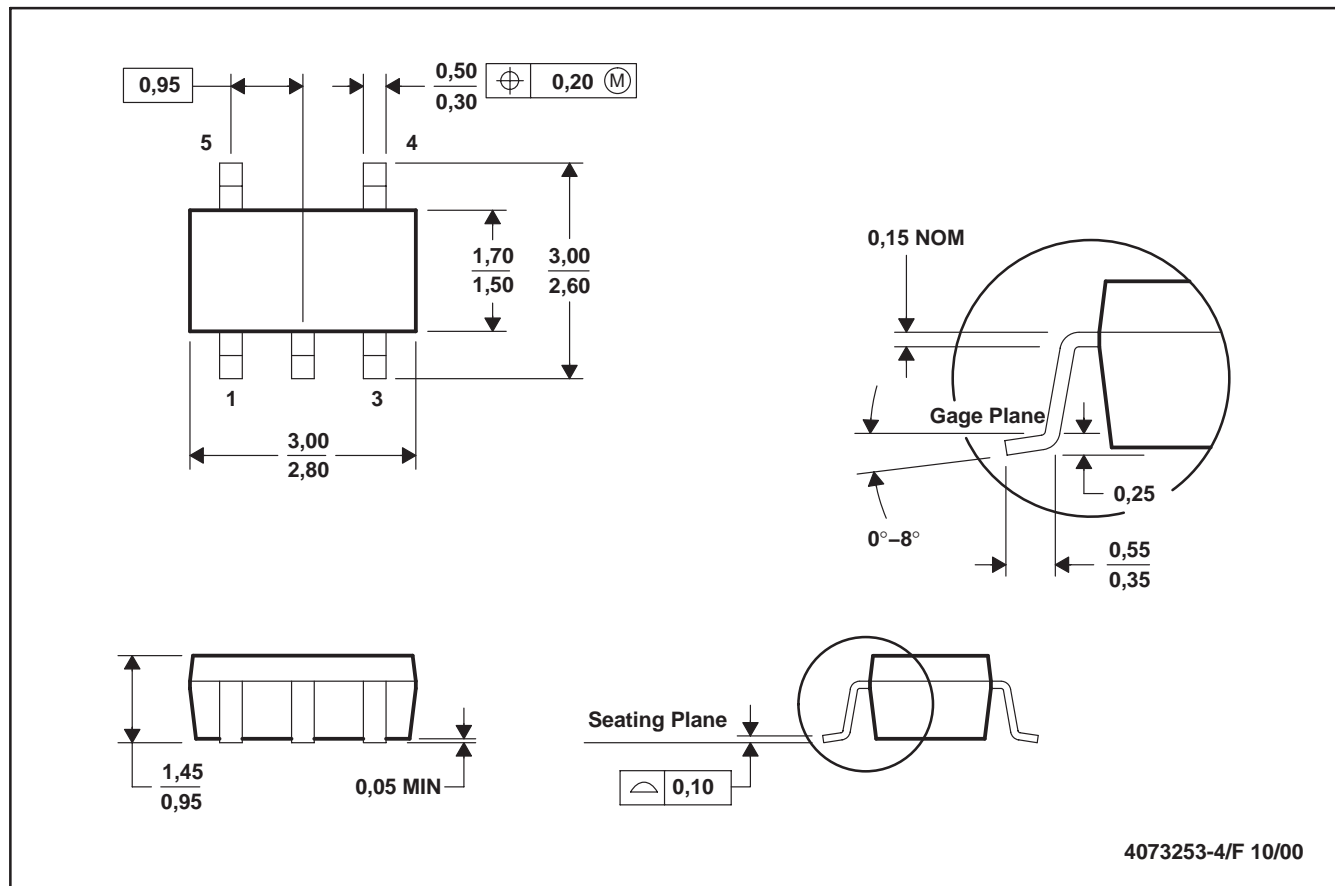


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## MECHANICAL INFORMATION

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-178

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