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FAIRCHILD

SEMICONDUCTOR®

April 2007

74ACT258
Quad 2-Input Multiplexer with 3-STATE Outputs

Features

■ I_{CC} and I_{OZ} reduced by 50%
■ Multiplexer expansion by tying outputs together
■ Inverting 3-STATE outputs
■ Outputs source/sink 24mA
■ TTL-compatible inputs

General Description

The ACT258 is a quad 2-input multiplexer with 3-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

Ordering Information

Order Number	Package Number	Package Description
74ACT258SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT258SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE 11, 5.3mm Wide
74ACT258MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

Connection Diagram
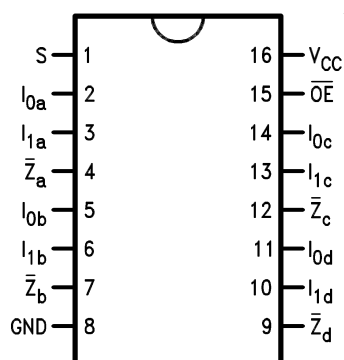
Pin Description

Pin Names	Description
S	Common Data Select Input
$\overline{OE}$	3-STATE Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
$\overline{Z}_a$–$\overline{Z}_d$	3-STATE Inverting Data Outputs

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Logic Symbol
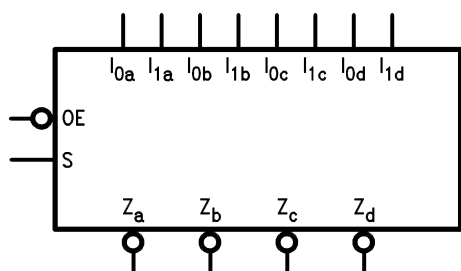
IEEE/IEC
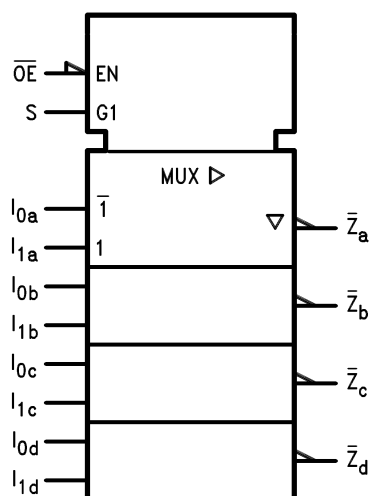
Functional Description

The ACT258 is a quad 2-input multiplexer with 3-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$

$$\overline{Z}_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$\overline{Z}_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$

$$\overline{Z}_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

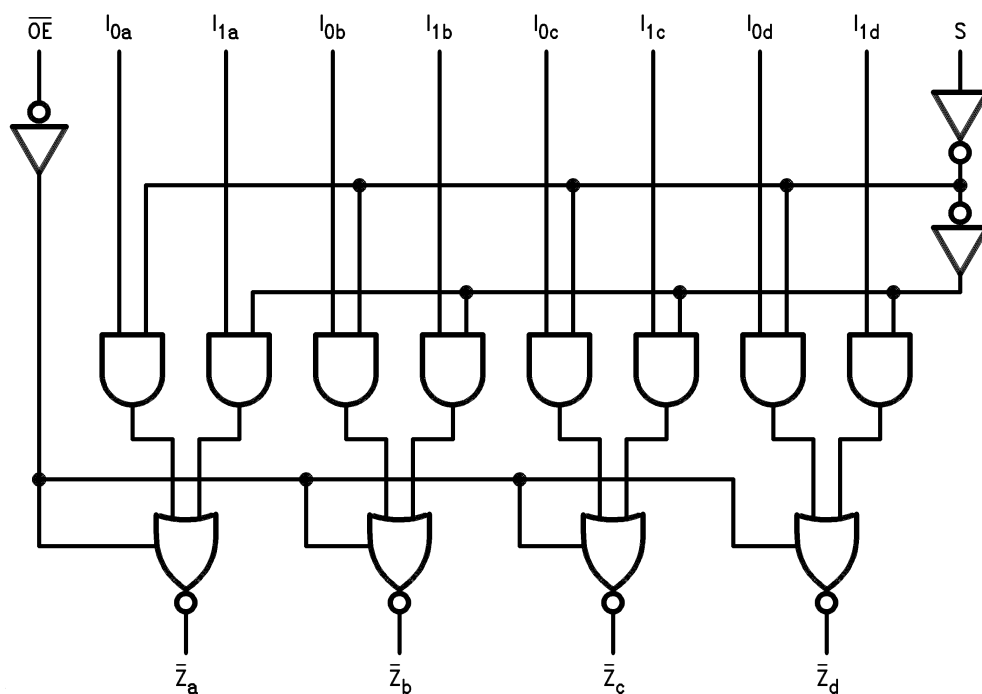| Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

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DC Electrical Characteristics

Symbol	Parameter	V_CC (V)	Conditions	T_A = +25°C Typ.	T_A = +25°C Guaranteed Limits	T_A = –40°C to +85°C Guaranteed Limits	Units
V_{IH}	Minimum HIGH Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	$I_{OUT} = -50\mu A$	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}: $I_{OH} = -24mA$		3.86	3.76	
		5.5	$I_{OH} = -24mA$[1]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	$I_{OUT} = 50\mu A$	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}: $I_{OL} = 24mA$		0.36	0.44	
		5.5	$I_{OL} = 24mA$[1]		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	μA
I_{OZ}	Maximum 3-STATE Current	5.5	$V_I = V_{IL}, V_{IH}$; $V_O = V_{CC}$, GND		±0.25	±2.5	μA
I_{CCT}	Maximum I_{CC}/Input	5.5	$V_I = V_{CC} - 2.1V$	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current[2]	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}		5.5	$V_{OHD} = 3.85V$ Min.			–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.

2. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)[3]	T_A = +25°C, C_L = 50pF			T_A = −40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, I_n to $\overline{Z}_n$	5.0	2.0	6.5	8.5	1.5	9.5	ns
t_{PHL}	Propagation Delay, I_n to $\overline{Z}_n$	5.0	2.0	5.5	7.5	1.5	8.0	ns
t_{PLH}	Propagation Delay, S to $\overline{Z}_n$	5.0	3.0	7.5	10.5	2.0	11.5	ns
t_{PHL}	Propagation Delay, S to $\overline{Z}_n$	5.0	1.5	7.0	9.5	1.5	11.0	ns
t_{PZH}	Output Enable Time	5.0	2.0	6.5	8.5	1.5	9.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	6.5	8.5	1.5	9.5	ns
t_{PHZ}	Output Disable Time	5.0	1.5	7.0	9.0	1.0	10.0	ns
t_{PLZ}	Output Disable Time	5.0	2.0	6.0	8.0	1.5	9.0	ns

Notes:

3. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	55.0	pF

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

LAND PATTERN RECOMMENDATION

SEE DETAIL A

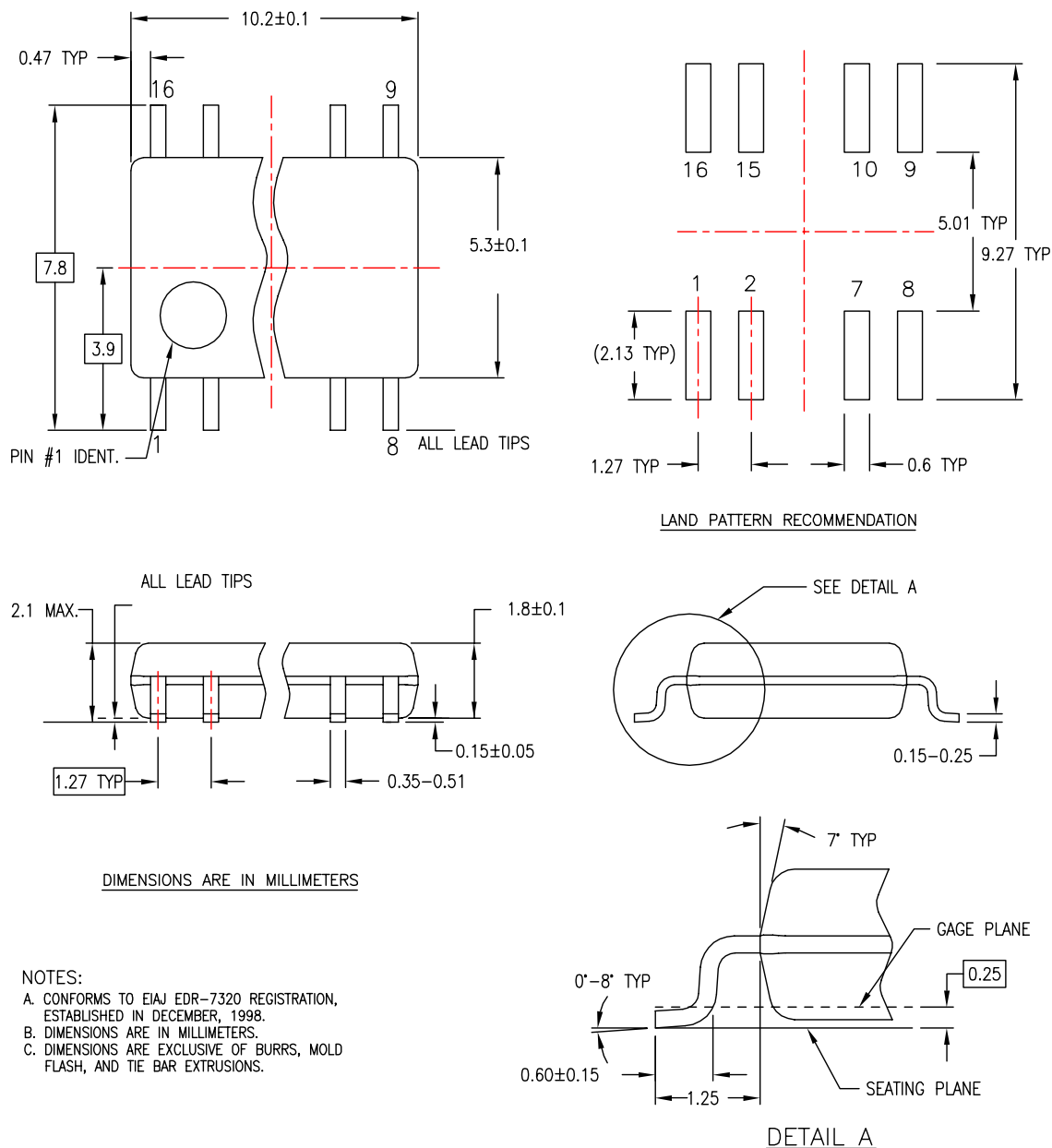NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS−012, VARIATION AC, ISSUE C, DATED MAY 1990.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) STANDARD LEAD FINISH: 200 MICROINCHES / 5.08 MICRONS MIN. LEAD/TIN (SOLDER) ON COPPER.
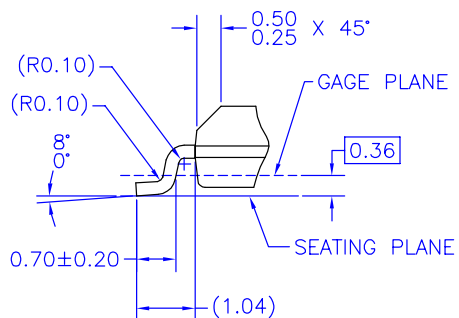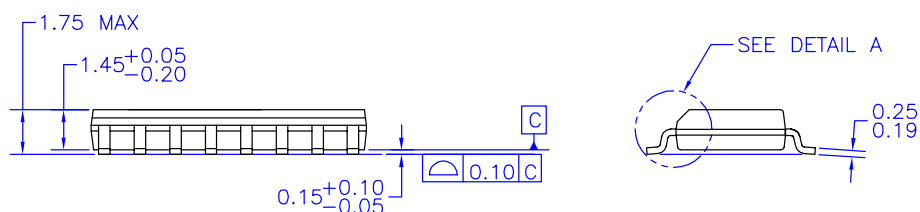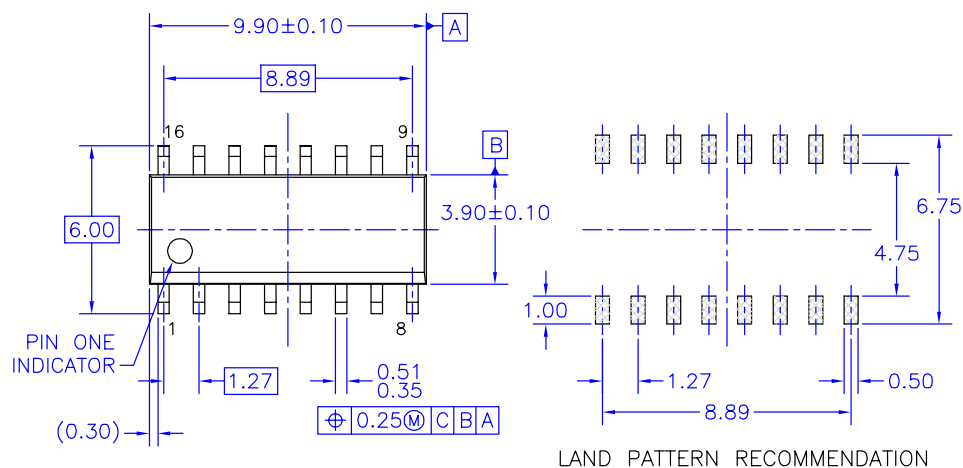
DETAIL A
SCALE: 2:1

M16AREVK

Figure 2. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

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Physical Dimensions (Continued)
Dimensions are in millimeters unless otherwise noted.

10.2±0.1

0.47 TYP

16   9

7.8

3.9

5.3±0.1

PIN #1 IDENT.   1

8 ALL LEAD TIPS

16   15   10   9

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   7   8

1.27 TYP   0.6 TYP

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS

2.1 MAX.

1.8±0.1

0.15±0.05

1.27 TYP   0.35−0.51

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15−0.25

7° TYP

GAGE PLANE

0.25

0°−8° TYP

0.60±0.15

1.25

SEATING PLANE

DETAIL A

NOTES:
A. CONFORMS TO EIAJ EDR−7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
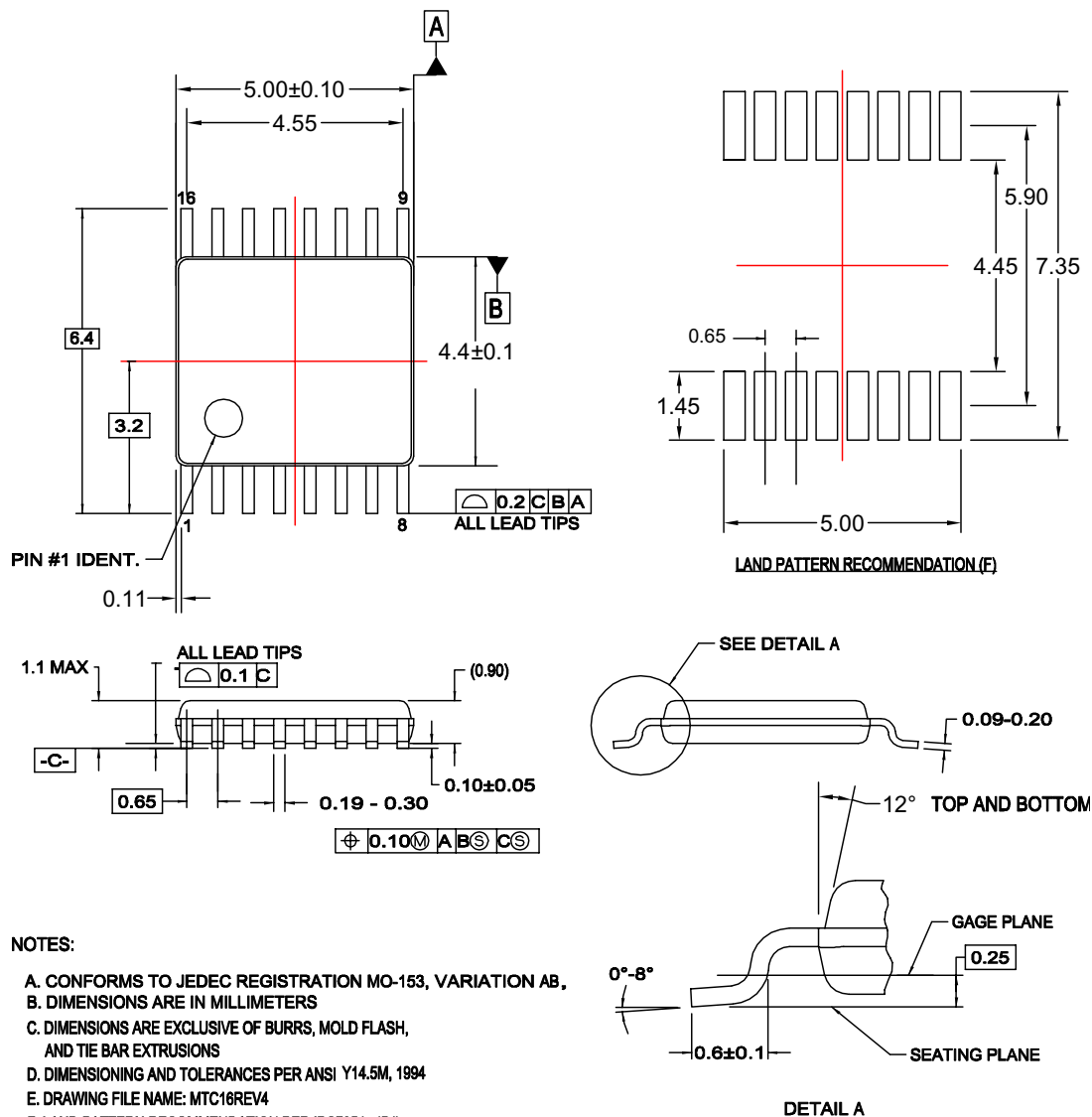
M16DREVC

Figure 3. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)
Dimensions are in millimeters unless otherwise noted.

A

5.00±0.10

4.55

16   9

6.4

3.2

4.4±0.1

B

⬡ 0.2 C B A
ALL LEAD TIPS

1   8

PIN #1 IDENT.

0.11

ALL LEAD TIPS
⬡ 0.1 C

1.1 MAX

(0.90)

-C-

0.65   0.19 - 0.30

0.10±0.05

⊕ 0.10 Ⓜ A BⓈ CⓈ

LAND PATTERN RECOMMENDATION (F)

5.90

4.45   7.35

0.65

1.45

5.00

SEE DETAIL A

0.09-0.20

12°   TOP AND BOTTOM

GAGE PLANE

0.25

0°-8°

0.6±0.1

SEATING PLANE

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB.
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
   AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID#
   TSOP65P640X110-16N

MTC16rev4

**Figure 4. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

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