

H5N2509P

Silicon N Channel MOS FET High Speed Power Switching

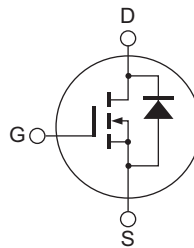
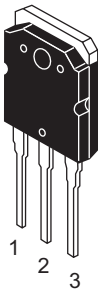
REJ03G1109-0200
(Previous: ADE-208-1378)
Rev.2.00
Sep 07, 2005

Features

- Low on-resistance: $R_{DS(on)} = 0.053 \Omega$ typ.
- Low leakage current: $I_{DSS} = 1 \mu A$ max (at $V_{DS} = 250 V$, $V_{GS} = 0 V$)
- High speed switching: $t_f = 110 ns$ typ (at $I_D = 15 A$, $R_L = 8.3 \Omega$, $V_{GS} = 10 V$)
- Low gate charge: $Q_g = 110 nC$ typ (at $V_{DD} = 200 V$, $V_{GS} = 10 V$, $I_D = 30 A$)
- Avalanche ratings

Outline

RENESAS Package code: PRSS0004ZE-A
(Package name: TO-3P)



1. Gate
2. Drain (Flange)
3. Source

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DS}	250	V
Gate to source voltage	V_{GS}	±30	V
Drain current	I_D	30	A
Drain peak current	$I_{D (pulse)}$ ^{Note 1}	120	A
Body-drain diode reverse drain current	I_{DR}	30	A
Body-drain diode reverse drain peak current	$I_{DR (pulse)}$ ^{Note 1}	120	A
Avalanche current	I_{AP} ^{Note 3}	30	A
Channel dissipation	P_{ch} ^{Note 2}	150	W
Channel to case thermal Impedance	θ_{ch-c}	0.833	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. Value at $T_c = 25^\circ C$ 3. $T_{ch} \leq 150^\circ C$

Electrical Characteristics

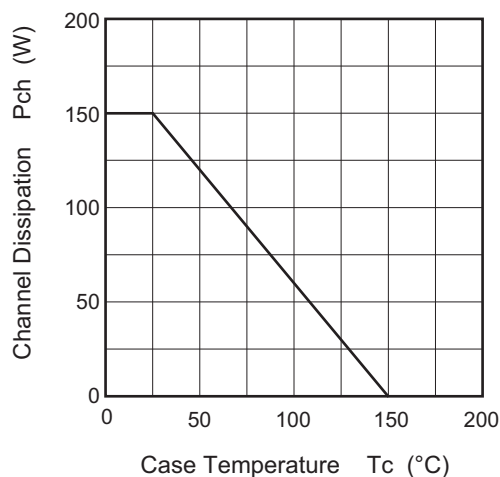
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR) DSS}$	250	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 250 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS (off)}$	3.0	—	4.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS (on)}$	—	0.053	0.069	Ω	$I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	17	28	—	S	$I_D = 15 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	3600	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	450	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	115	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d (on)}$	—	48	—	ns	$I_D = 15 \text{ A}$
Rise time	t_r	—	120	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d (off)}$	—	190	—	ns	$R_L = 8.3 \Omega$
Fall time	t_f	—	110	—	ns	$R_g = 10 \Omega$
Total gate charge	Q_g	—	110	—	nC	$V_{DD} = 200 \text{ V}$
Gate to source charge	Q_{gs}	—	19	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	53	—	nC	$I_D = 30 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.9	1.35	V	$I_F = 30 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	210	—	ns	$I_F = 30 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery charge	Q_{rr}	—	1.8	—	μC	$di_F/dt = 100 \text{ A}/\mu s$

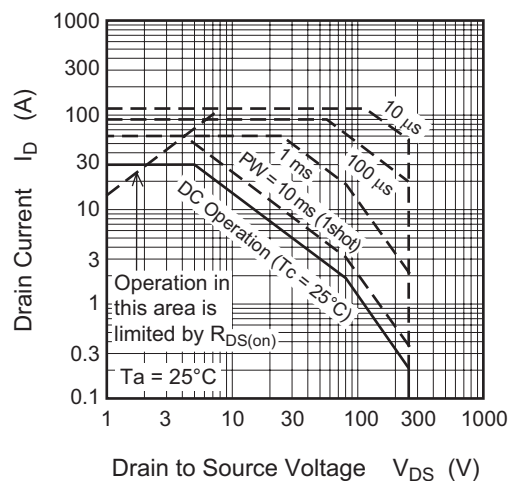
Note: 4. Pulse test

Main Characteristics

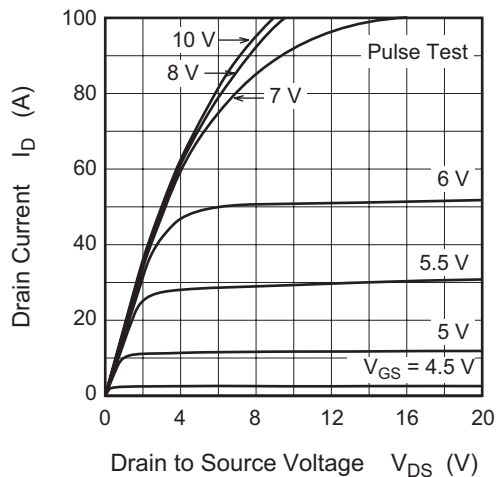
Power vs. Temperature Derating



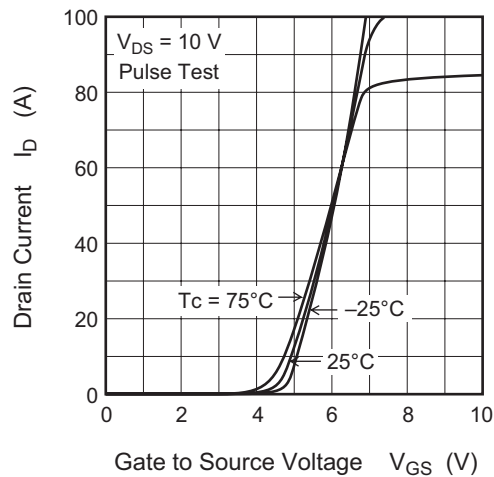
Maximum Safe Operation Area



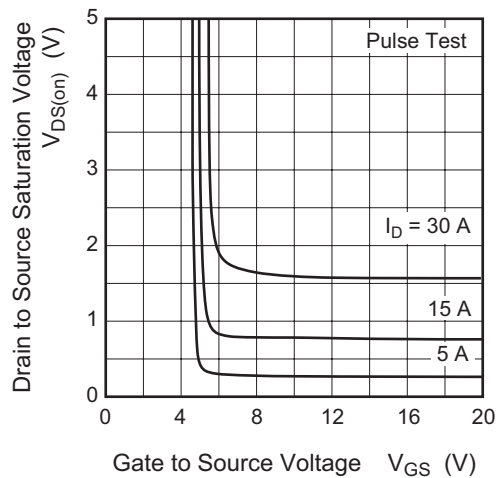
Typical Output Characteristics



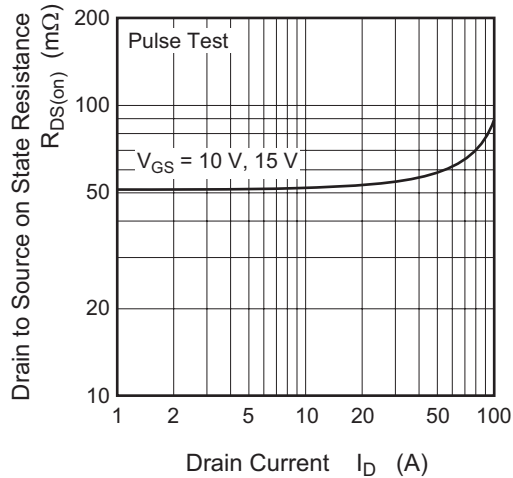
Typical Transfer Characteristics

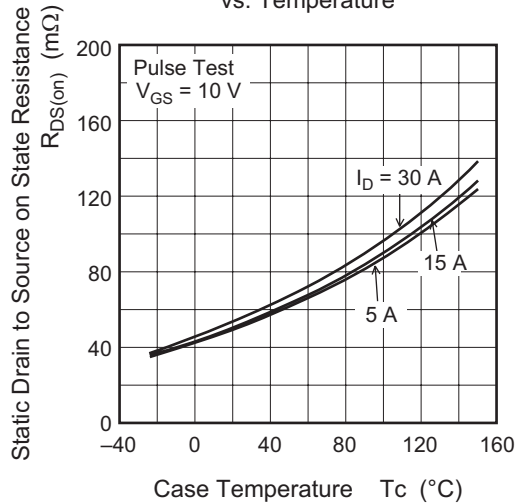
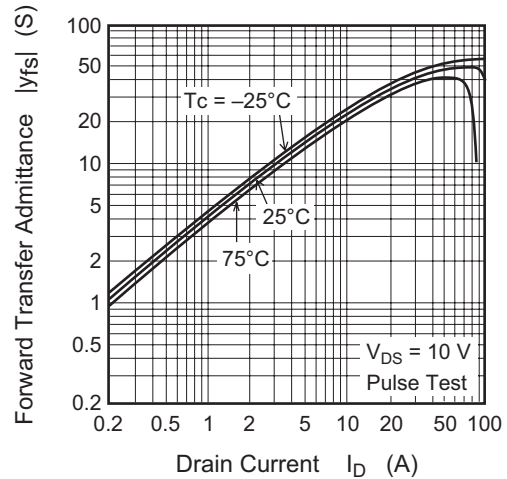
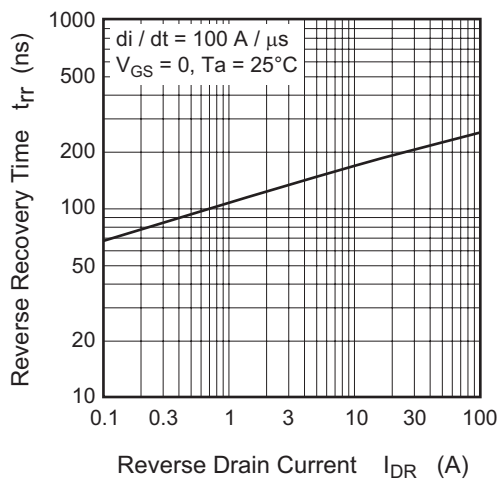
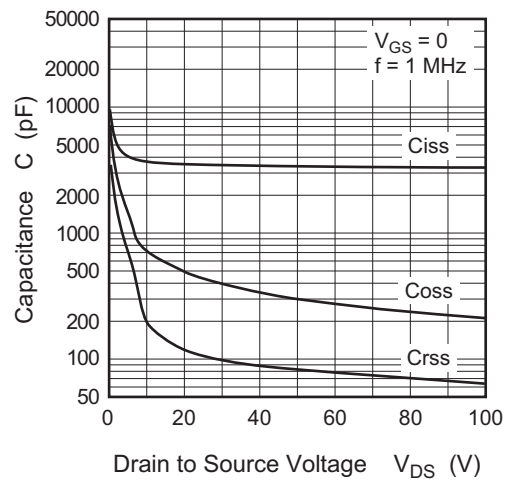


Drain to Source Saturation Voltage vs. Gate to Source Voltage

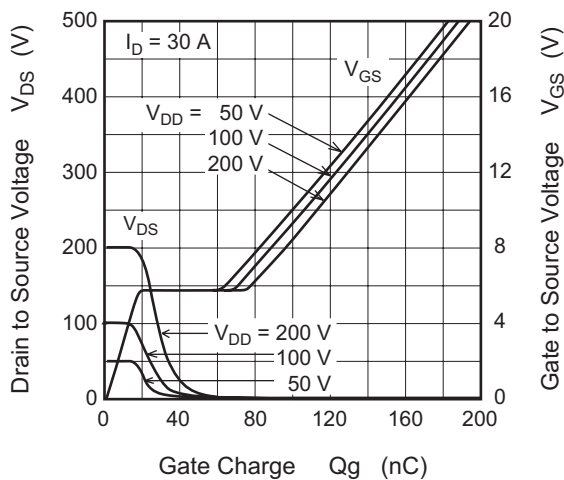


Static Drain to Source on State Resistance vs. Drain Current

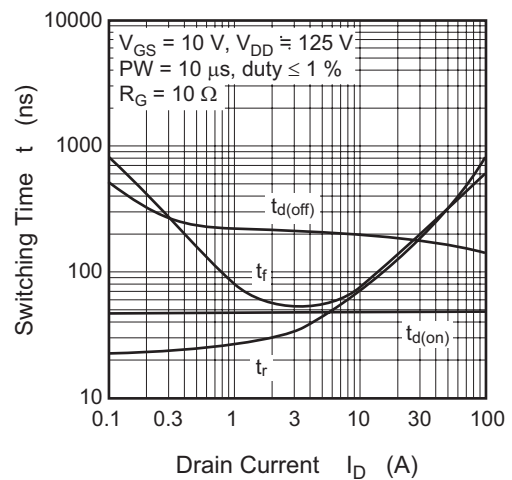


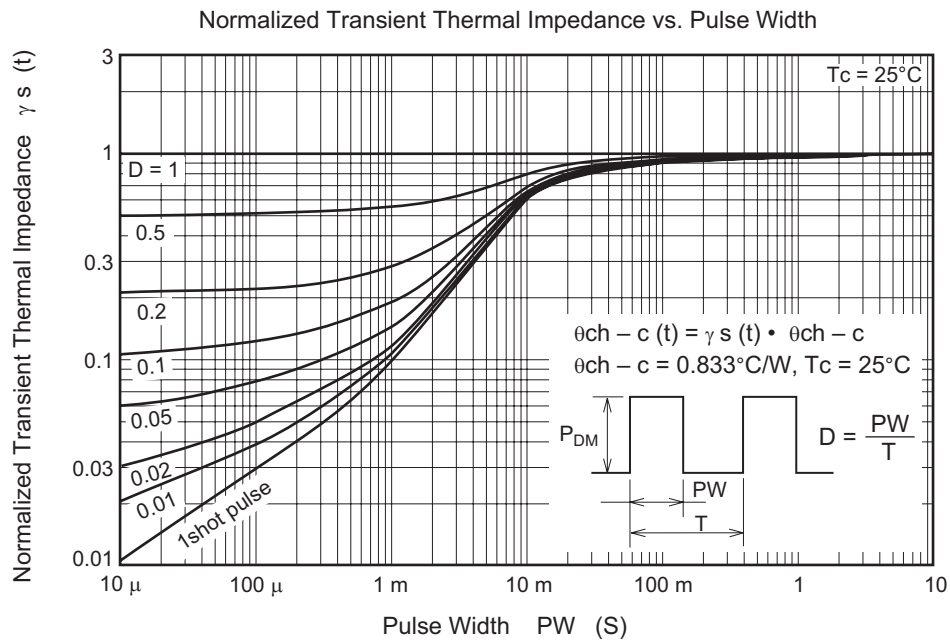
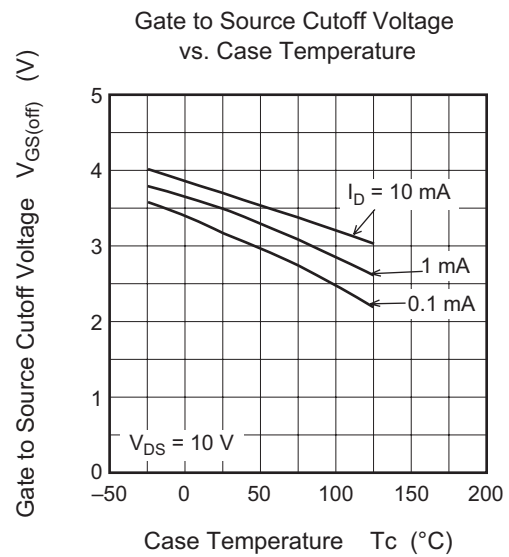
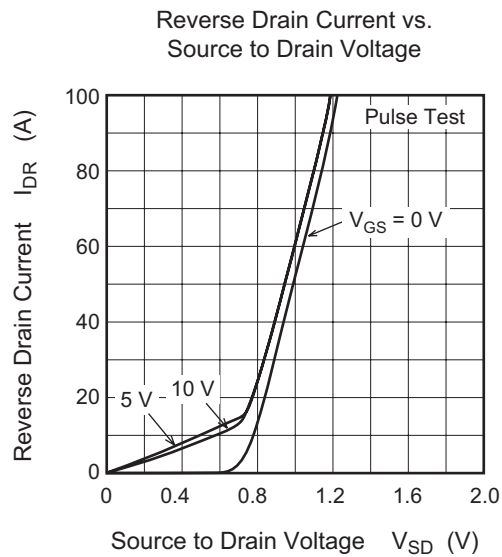
Static Drain to Source on State Resistance
vs. TemperatureForward Transfer Admittance vs.
Drain CurrentBody-Drain Diode Reverse
Recovery TimeTypical Capacitance vs.
Drain to Source Voltage

Dynamic Input Characteristics

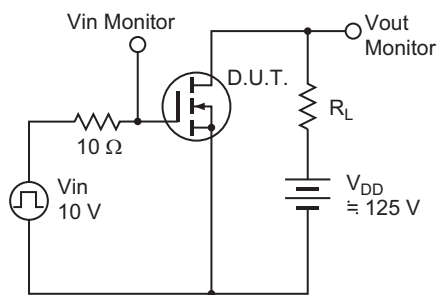


Switching Characteristics

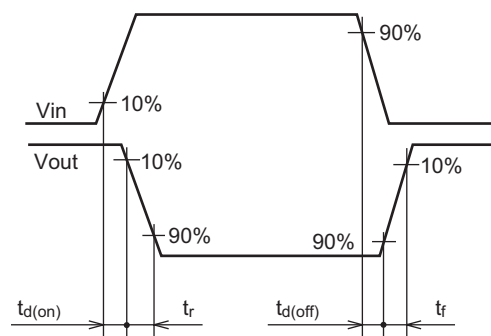




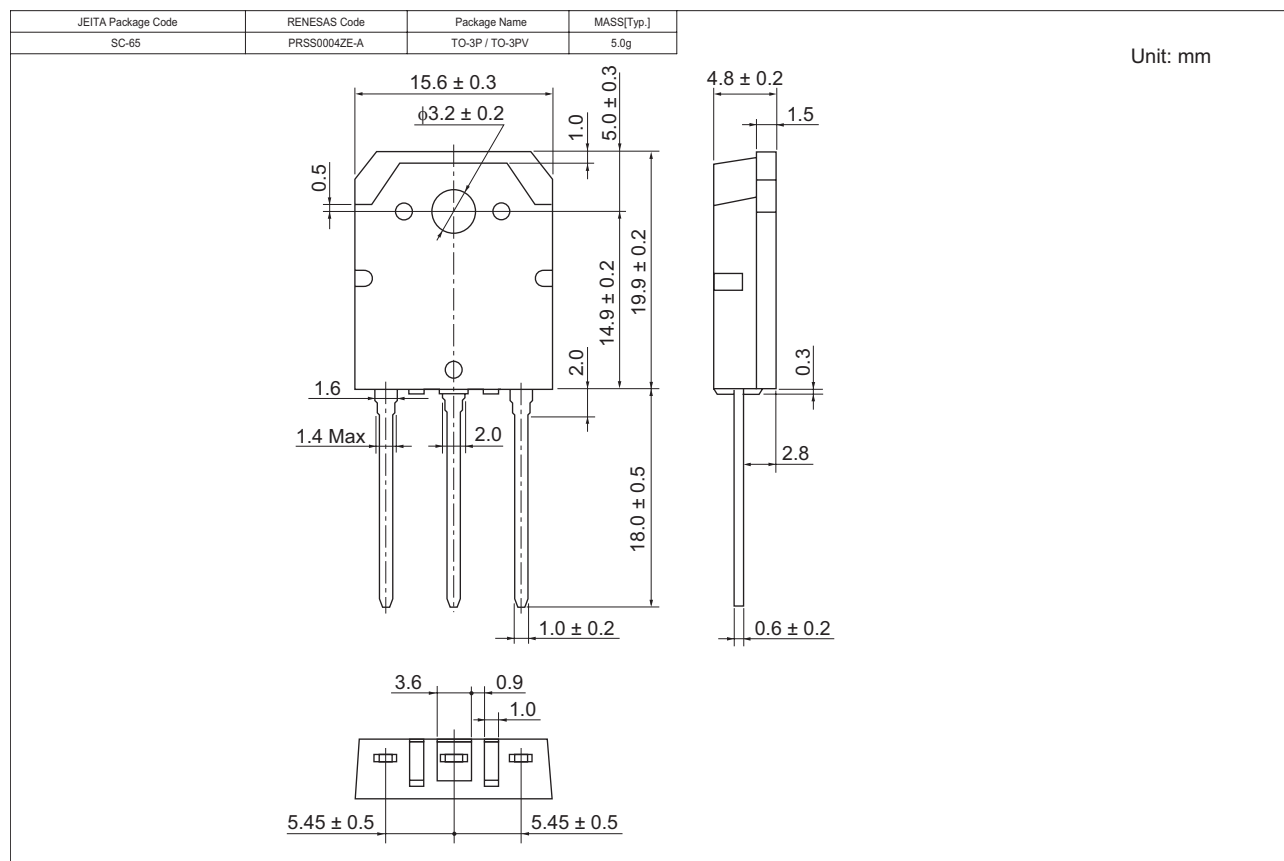
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
H5N2509P-E	360 pcs	Box (Tube)

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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