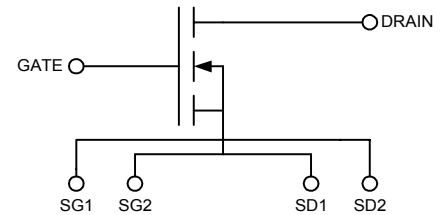


N-Channel Enhancement Mode
Low Q_g and R_g
High dv/dt
Nanosecond Switching

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	200	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1\text{ M}\Omega$	200	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_c = 25^\circ\text{C}$	15.0	A
I_{DM}	$T_c = 25^\circ\text{C}$, pulse width limited by T_{JM}	90	A
I_{AR}	$T_c = 25^\circ\text{C}$	9.0	A
E_{AR}	$T_c = 25^\circ\text{C}$	7.5	mJ
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 0.2\Omega$	5	V/ns
	$I_S = 0$	>200	V/ns
P_{DC}		200	W
P_{DHS}	$T_c = 25^\circ\text{C}$ Derate $4.4\text{ W}/^\circ\text{C}$ above 25°C	80	W
P_{DAMB}	$T_c = 25^\circ\text{C}$	3.5	W
R_{thJC}		0.74	C/W
R_{thJHS}		1.15	C/W

Symbol	Test Conditions	Characteristic Values		
		$T_J = 25^\circ\text{C}$ unless otherwise specified		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0\text{ V}$, $I_D = 3\text{ ma}$	200		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 4\text{ ma}$	2	3	4 V
I_{GSS}	$V_{GS} = \pm 20\text{ V}_{DC}$, $V_{DS} = 0$			$\pm 100\text{ nA}$
I_{DSS}	$V_{DS} = 0.8 V_{DSS}$, $T_J = 25^\circ\text{C}$ $V_{GS} = 0$, $T_J = 125^\circ\text{C}$			25 μA 250 μA
$R_{DS(on)}$	$V_{GS} = 15\text{ V}$, $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300\mu\text{s}$, duty cycle $d \leq 2\%$			0.2 Ω
g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 0.5 I_{D25}$, pulse test	3.0	8.0	S
T_J		-55		+175 $^\circ\text{C}$
T_{JM}			1750	$^\circ\text{C}$
T_{stg}		-55		+175 $^\circ\text{C}$
T_L	1.6mm (0.063 in) from case for 10 s		300	$^\circ\text{C}$
Weight			2	g

$$\begin{aligned} V_{DSS} &= 200\text{ V} \\ I_{D25} &= 15\text{ A} \\ R_{DS(on)} &= 0.2\ \Omega \\ P_{DC} &= 200\text{ W} \end{aligned}$$



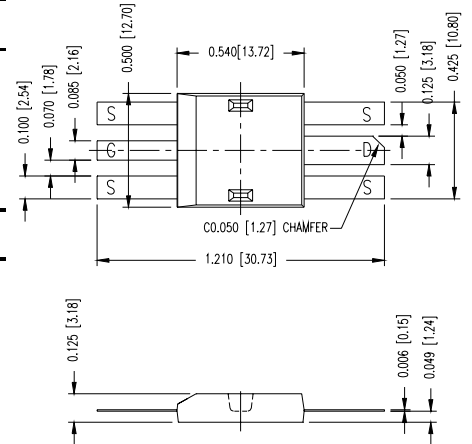
Features

- Isolated Substrate
 - high isolation voltage (>2500V)
 - excellent thermal transfer
 - Increased temperature and power cycling capability
- IXYS advanced low Q_g process
- Low gate charge and capacitances
 - easier to drive
 - faster switching
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

Advantages

- Optimized for RF and high speed switching at frequencies to >100MHz
- Easy to mount—no insulators needed
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$ unless otherwise specified)		
		min.	typ.	max.
R_G				5 Ω
C_{iss}			700	pF
C_{oss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 0.8 V_{DSS(max)}$, $f = 1\text{ MHz}$		150	pF
C_{rss}			20	pF
C_{stray}	Back Metal to any Pin		16	pF
$T_{d(on)}$			4	ns
T_{on}	$V_{GS} = 15\text{ V}$, $V_{DS} = 0.8 V_{DSS}$ $I_D = 0.5 I_{DM}$		4	ns
$T_{d(off)}$	$R_G = 0.2\ \Omega$ (External)		4	ns
T_{off}			4	ns
$Q_{g(on)}$		16		39 nC
Q_{gs}	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.5 V_{DSS}$ $I_D = 0.5 I_{D25}$	3.0		5.7 nC
Q_{gd}		8.0		20 nC



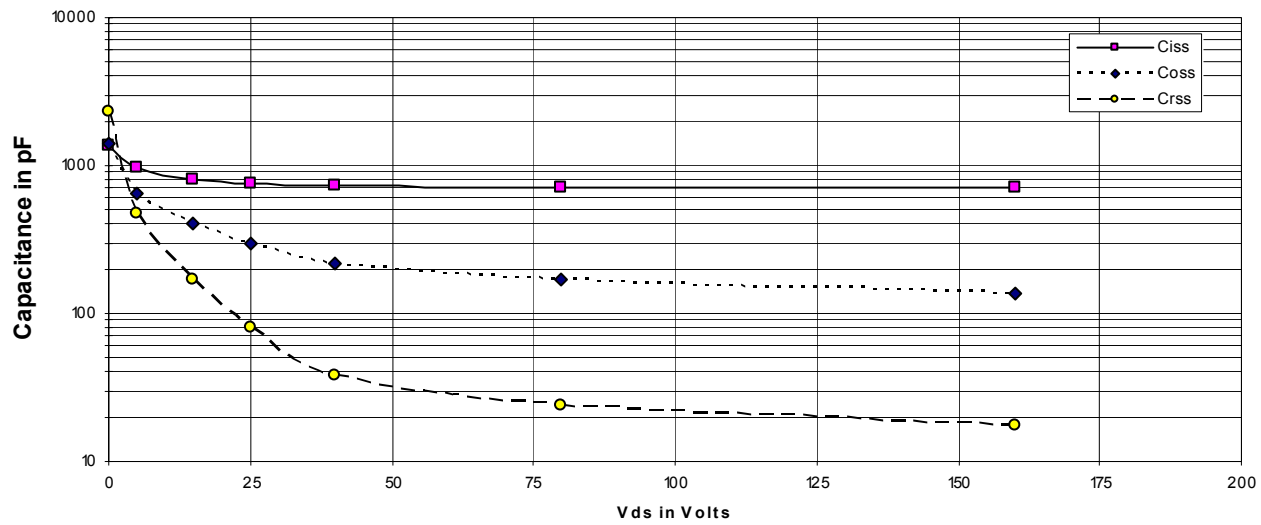
Source-Drain Diode		Characteristic Values ($T_J = 25^\circ\text{C}$ unless otherwise specified)		
Symbol	Test Conditions	min.	typ.	max.
I_S	$V_{GS} = 0\text{ V}$			9.0 A
I_{SM}	Repetitive; pulse width limited by T_{JM}			90 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$			1.4 V
T_{rr}			450	ns

For detailed device mounting and installation instructions, see the “*DE-Series MOSFET Mounting Instructions*” technical note on IXYS RF’s web site at www.ixysrf.com/Technical_Support/App_notes.html

IXYS RF reserves the right to change limits, test conditions and dimensions.

IXYS RF MOSFETS are covered by one or more of the following U.S. patents:

4,835,592	4,850,072	4,881,106	4,891,686	4,931,844	5,017,508
5,034,796	5,049,961	5,063,307	5,187,117	5,237,481	5,486,715
5,381,025	5,640,045				



Capacitances vs Vds

201N09A DE-SERIES SPICE Model

The DE-SERIES SPICE Model is illustrated in Figure 1. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms L_G , L_S and L_D . R_d is the $R_{DS(ON)}$ of the device, R_{ds} is the resistive leakage term. The output capacitance, C_{OSS} , and reverse transfer capacitance, C_{RSS} are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via R_{on} and R_{off} .

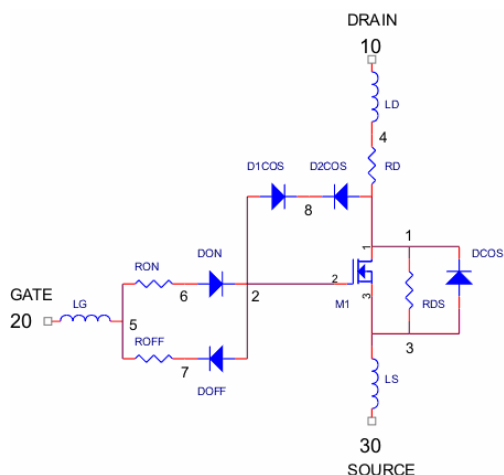


Figure 1 DE-SERIES SPICE Model

This SPICE model may be downloaded as a text file from the DEI web site at www.directedenergy.com/spice.htm

Net List:

*SYM=POWMOSN

.SUBCKT 201N09 10 20 30

* TERMINALS: D G S

* 200 Volt 9 Amp .2 ohm N-Channel Power MOSFET 10-30-2001

M1 1 2 3 3 DMOS L=1U W=1U

RON 5 6 1.5

DON 6 2 D1

ROF 5 7 .2

DOF 2 7 D1

D1CRS 2 8 D2

D2CRS 1 8 D2

CGS 2 3 .6N

RD 4 1 .2

DCOS 3 1 D3

RDS 1 3 5.0MEG

LS 3 30 .1N

LD 10 4 1N

LG 20 5 1N

.MODEL DMOS NMOS (LEVEL=3 VTO=3.0 KP=2.7)

.MODEL D1 D (IS=.5F CJO=1P BV=100 M=.5 VJ=.6 TT=1N)

.MODEL D2 D (IS=.5F CJO=1100P BV=500 M=.5 VJ=.6 TT=1N RS=10M)

.MODEL D3 D (IS=.5F CJO=300P BV=500 M=.3 VJ=.4 TT=400N RS=10M)

.ENDS

Doc #9200-0241 Rev 3
 © 2003 IXYS RF