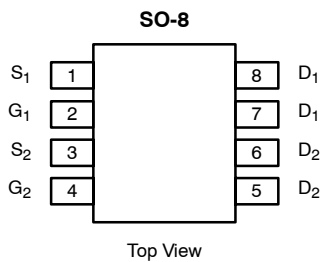


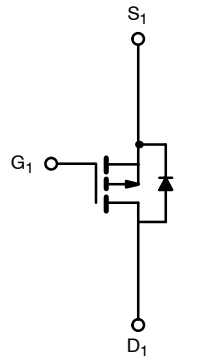


Dual P-Channel 2.5-V (G-S) MOSFET

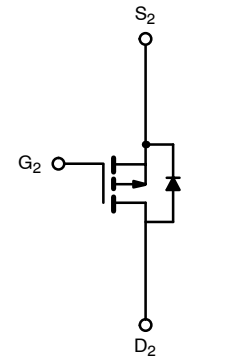
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.06 @ $V_{GS} = -4.5$ V	-4.7
	0.10 @ $V_{GS} = -2.5$ V	-3.7



Ordering Information: Si9933BDY—E3 (Lead Free)
Si9933BDY-T1—E3 (Lead Free with Tape and Reel)



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	10 secs	Steady State
Drain-Source Voltage		V_{DS}	-20	
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	-4.7	-3.6
	$T_A = 70^\circ\text{C}$		-3.8	-2.8
Pulsed Drain Current		I_{DM}	-20	
continuous Source Current (Diode Conduction) ^a		I_S	-1.7	-0.9
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.0	1.1
	$T_A = 70^\circ\text{C}$		1.3	0.7
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	55	62.5	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	33	40	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

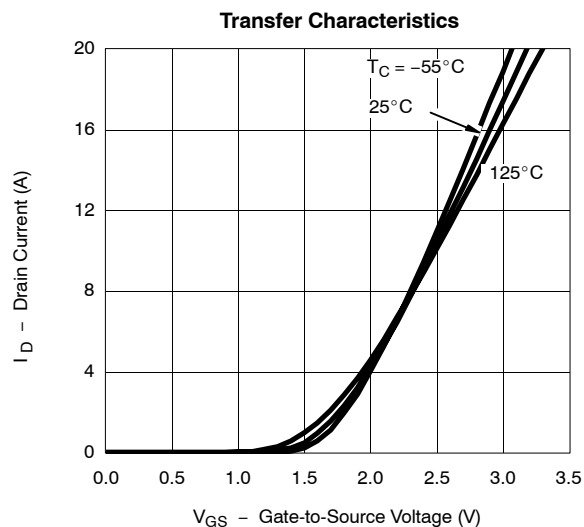
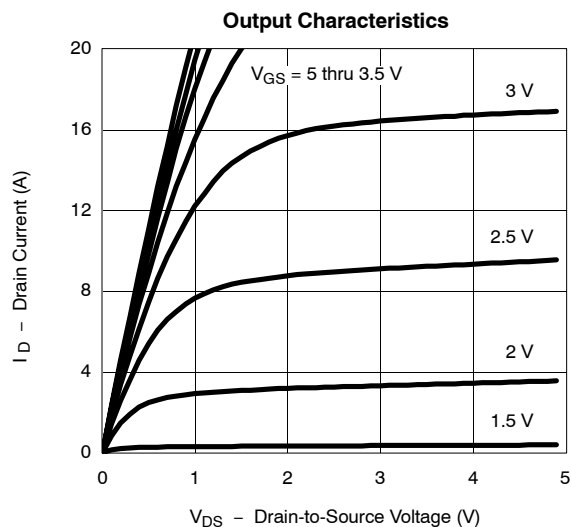
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

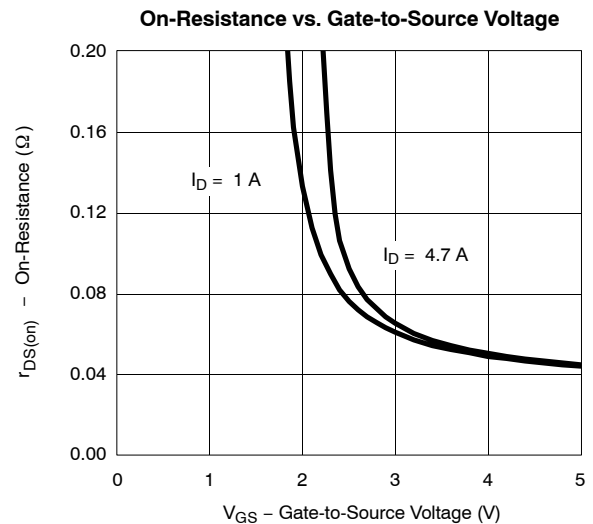
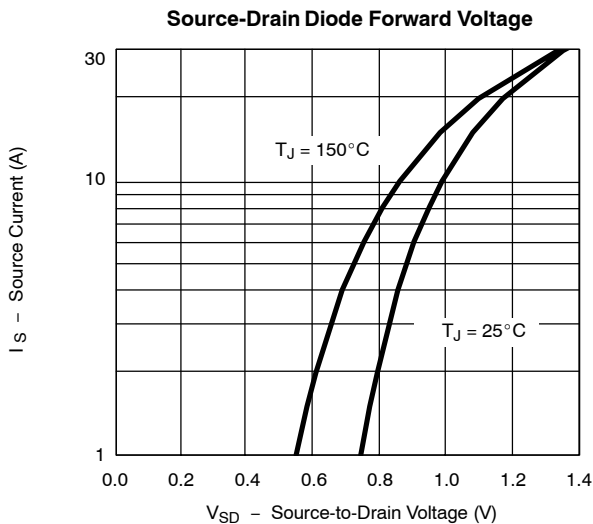
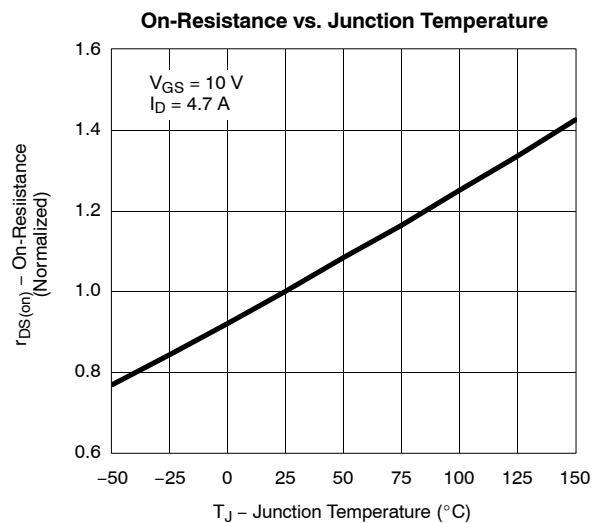
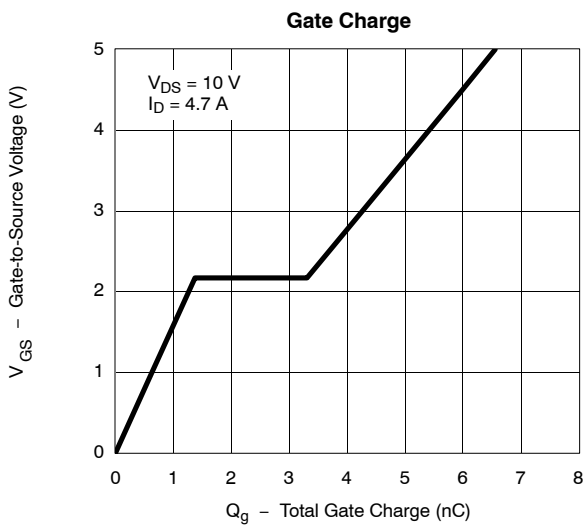
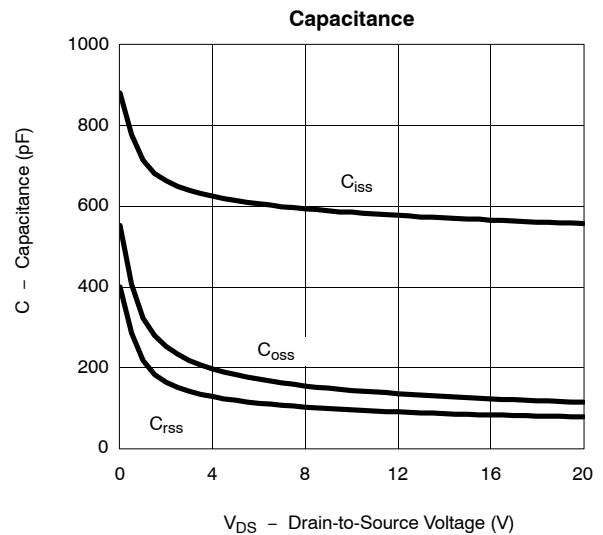
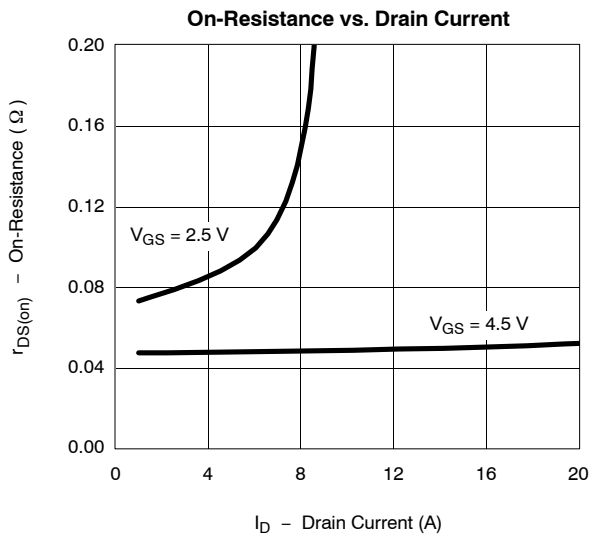
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-0.6		-1.4	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}$, $V_{GS} = -4.5\ \text{V}$	-20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}$, $I_D = -4.7\ \text{A}$		0.048	0.06	Ω
		$V_{GS} = -2.5\ \text{V}$, $I_D = -1\ \text{A}$		0.08	0.10	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}$, $I_D = -4.7\ \text{A}$		11		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.7\ \text{A}$, $V_{GS} = 0\ \text{V}$		-0.75	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}$, $V_{GS} = -4.5\ \text{V}$, $I_D = -4.7\ \text{A}$		6	9	nC
Gate-Source Charge	Q_{gs}			1.4		
Gate-Drain Charge	Q_{gd}			1.9		
Gate Resistance	R_g	$f = 1\ \text{MHz}$		9.5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}$, $V_{GEN} = -4.5\ \text{V}$, $R_g = 6\ \Omega$		22	35	ns
Rise Time	t_r			35	55	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Fall Time	t_f			25	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		25	50	

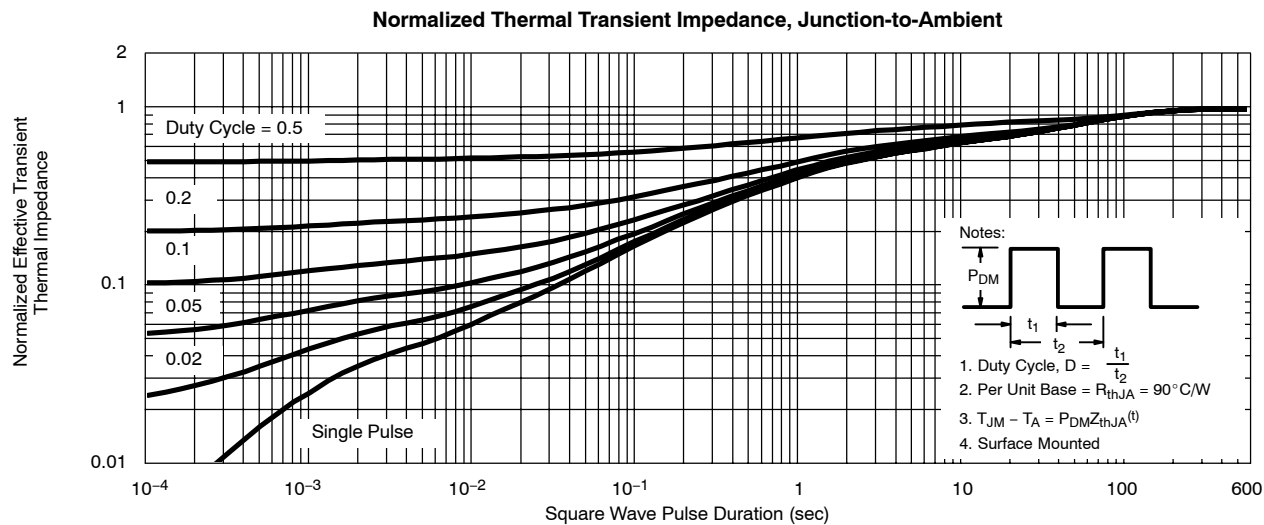
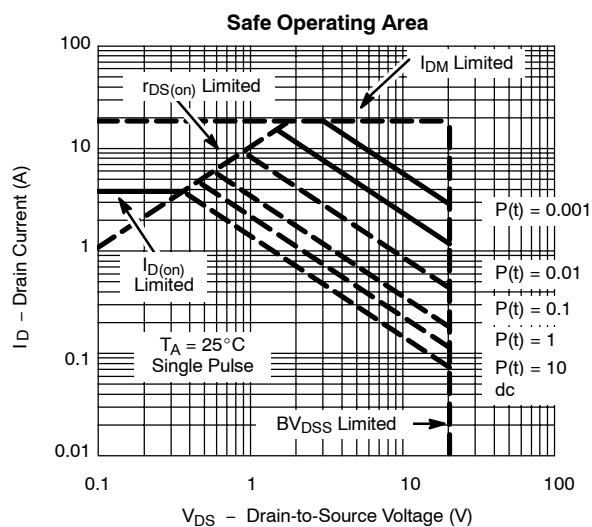
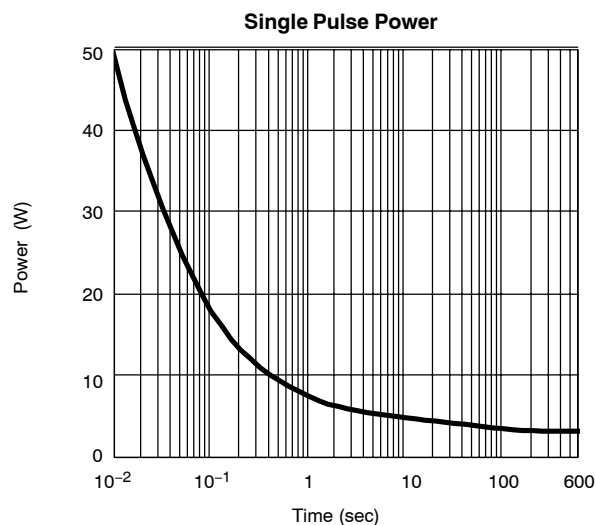
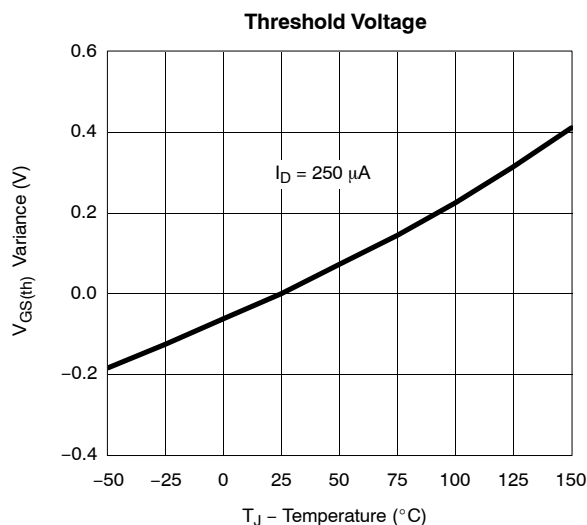
Notes

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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