



# W26L010A

## 64K × 16 HIGH-SPEED CMOS STATIC RAM

### GENERAL DESCRIPTION

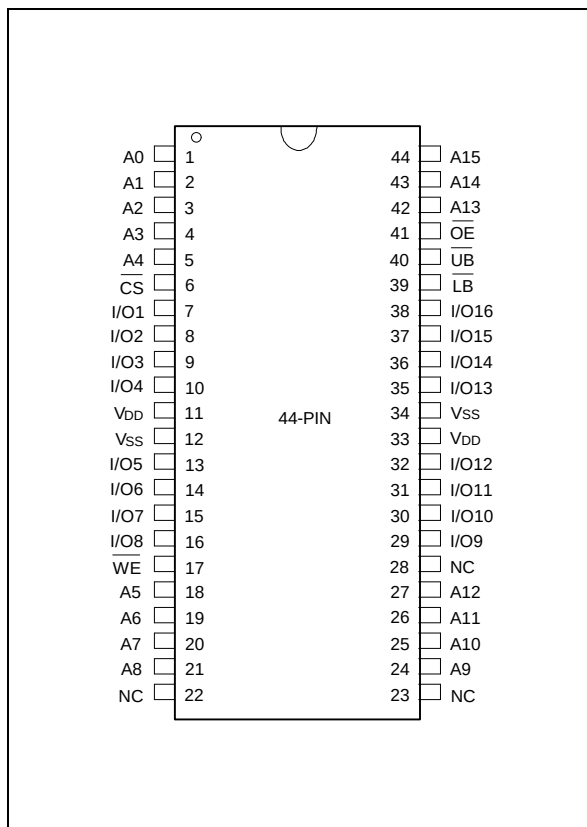
The W26L010A is a high-speed, low-power CMOS static RAM organized as 65,536 × 16 bits that operates on a single 3.3-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

The W26L010A has an active low chip select, separate upper and lower byte selects, and a fast output enable. No clock or refreshing is required. Separate byte select controls ( $\overline{\text{LB}}$  and  $\overline{\text{UB}}$ ) allow individual bytes to be written and read.  $\overline{\text{LB}}$  controls I/O1–I/O8, the lower byte.  $\overline{\text{UB}}$  controls I/O9–I/O16, the upper byte. This device is well suited for use in high-density, high-speed system applications.

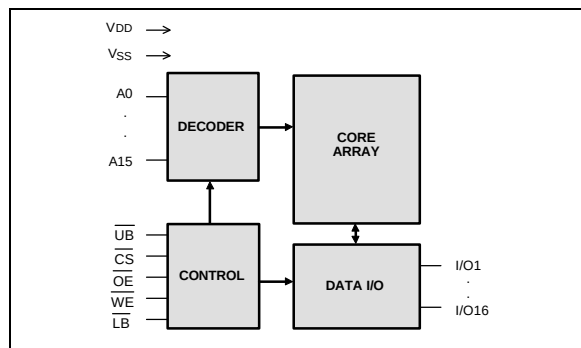
### FEATURES

- High speed access time: 10/12 nS (max.)
- Low power consumption:
  - Active: 530 mW (max.)
- Single +3.3V power supply
- Fully static operation
  - No clock or refreshing
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Data byte control
  - $\overline{\text{LB}}$  (I/O1–I/O8),  $\overline{\text{UB}}$  (I/O9–I/O16)
- Available packages: 44-pin 400 mil SOJ and 44-pin TSOP(II)

### PIN CONFIGURATION



### BLOCK DIAGRAM



### PIN DESCRIPTION

| SYMBOL                 | DESCRIPTION                  |
|------------------------|------------------------------|
| A0–A15                 | Address Inputs               |
| I/O1–I/O16             | Data Inputs/Outputs          |
| $\overline{\text{CS}}$ | Chip Select Inputs           |
| $\overline{\text{WE}}$ | Write Enable Input           |
| $\overline{\text{OE}}$ | Output Enable Input          |
| $\overline{\text{LB}}$ | Lower Byte Select I/O1–I/O8  |
| $\overline{\text{UB}}$ | Upper Byte Select I/O9–I/O16 |
| VDD                    | Power Supply                 |
| VSS                    | Ground                       |
| NC                     | No Connection                |

**TRUTH TABLE**

| $\overline{\text{CS}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{LB}}$ | $\overline{\text{UB}}$ | MODE             | I/O1- I/O8 | I/O9- I/O16 | V <sub>DD</sub><br>CURRENT         |
|------------------------|------------------------|------------------------|------------------------|------------------------|------------------|------------|-------------|------------------------------------|
| H                      | X                      | X                      | X                      | X                      | Not Selected     | High Z     | High Z      | I <sub>SB</sub> , I <sub>SB1</sub> |
| L                      | H                      | H                      | X                      | X                      | Output Disable   | High Z     | High Z      | I <sub>DD</sub>                    |
| L                      | L                      | H                      | L                      | L                      | 2 Bytes Read     | DOUT       | DOUT        | I <sub>DD</sub>                    |
| L                      | L                      | H                      | L                      | H                      | Lower Byte Read  | DOUT       | High Z      | I <sub>DD</sub>                    |
| L                      | L                      | H                      | H                      | L                      | Upper Byte Read  | High Z     | DOUT        | I <sub>DD</sub>                    |
| L                      | X                      | L                      | L                      | L                      | 2 Bytes Write    | DIN        | DIN         | I <sub>DD</sub>                    |
| L                      | X                      | L                      | L                      | H                      | Lower Byte Write | DIN        | High Z      | I <sub>DD</sub>                    |
| L                      | X                      | L                      | H                      | L                      | Upper Byte Write | High Z     | DIN         | I <sub>DD</sub>                    |
| L                      | X                      | X                      | H                      | H                      | Output Disable   | High Z     | High Z      | I <sub>DD</sub>                    |

**DC CHARACTERISTICS****Absolute Maximum Ratings**

| PARAMETER                                   | RATING                       | UNIT |
|---------------------------------------------|------------------------------|------|
| Supply Voltage to V <sub>SS</sub> Potential | -0.5 to +4.6                 | V    |
| Input/Output to V <sub>SS</sub> Potential   | -0.5 to V <sub>DD</sub> +0.5 | V    |
| Allowable Power Dissipation                 | 1.5                          | W    |
| Storage Temperature                         | -65 to +150                  | °C   |
| Operating Temperature                       | 0 to +70                     | °C   |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## Operating Characteristics

(V<sub>DD</sub> = 3.3V ±5%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C)

| PARAMETER              | SYM.             | TEST CONDITIONS                                                                                    |    | MIN. | TYP. | MAX.                    | UNIT |
|------------------------|------------------|----------------------------------------------------------------------------------------------------|----|------|------|-------------------------|------|
| Input Low Voltage      | V <sub>IL</sub>  | -                                                                                                  |    | -0.5 | -    | +0.8                    | V    |
| Input High Voltage     | V <sub>IH</sub>  | -                                                                                                  |    | +2.0 | -    | V <sub>DD</sub><br>+0.3 | V    |
| Input Leakage Current  | I <sub>LI</sub>  | V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>                                               |    | -10  | -    | +10                     | μA   |
| Output Leakage Current | I <sub>LO</sub>  | V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>DD</sub><br>Output Pins in High Z,<br>See Truth Table |    | -10  | -    | +10                     | μA   |
| Output Low Voltage     | V <sub>OL</sub>  | I <sub>OL</sub> = +8.0 mA                                                                          |    | -    | -    | 0.4                     | V    |
| Output High Voltage    | V <sub>OH</sub>  | I <sub>OH</sub> = -4.0 mA                                                                          |    | 2.4  | -    | -                       | V    |
| Operating Power        | I <sub>DD</sub>  | $\overline{CS}$ = V <sub>IL</sub> (max.), Cycle = min.                                             | 10 | -    | -    | 160                     | mA   |
| Supply Current         |                  | I/O = open, Duty = 100%                                                                            | 12 | -    | -    | 140                     |      |
| Standby Power          | I <sub>SB</sub>  | $\overline{CS}$ = V <sub>IH</sub> (min.), Cycle = min.                                             |    | -    | -    | 30                      | mA   |
| Supply Current         | I <sub>SB1</sub> | $\overline{CS}$ = V <sub>DD</sub> -0.2V, I/O = open<br>All other pins = V <sub>DD</sub> -0.2V/GND  |    | -    | -    | 10                      | mA   |

Note: Typical characteristics are evaluated at V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 25° C.

## CAPACITANCE

(V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 25° C, f = 1 MHz)

| PARAMETER                | SYM.             | CONDITIONS            | MAX. | UNIT |
|--------------------------|------------------|-----------------------|------|------|
| Input Capacitance        | C <sub>IN</sub>  | V <sub>IN</sub> = 0V  | 6    | pF   |
| Input/Output Capacitance | C <sub>I/O</sub> | V <sub>OUT</sub> = 0V | 8    | pF   |

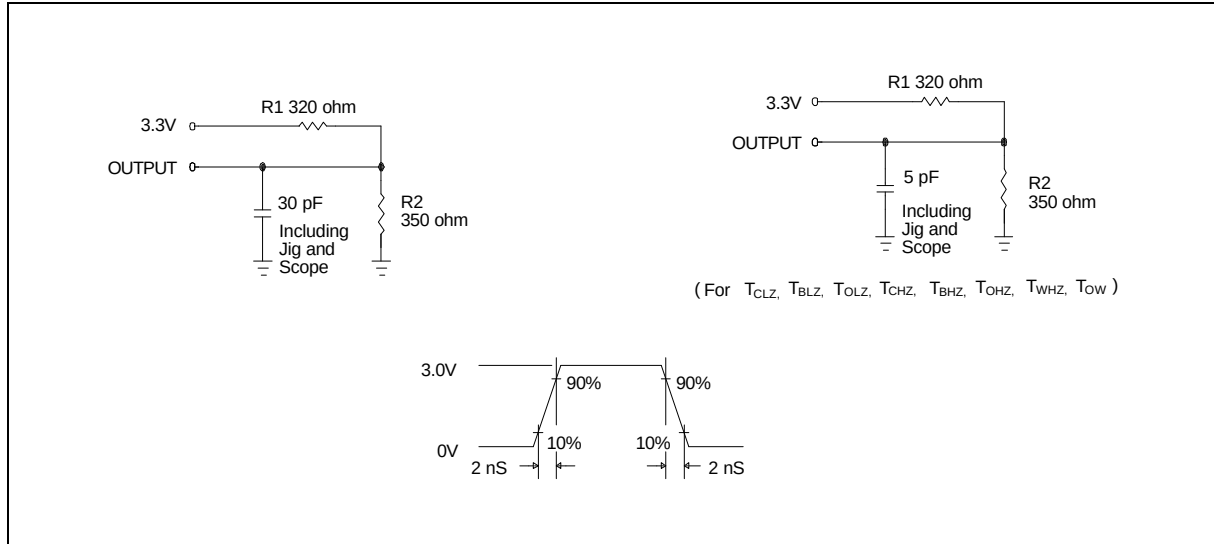
Note: These parameters are sampled but not 100% tested.

## AC CHARACTERISTICS

### AC Test Conditions

| PARAMETER                               | CONDITIONS                                                            |
|-----------------------------------------|-----------------------------------------------------------------------|
| Input Pulse Levels                      | 0V to 3V                                                              |
| Input Rise and Fall Times               | 2 nS                                                                  |
| Input and Output Timing Reference Level | 1.5V                                                                  |
| Output Load                             | C <sub>L</sub> = 30 pF, I <sub>OH</sub> /I <sub>OL</sub> = -4 mA/8 mA |

## AC Test Loads and Waveform



( $V_{DD} = 3.3V \pm 5\%$ ,  $V_{SS} = 0V$ ,  $T_A = 0$  to  $70^\circ C$ )

### (1) Read Cycle

| PARAMETER                                                      | SYM.        | W26L010A-10 |      | W26L010A-12 |      | UNIT |
|----------------------------------------------------------------|-------------|-------------|------|-------------|------|------|
|                                                                |             | MIN.        | MAX. | MIN.        | MAX. |      |
| Read Cycle Time                                                | $T_{RC}$    | 10          | -    | 12          | -    | nS   |
| Address Access Time                                            | $T_{AA}$    | -           | 10   | -           | 12   | nS   |
| Chip Select Access Time                                        | $T_{ACS}$   | -           | 10   | -           | 12   | nS   |
| Output Enable to Output Valid                                  | $T_{OE}$    | -           | 5    | -           | 6    | nS   |
| $\overline{UB}$ , $\overline{LB}$ Access Time                  | $T_{BA}$    | -           | 5    | -           | 6    | nS   |
| Output Hold from Address Change                                | $T_{OH}$    | 3           | -    | 3           | -    | nS   |
| Chip Select to Output in Low Z                                 | $T_{CLZ}^*$ | 3           | -    | 3           | -    | nS   |
| Chip Deselect to Output in High Z                              | $T_{CHZ}^*$ | -           | 5    | -           | 6    | nS   |
| Output Enable to Output in Low Z                               | $T_{OLZ}^*$ | 0           | -    | 0           | -    | nS   |
| Output Disable to Output in High Z                             | $T_{OHZ}^*$ | -           | 5    | -           | 6    | nS   |
| $\overline{UB}$ , $\overline{LB}$ Select to Output in Low Z    | $T_{BLZ}^*$ | 0           | -    | 0           | -    | nS   |
| $\overline{UB}$ , $\overline{LB}$ Deselect to Output in High Z | $T_{BHZ}^*$ | -           | 5    | -           | 6    | nS   |

\* These parameters are sampled but not 100% tested.



AC Characteristics, continued

## (2) Write Cycle

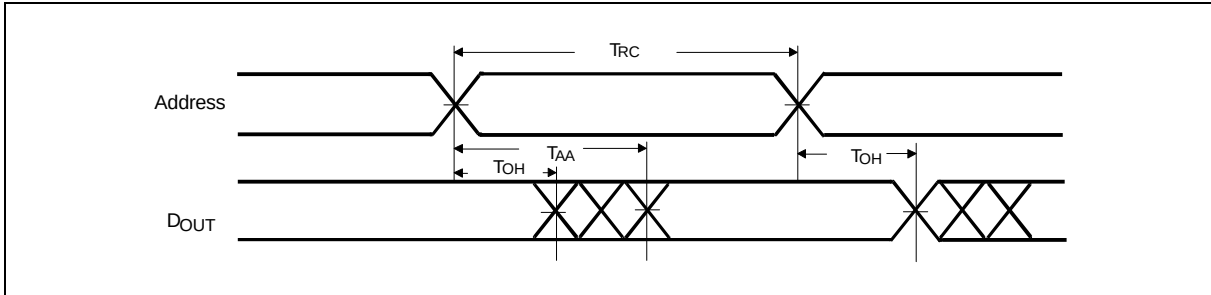
| PARAMETER                                                              | SYM.                                            | W26L010A-10 |      | W26L010A-12 |      | UNIT |
|------------------------------------------------------------------------|-------------------------------------------------|-------------|------|-------------|------|------|
|                                                                        |                                                 | MIN.        | MAX. | MIN.        | MAX. |      |
| Write Cycle Time                                                       | TWC                                             | 10          | –    | 12          | –    | nS   |
| Chip Select to End of Write                                            | TCW                                             | 9           | –    | 10          | –    | nS   |
| Address Valid to End of Write                                          | TAW                                             | 9           | –    | 10          | –    | nS   |
| Address Setup Time                                                     | TAS                                             | 0           | –    | 0           | –    | nS   |
| $\overline{\text{UB}}$ , $\overline{\text{LB}}$ Select to End of Write | TBW                                             | 9           | –    | 10          | –    | nS   |
| Write Pulse Width                                                      | TWP                                             | 9           | –    | 10          | –    | nS   |
| Write Recovery Time                                                    | $\overline{\text{CS}}$ , $\overline{\text{WE}}$ | 0           | –    | 0           | –    | nS   |
| Data Valid to End of Write                                             | TDW                                             | 6           | –    | 7           | –    | nS   |
| Data Hold from End of Write                                            | TDH                                             | 0           | –    | 0           | –    | nS   |
| Write to Output in High Z                                              | TWHZ*                                           | –           | 6    | –           | 7    | nS   |
| End of Write to Output Active                                          | TOW*                                            | 3           | –    | 3           | –    | nS   |

\* These parameters are sampled but not 100% tested.

## Timing Waveforms

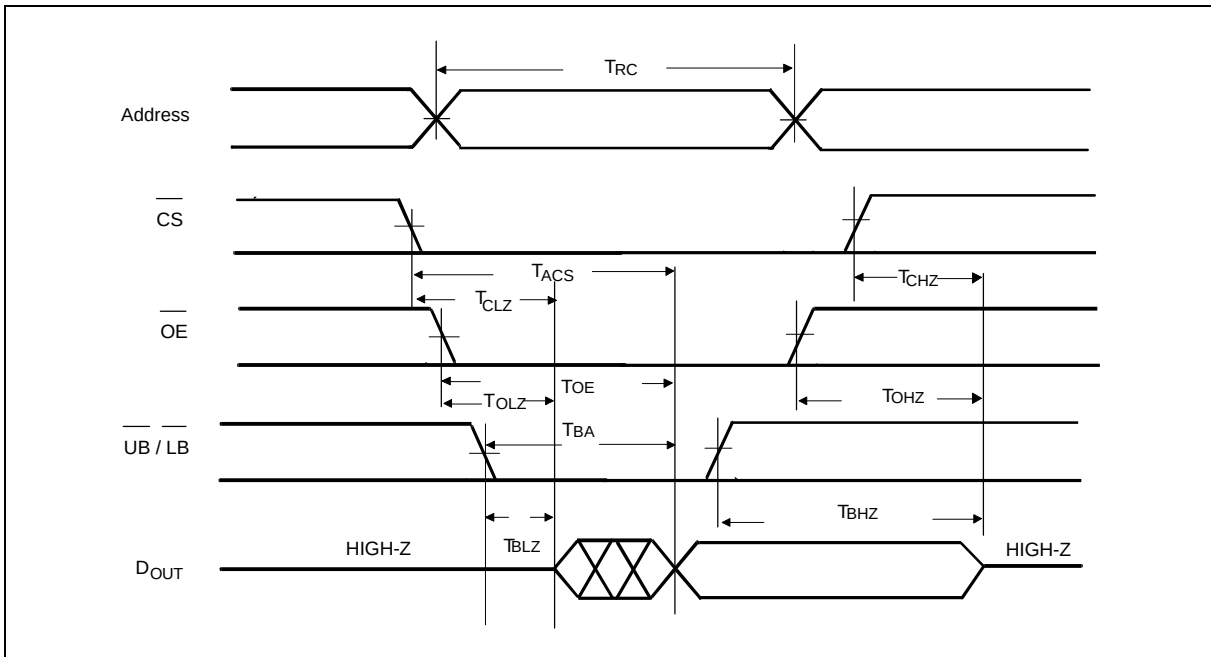
### Read Cycle 1

(Address Controlled,  $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )



### Read Cycle 2

(Chip Select Controlled,  $\overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )



Notes:

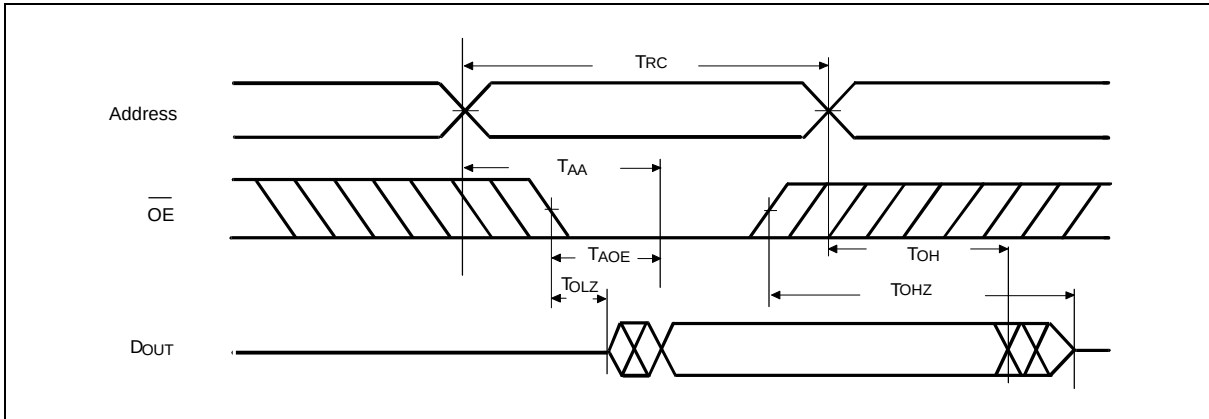
1.  $\overline{WE}$  is high for read cycle.
2. Device is continuously selected.  
 $\overline{CS} = \overline{OE} = \overline{LB} = \text{Low}$   
 $\overline{CS} = \overline{OE} = \overline{LB} = \text{Low}$
3. Address valid prior to or coincident with  $\overline{CS}$  transition low.



Timing Waveforms, continued

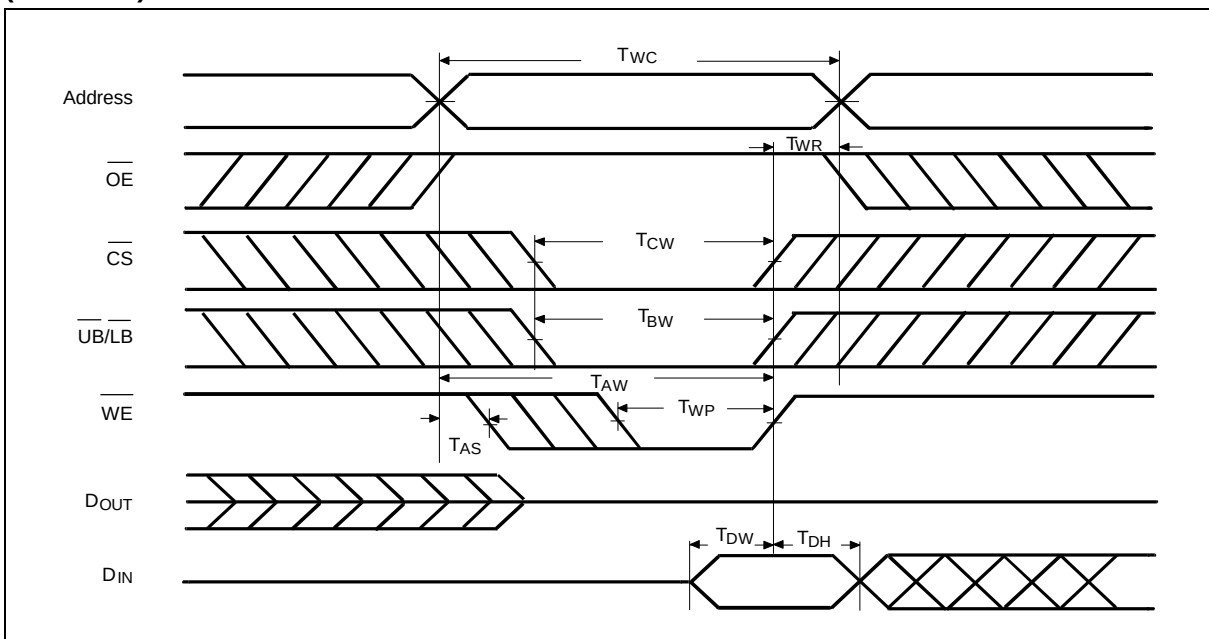
## Read Cycle 3

(Output Enable Controlled,  $\overline{CS} = \overline{UB} = \overline{LB} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )



## Write Cycle 1

(OE Clock)

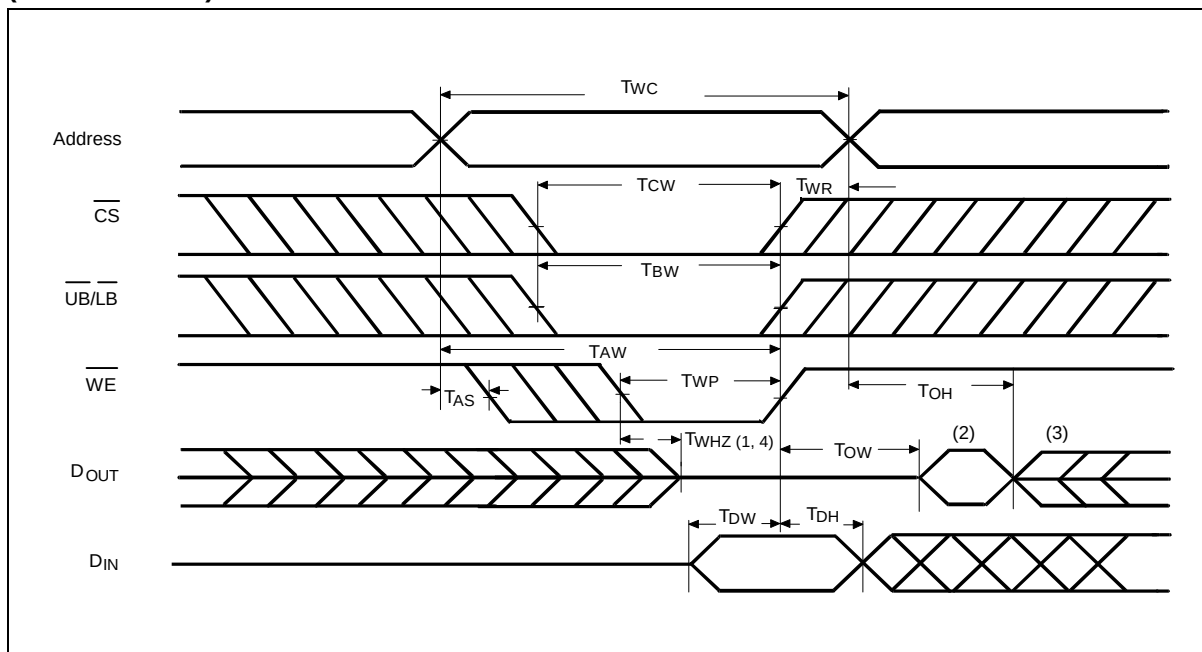




Timing Waveforms, continued

## Write Cycle 2

(OE = V<sub>IL</sub> Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured  $\pm 500$  mV from steady state with  $C_L = 5$  pF. This parameter is guaranteed but not 100% tested.

## ORDERING INFORMATION

| PART NO.     | ACCESS TIME (nS) | OPERATING CURRENT MAX. (mA) | STANDBY CURRENT MAX. (mA) | PACKAGE            |
|--------------|------------------|-----------------------------|---------------------------|--------------------|
| W26L010AJ-10 | 10               | 160                         | 10                        | 44-pin 400 mil SOJ |
| W26L010AJ-12 | 12               | 140                         | 10                        | 44-pin 400 mil SOJ |
| W26L010AT-10 | 10               | 160                         | 10                        | 44-pin TSOP        |
| W26L010AT-12 | 12               | 140                         | 10                        | 44-pin TSOP        |

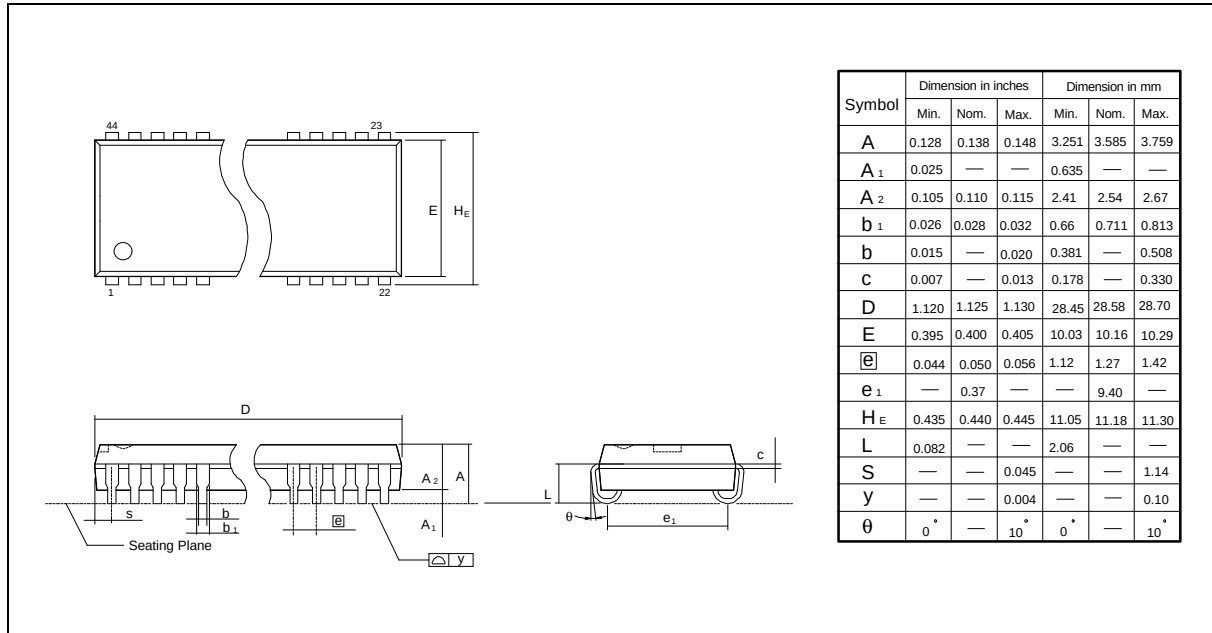
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

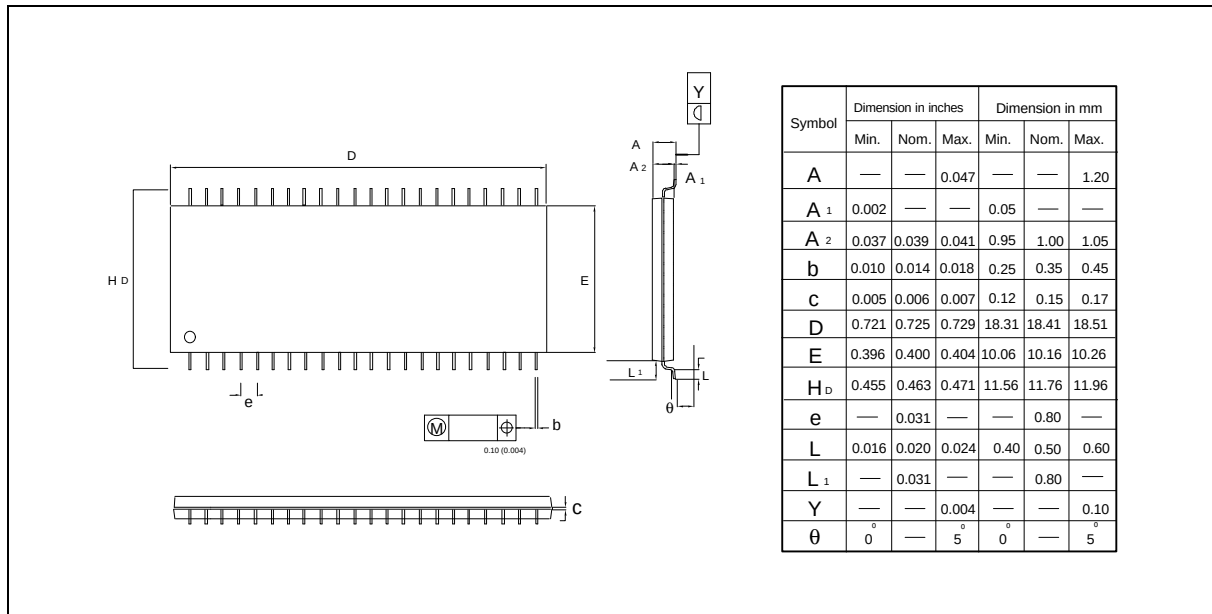


## PACKAGE DIMENSIONS

### 44-pin Small Outline J Band



### 44-pin Standard Type Two TSOP





## VERSION HISTORY

| VERSION | DATE      | PAGE          | DESCRIPTION                                                 |
|---------|-----------|---------------|-------------------------------------------------------------|
| A1      | May 1995  |               | Initial Issued                                              |
| A2      | Feb. 1998 | 1, 3, 4, 5, 8 | Change the relative specification from 15/20 nS to 10/12 nS |
|         |           | 1, 8, 9       | Add TSOP package                                            |
|         |           | 6, 7          | Modify timing waveforms                                     |
| A3      | Jul. 1998 | 3, 4          | Revise Vcc from 3.3V $\pm 10\%$ to 3.3V $\pm 5\%$           |



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Note: All data and specifications are subject to change without notice.