

MOSFET - P-Channel, TSOP-6 –3.5 A, –30 V

NTGS3455T1

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature TSOP-6 Surface Mount Package
- Pb-Free Package is Available

Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

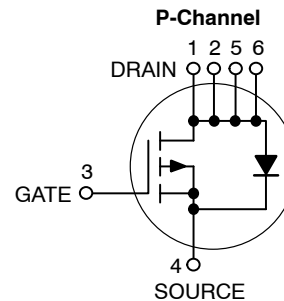
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	–30	Volts
Gate-to-Source Voltage – Continuous	V_{GS}	± 20.0	Volts
Thermal Resistance Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_d	2.0	Watts
Drain Current	I_D	–3.5	Amps
– Continuous @ $T_A = 25^\circ\text{C}$	I_{DM}	–20	Amps
– Pulsed Drain Current ($T_p < 10 \mu\text{s}$)	P_d	1.0	Watts
Maximum Operating Power Dissipation	I_D	–2.5	Amps
Maximum Operating Drain Current			
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	128	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_d	1.0	Watts
Drain Current	I_D	–2.5	Amps
– Continuous @ $T_A = 25^\circ\text{C}$	I_{DM}	–14	Amps
– Pulsed Drain Current ($T_p < 10 \mu\text{s}$)	P_d	0.5	Watts
Maximum Operating Power Dissipation	I_D	–1.75	Amps
Maximum Operating Drain Current			
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes for 10 Seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted onto a 2" square FR-4 board (1 in sq, 2 oz. Cu. 0.06" thick single sided), $t < 5.0$ seconds.
2. Mounted onto a 2" square FR-4 board (1 in sq, 2 oz. Cu. 0.06" thick single sided), operating to steady state.

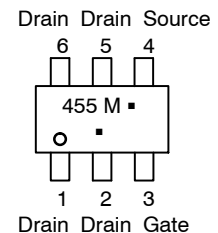
$V_{(BR)DS}$	$R_{DS(on)}$ TYP	I_D Max
–30 V	100 m Ω @ –10 V	–3.5 A



MARKING DIAGRAM & PIN ASSIGNMENT



TSOP-6
CASE 318G
STYLE 1



455 = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
NTGS3455T1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

DISCONTINUED (Note 1)

NTGS3455T1	TSOP-6	3000 / Tape & Reel
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your onsemi representative for information. The most current information on this device may be available on www.onsemi.com.

NTGS3455T1

ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted) (Notes 3 & 4)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = -10\text{ }\mu\text{A}$)	$V_{(BR)DSS}$	-30	-	-	Vdc
Zero Gate Voltage Drain Current ($V_{GS} = 0\text{ Vdc}$, $V_{DS} = -30\text{ Vdc}$, $T_J = 25\text{ }^{\circ}\text{C}$) ($V_{GS} = 0\text{ Vdc}$, $V_{DS} = -30\text{ Vdc}$, $T_J = 70\text{ }^{\circ}\text{C}$)	I_{DSS}	- -	- -	-1.0 -5.0	μAdc
Gate-Body Leakage Current ($V_{GS} = -20.0\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	-100	nAdc
Gate-Body Leakage Current ($V_{GS} = +20.0\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	-1.0	-1.87	-3.0	Vdc
Static Drain-Source On-State Resistance ($V_{GS} = -10\text{ Vdc}$, $I_D = -3.5\text{ Adc}$) ($V_{GS} = -4.5\text{ Vdc}$, $I_D = -2.7\text{ Adc}$)	$R_{DS(on)}$	- -	0.094 0.144	0.100 0.170	Ω
Forward Transconductance ($V_{DS} = -15\text{ Vdc}$, $I_D = -3.5\text{ Adc}$)	g_{FS}	-	6.0	-	mhos

DYNAMIC CHARACTERISTICS

Total Gate Charge	$(V_{DS} = -15\text{ Vdc}$, $V_{GS} = -10\text{ Vdc}$, $I_D = -3.5\text{ Adc})$	Q_{tot}	-	9.0	13	nC
Gate-Source Charge		Q_{gs}	-	2.5	-	
Gate-Drain Charge		Q_{gd}	-	2.0	-	
Input Capacitance	$(V_{DS} = -5.0\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $f = 1.0\text{ MHz})$	C_{iss}	-	480	-	pF
Output Capacitance		C_{oss}	-	220	-	
Reverse Transfer Capacitance		C_{rss}	-	60	-	

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$(V_{DD} = -20\text{ Vdc}$, $I_D = -1.0\text{ Adc}$, $V_{GS} = -10\text{ Vdc}$, $R_g = 6.0\text{ }\Omega$)	$t_{d(on)}$	-	10	20	ns
Rise Time		t_r	-	15	30	
Turn-Off Delay Time		$t_{d(off)}$	-	20	35	
Fall Time		t_f	-	10	20	
Reverse Recovery Time	$(I_S = -1.7\text{ Adc}$, $dI_S/dt = 100\text{ A}/\mu\text{s})$	t_{rr}	-	30	-	ns

BODY-DRAIN DIODE RATINGS

Diode Forward On-Voltage	$(I_S = -1.7\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$)	V_{SD}	-	-0.90	-1.2	Vdc
Diode Forward On-Voltage	$(I_S = -3.5\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$)	V_{SD}	-	-1.0	-	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.

4. Class 1 ESD rated – Handling precautions to protect against electrostatic discharge are mandatory.

NTGS3455T1

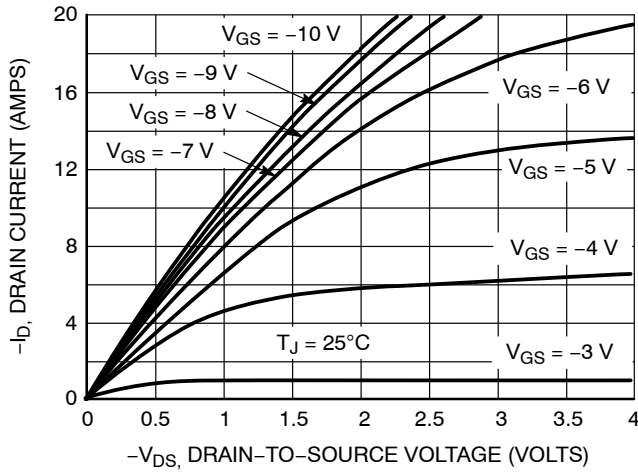


Figure 1. On-Region Characteristics

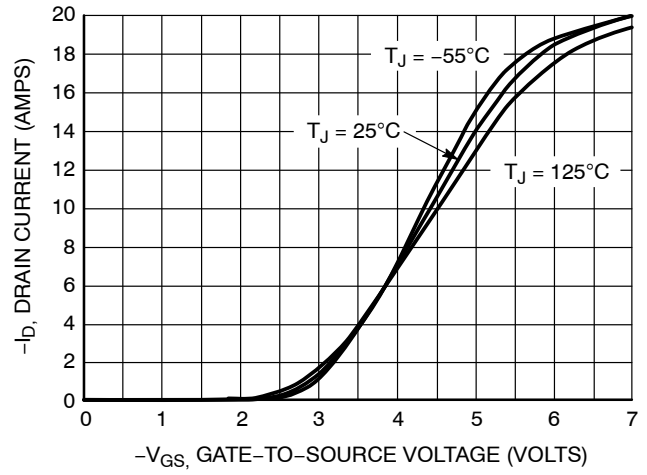


Figure 2. Transfer Characteristics

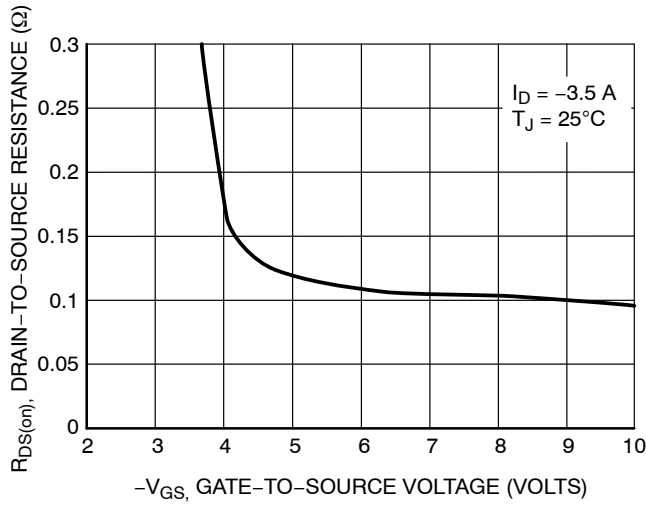


Figure 3. On-Resistance vs. Gate-to-Source Voltage

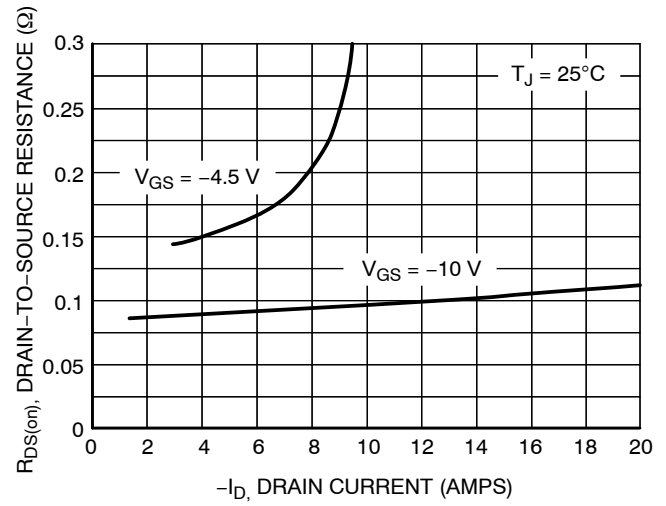


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

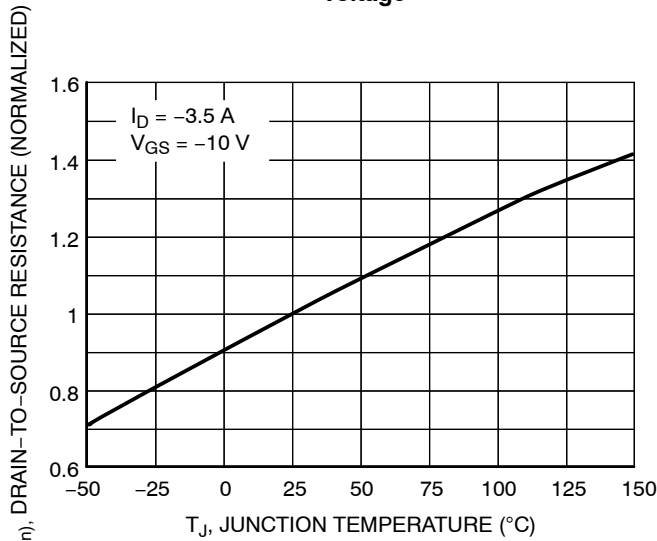


Figure 5. On-Resistance Variation with Temperature

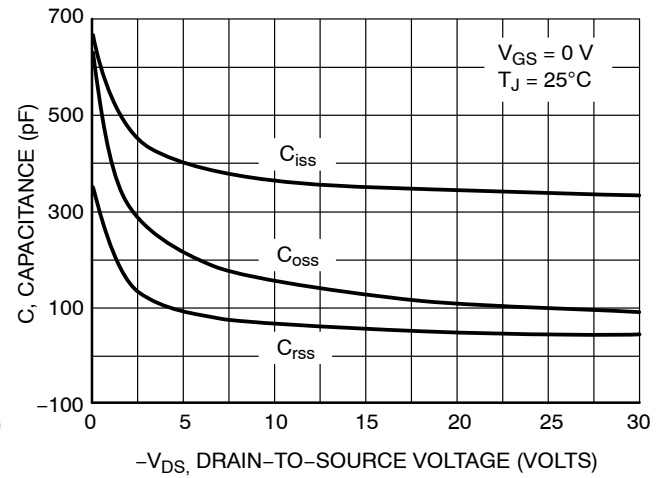


Figure 6. Capacitance Variation

NTGS3455T1

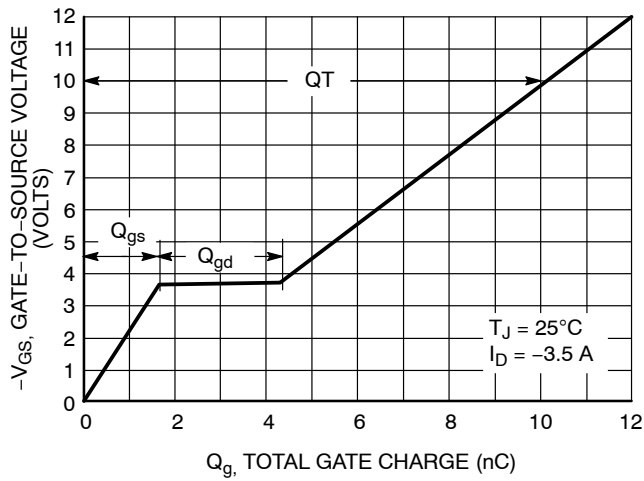


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

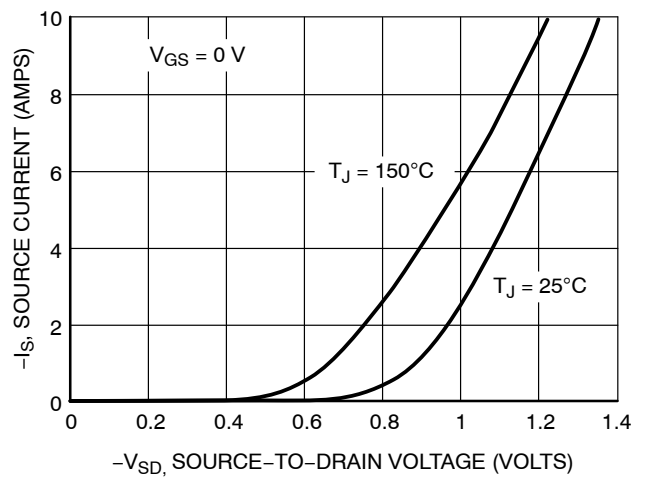


Figure 8. Diode Forward Voltage vs. Current

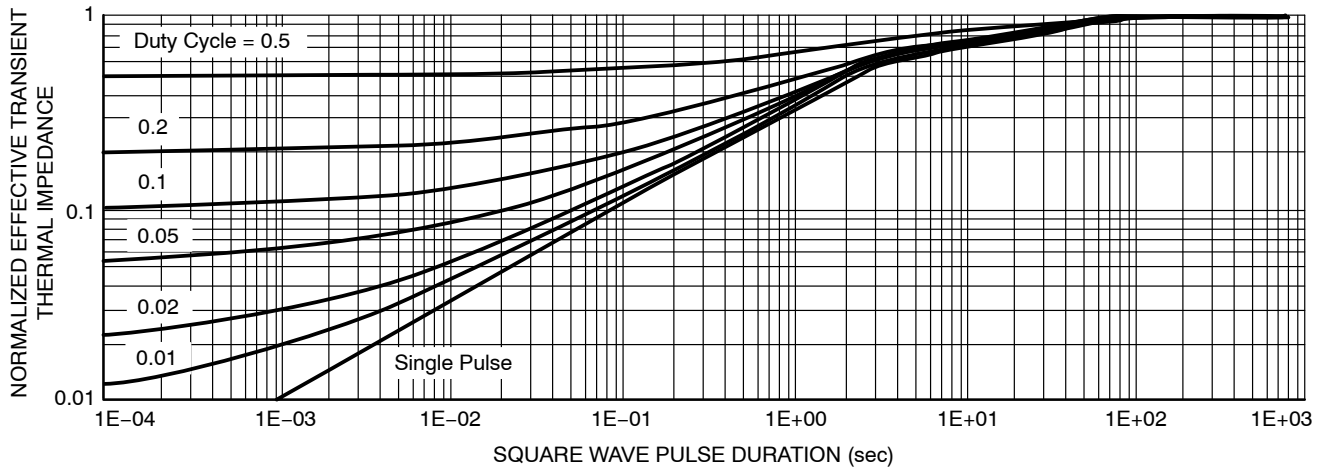


Figure 9. Normalized Thermal Transient Impedance, Junction-to-Ambient

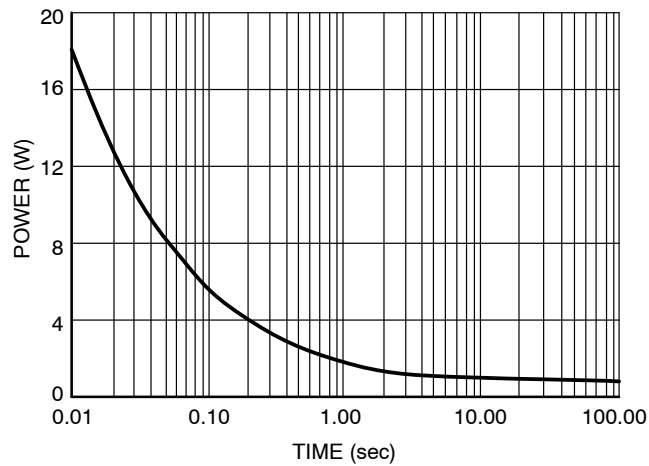
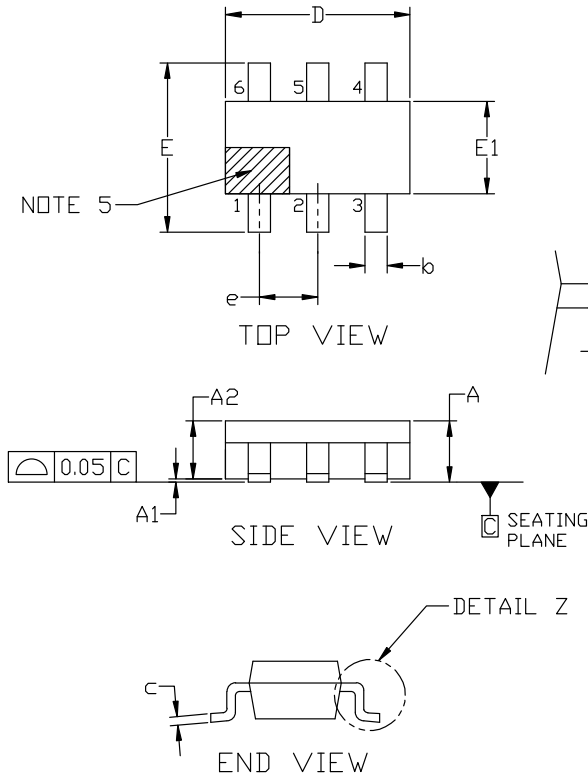


Figure 10. Single Pulse Power


TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

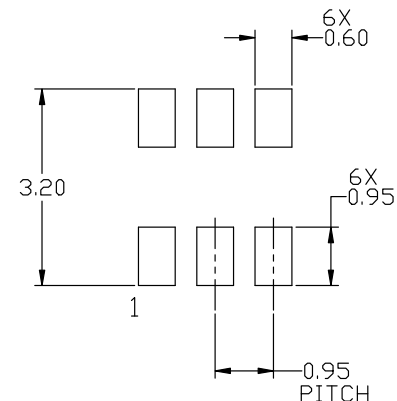


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS

DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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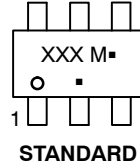
TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

GENERIC
MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
■ = Pb-Free Package

XXX = Specific Device Code
M = Date Code
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 2: PIN 1. EMITTER 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. BASE 2 6. COLLECTOR 2	STYLE 3: PIN 1. ENABLE 2. N/C 3. R BOOST 4. Vz 5. V in 6. V out	STYLE 4: PIN 1. N/C 2. V in 3. NOT USED 4. GROUND 5. ENABLE 6. LOAD	STYLE 5: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 6: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR
STYLE 7: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. N/C 5. COLLECTOR 6. EMITTER	STYLE 8: PIN 1. Vbus 2. D(in) 3. D(in)+ 4. D(out)+ 5. D(out) 6. GND	STYLE 9: PIN 1. LOW VOLTAGE GATE 2. DRAIN 3. SOURCE 4. DRAIN 5. DRAIN 6. HIGH VOLTAGE GATE	STYLE 10: PIN 1. D(OUT)+ 2. GND 3. D(OUT)- 4. D(IN)- 5. VBUS 6. D(IN)+	STYLE 11: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1/GATE 2	STYLE 12: PIN 1. I/O 2. GROUND 3. I/O 4. I/O 5. VCC 6. I/O
STYLE 13: PIN 1. GATE 1 2. SOURCE 2 3. GATE 2 4. DRAIN 2 5. SOURCE 1 6. DRAIN 1	STYLE 14: PIN 1. ANODE 2. SOURCE 3. GATE 4. CATHODE/DRAIN 5. CATHODE/DRAIN 6. CATHODE/DRAIN	STYLE 15: PIN 1. ANODE 2. SOURCE 3. GATE 4. DRAIN 5. N/C 6. CATHODE	STYLE 16: PIN 1. ANODE/CATHODE 2. BASE 3. EMITTER 4. COLLECTOR 5. ANODE 6. CATHODE	STYLE 17: PIN 1. EMITTER 2. BASE 3. ANODE/CATHODE 4. ANODE 5. CATHODE 6. COLLECTOR	

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