

LVCMOS/LVTTL CLOCK DIVIDER

ICS87001-01

General Description



The ICS87001-01 is a low skew, $\div 1$, $\div 2$ $\div 3$, $\div 4$ $\div 5$, $\div 6$ $\div 8$, $\div 16$ LVCMOS/LVTTL Fanout Buffer/Divider and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS87001-01 has selectable clock inputs that

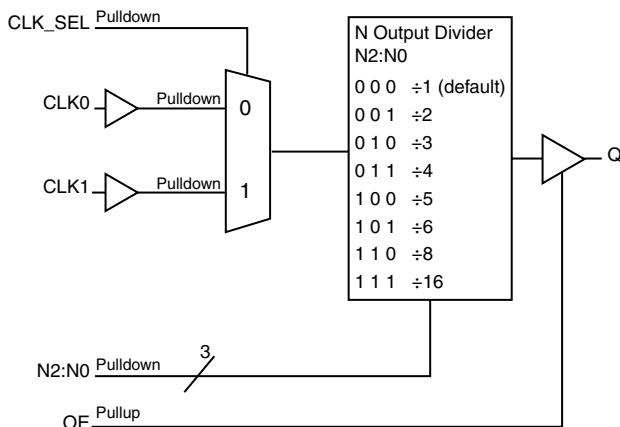
accept single ended input levels. Output enable pin controls whether the output is in the active or high impedance state.

The ICS87001-01 is characterized at 3.3V, 2.5V and mixed 3.3V/2.5V, 3.3V/1.8V, 2.5V/1.8V input/output supply operating modes. Guaranteed part-to-part skew characteristics make the ICS87001-01 ideal for those applications demanding well defined performance and repeatability.

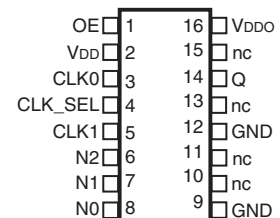
Features

- One LVCMOS / LVTTL output, 15 Ω output impedance
- Selectable LVCMOS / LVTTL clock inputs
- Maximum output frequency: 250MHz
- Part-to-part skew: TBD
- Power supply modes:
Core/Output
3.3V/3.3V
3.3V/2.5V
3.3V/1.8V
2.5V/2.5V
2.5V/1.8V
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS87001-01

16-Lead TSSOP

4.4mm x 3.0mm x 0.925mm

package body

G Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.
2	V _{DD}	Power		Power supply pin.
3, 5	CLK0, CLK1	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
4	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
6, 7, 8	N2, N1, N0	Input	Pulldown	N divider pins. LVCMOS/LVTTL interface levels. See Table 3.
9, 12	GND	Power		Power supply ground.
10, 11, 13, 15	nc	Unused		No connect.
14	Q	Output		Single-ended clock output. 15Ω output impedance. LVCMOS/LVTTL interface levels.
16	V _{DDO}	Power		Output supply pin.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
C _{PD}	Power Dissipation Capacitance			10		pF
R _{OUT}	Output Impedance			15		Ω

Function Tables

Table 3. Programmable Output Divider Function Table

Inputs			N Divider Value	Output Frequency (MHz)
N2	N1	N0		
0	0	0	÷1 (default)	250
0	0	1	÷2	125
0	1	0	÷3	83.333
0	1	1	÷4	62.5
1	0	0	÷5	50
1	0	1	÷6	41.667
1	1	0	÷8	31.25
1	1	1	÷16	15.625

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	100.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			40		mA
I_{DDO}	Output Supply Current			1		mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			40		mA
I_{DDO}	Output Supply Current			1		mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.15V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.65	1.8	1.95	V
I_{DD}	Power Supply Current			40		mA
I_{DDO}	Output Supply Current			1		mA

Table 4D. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			39		mA
I_{DDO}	Output Supply Current			1		mA

Table 4E. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.15V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.65	1.8	1.95	V
I_{DD}	Power Supply Current			39		mA
I_{DDO}	Output Supply Current			1		mA

Table 4F. LVCMOS/LVTTL DC Characteristics, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.625V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.465V$	-0.3		0.8	V
			$V_{DD} = 2.625V$	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK1, N[2:0], CLK_SEL	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	μA
		OE	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	μA
I_{IL}	Input Low Current	CLK0, CLK1, N[2:0], CLK_SEL	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			μA
		OE	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			μA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$	2.6			V
			$V_{DDO} = 2.5V \pm 5\%$	1.8			V
			$V_{DDO} = 1.8V \pm 0.15V$	1.5			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$			0.5	V
			$V_{DDO} = 2.5V \pm 5\%$			0.5	V
			$V_{DDO} = 1.8V \pm 0.15V$			0.4	V
I_{OZL}	Output Hi-Z Current Low			-5			μA
I_{OZH}	Output Hi-Z Current High					5	μA

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, *Output Load Test Circuit diagrams*.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay, Low to High; NOTE 1			4.3		ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3					ps
t_R / t_F	Output Rise/Fall Time; NOTE 4	20% to 80%		700		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 4				5	ns
t_{DIS}	Output Disable Time; NOTE 4				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq 250\text{MHz}$ unless noted otherwise.

NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions.

Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: This parameters are guaranteed by characterization. Not tested in production.

Table 5B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay, Low to High; NOTE 1			4.6		ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3					ps
t_R / t_F	Output Rise/Fall Time; NOTE 4	20% to 80%		800		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 4				5	ns
t_{DIS}	Output Disable Time; NOTE 4				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq 250\text{MHz}$ unless noted otherwise.

NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions.

Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: This parameters are guaranteed by characterization. Not tested in production.

Table 5C. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.15V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay, Low to High; NOTE 1			5		ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3					ps
t_R / t_F	Output Rise/Fall Time; NOTE 4	20% to 80%		1		ns
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 4				5	ns
t_{DIS}	Output Disable Time; NOTE 4				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq 250\text{MHz}$ unless noted otherwise.

NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: This parameters are guaranteed by characterization. Not tested in production..

Table 5D. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay, Low to High; NOTE 1			4.7		ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3					ps
t_R / t_F	Output Rise/Fall Time; NOTE 4	20% to 80%		900		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 4				5	ns
t_{DIS}	Output Disable Time; NOTE 4				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq 250\text{MHz}$ unless noted otherwise.

NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: This parameters are guaranteed by characterization. Not tested in production.

Table 5E. AC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.15V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay, Low to High; NOTE 1			5		ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3					ps
t_R / t_F	Output Rise/Fall Time; NOTE 4	20% to 80%		1.1		ns
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 4				5	ns
t_{DIS}	Output Disable Time; NOTE 4				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq 250MHz$ unless noted otherwise.

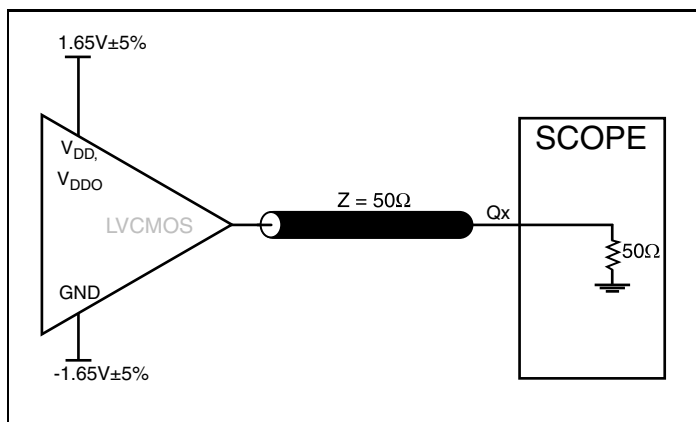
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

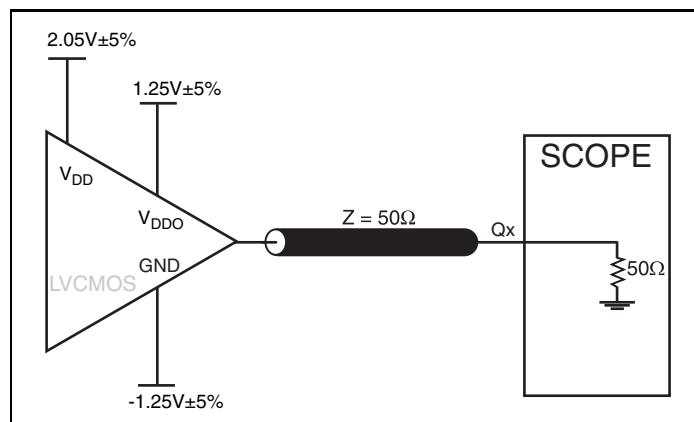
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: This parameters are guaranteed by characterization. Not tested in production.

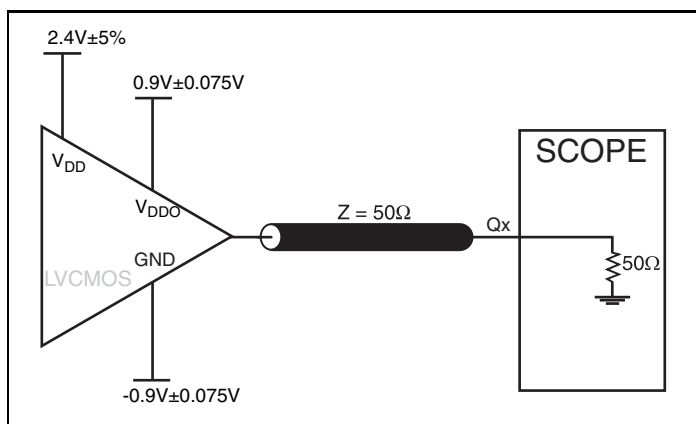
Parameter Measurement Information



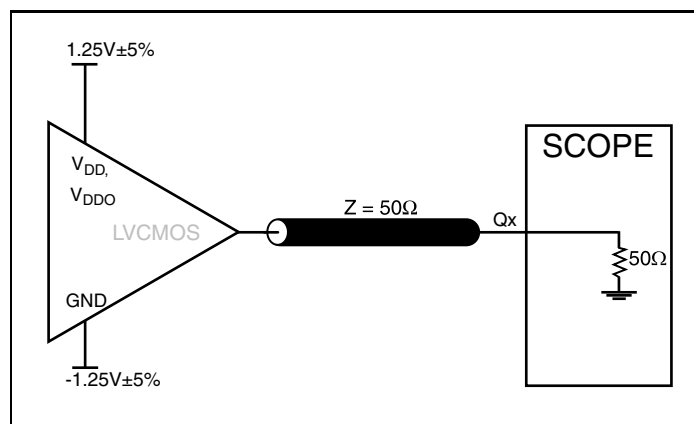
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



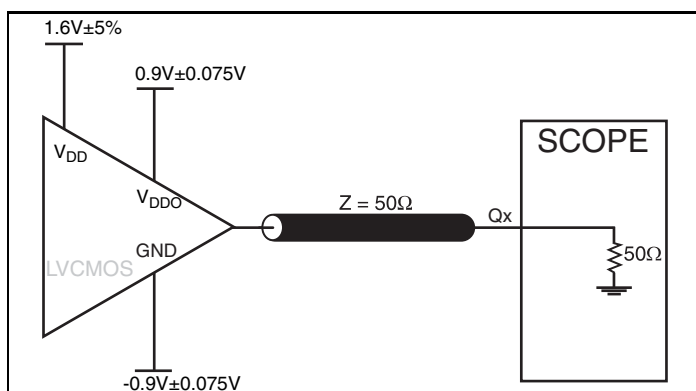
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



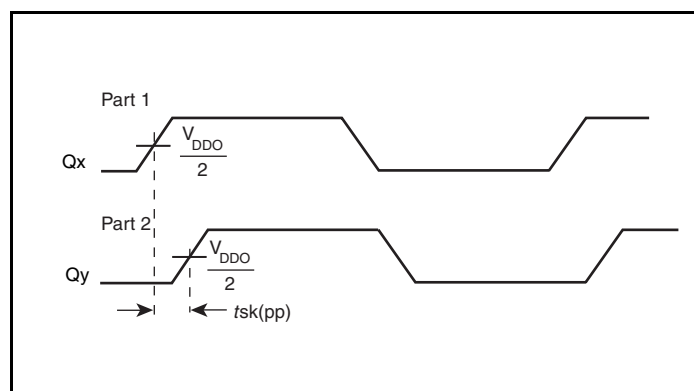
3.3V Core/1.8V LVCMOS Output Load AC Test Circuit



2.5V Core/2.5V LVCMOS Output Load AC Test Circuit

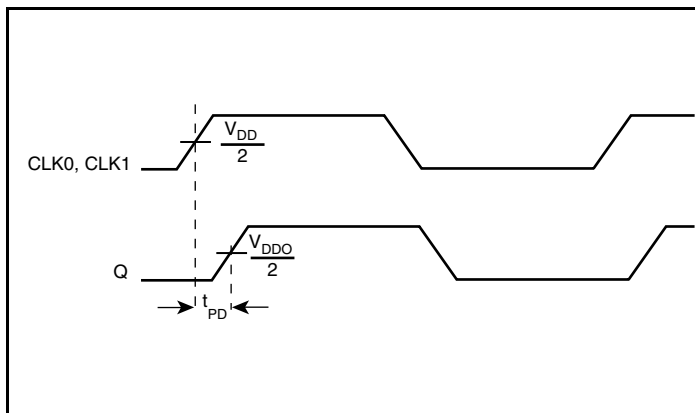


2.5V Core/1.8V LVCMOS Output Load AC Test Circuit

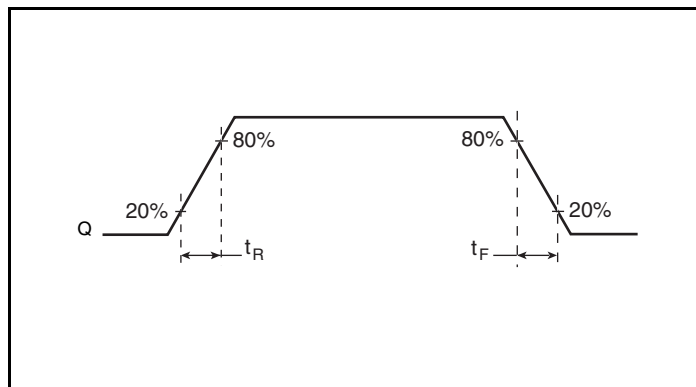


Part-to-Part Skew

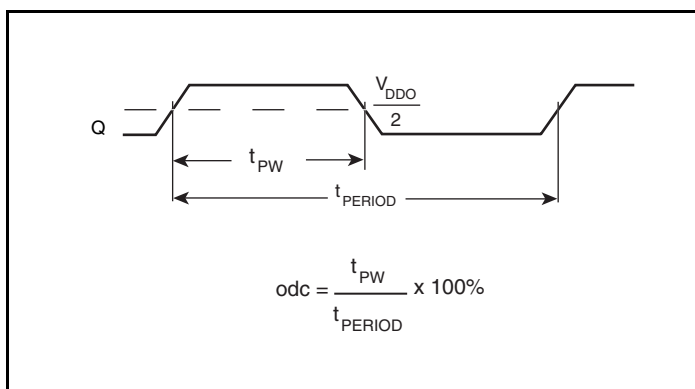
Parameter Measurement Information, continued



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from the CLK input to ground.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

Transistor Count

The transistor count for ICS87001-01: 2781

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

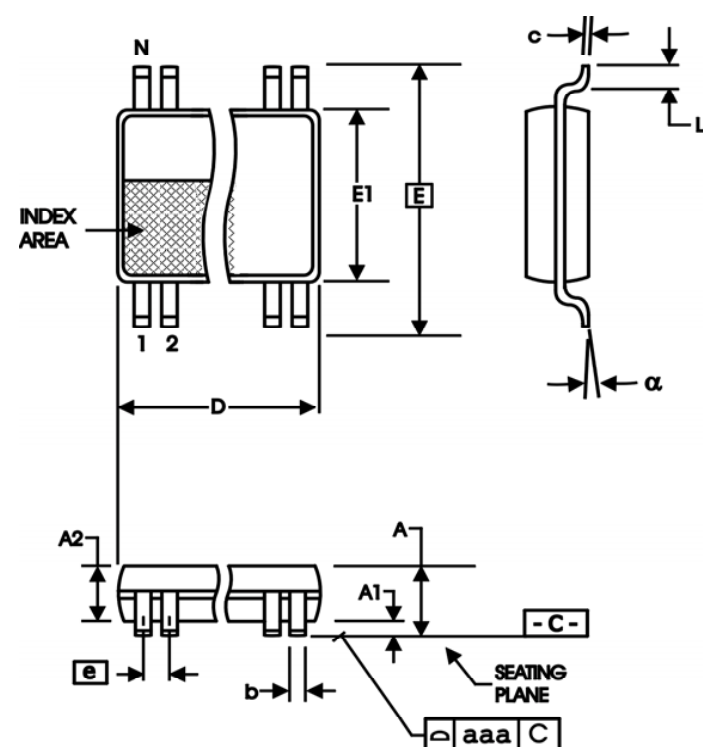


Table 7. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	16	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87001BG-01	87001B01	16 Lead TSSOP	Tube	0°C to 70°C
87001BG-01T	87001B01	16 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
87001BG-01LF	7001B01L	"Lead-Free" 16 Lead TSSOP	Tube	0°C to 70°C
87001BG-01LFT	7001B01L	"Lead-Free" 16 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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