

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	62.5 ns ($f(X_{IN}) = 16$ MHz, $V_{CC} = 3.0$ to 5.5 V) 100 ns ($f(X_{IN}) = 10$ MHz, $V_{CC} = 2.7$ to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2 "Product List"
Peripheral function	Interrupt	Internal: 10 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler)
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Input capture circuit
	Serial I/O	•1 channel Clock synchronous, UART •1 channel UART
	A-D converter	10-bit A-D converter: 1 circuit, 8 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •Ring oscillator
	Oscillation stop detection function	Stop detection of main clock oscillation
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8, max. 20 mA)
Electrical characteristics	Power supply voltage	$V_{CC} = 3.0$ to 5.5 V ($f(X_{IN}) = 16$ MHz) $V_{CC} = 2.7$ to 5.5 V ($f(X_{IN}) = 10$ MHz)
	Power consumption	Typ. 8 mA ($V_{CC} = 5.0$ V, ($f(X_{IN}) = 16$ MHz, High-speed mode) Typ. 5 mA ($V_{CC} = 3.0$ V, ($f(X_{IN}) = 10$ MHz, High-speed mode) Typ. 35 μ A ($V_{CC} = 3.0$ V, Wait mode, Peripheral clock off) Typ. 0.7 μ A ($V_{CC} = 3.0$ V, Stop mode)
Flash memory	Program/erase voltage	$V_{CC} = 2.7$ to 5.5 V
	Number of program/erase	100 times
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (option)
Package		32-pin plastic mold LQFP

Option: If you require this option, please specify so.

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

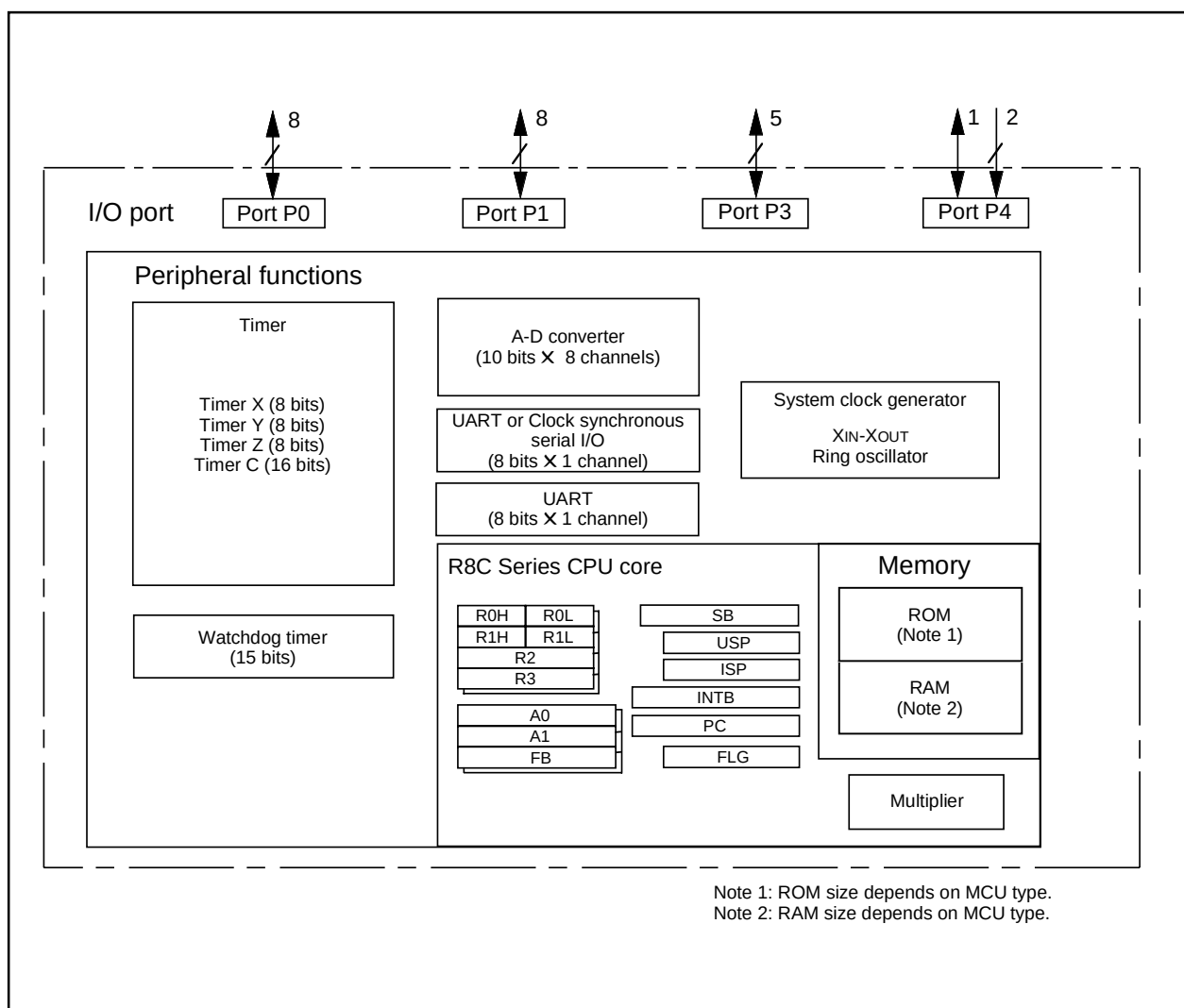


Figure 1.1 Block Diagram

1.4 Product List

Table 1.2 lists the products.

Table 1.2 Product List

As of Oct. 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21102FP	8K bytes	512 bytes	32P6U-A	Flash memory version
R5F21103FP	12K bytes	768 bytes	32P6U-A	
R5F21104FP	16K bytes	1K bytes	32P6U-A	
R5F21102DFP	8K bytes	512 bytes	32P6U-A	D version
R5F21103DFP	12K bytes	768 bytes	32P6U-A	
R5F21104DFP	16K bytes	1K bytes	32P6U-A	

★★ : Under development

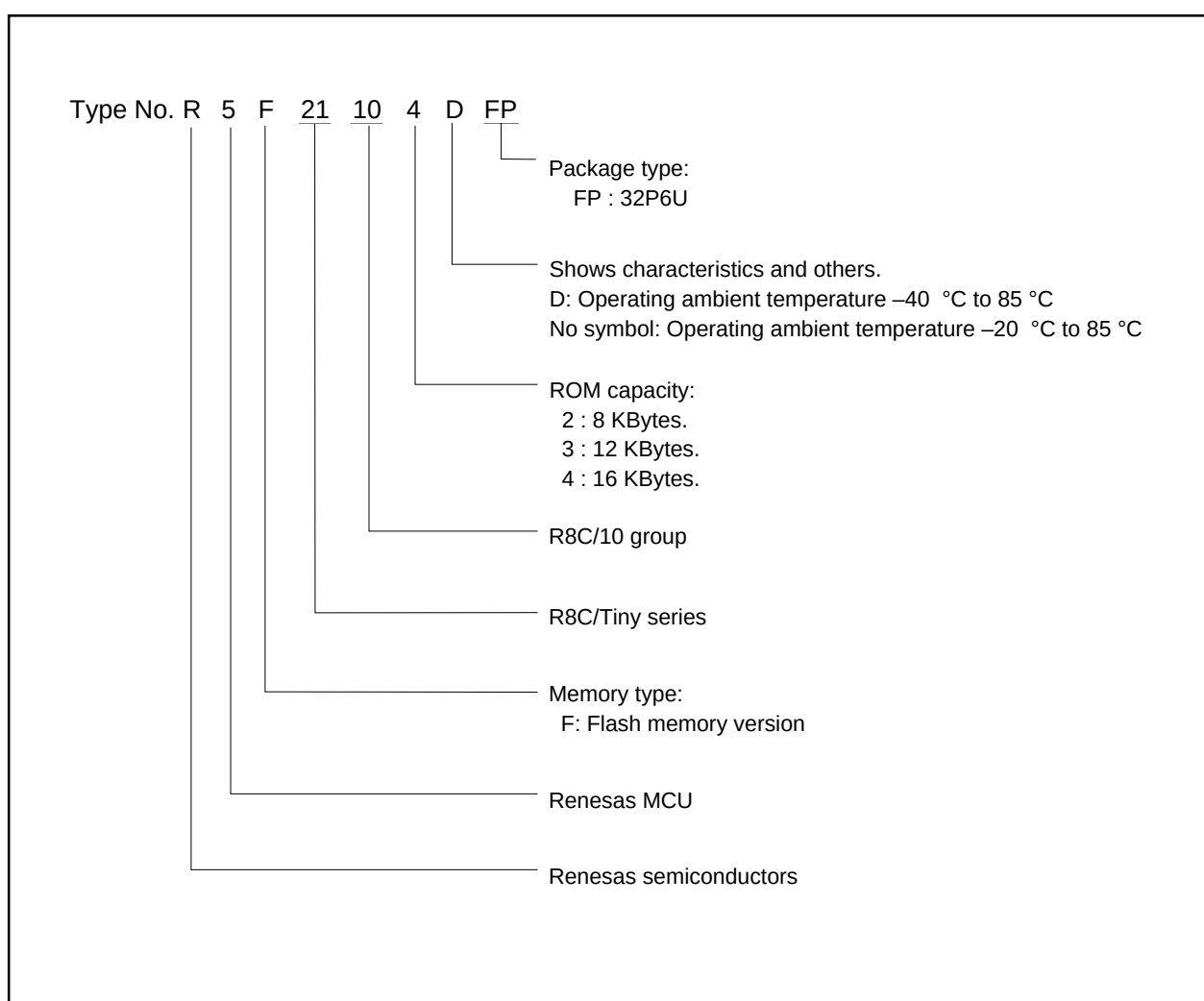


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Configuration

Figure 1.3 shows the pin configuration (top view).

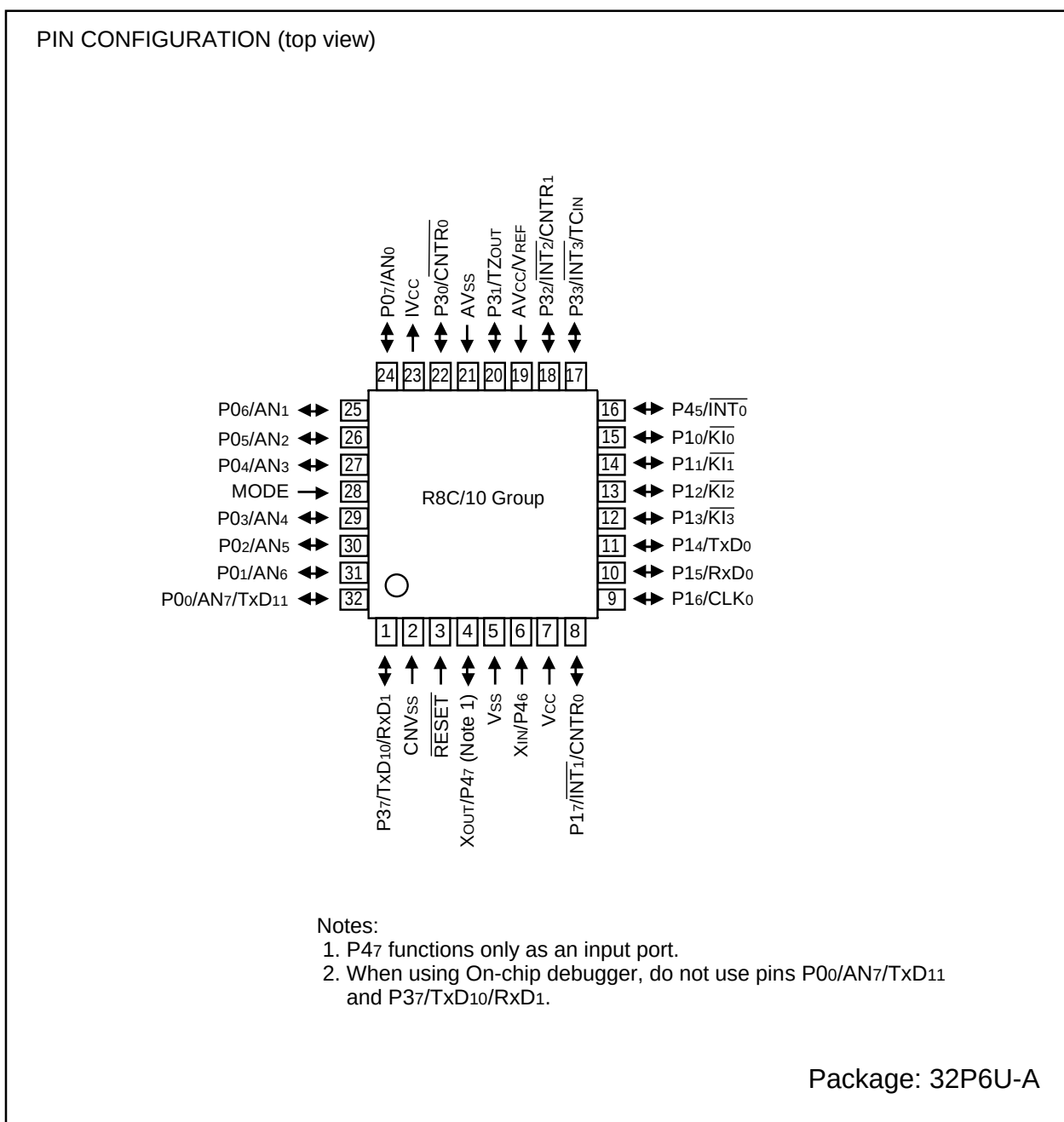


Figure 1.3 Pin Configuration (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	Input	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	Output	Connect this pin to Vss via a capacitor (0.1 μ F).
Analog power supply input	AVcc, AVss	Input	These are power supply input pins for A-D converter. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	RESET	Input	"L" on this input resets the MCU.
CNVss	CNVss	Input	Connect this pin to Vss via a resistor.
MODE	MODE	Input	Connect this pin to Vcc via a resistor.
Main clock input	XIN	Input	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	Output	
INT interrupt input	INT $\bar{0}$ to INT $\bar{3}$	Input	These are INT interrupt input pins.
Key input interrupt input	KI $\bar{0}$ to KI $\bar{3}$	Input	These are key input interrupt input pins.
Timer X	CNTR $\bar{0}$	Input/Output	This is the timer X I/O pin.
	CNTR $\bar{0}$	Output	This is the timer X output pin.
Timer Y	CNTR $\bar{1}$	Input/Output	This is the timer Y I/O pin.
Timer Z	TZOUT	Output	This is the timer Z output pin.
Timer C	TCIN	Input	This is the timer C input pin.
Serial interface	CLK $\bar{0}$	Input/Output	This is a transfer clock I/O pin.
	RxD $\bar{0}$, RxD $\bar{1}$	Input	These are serial data input pins.
	TxD $\bar{0}$, TxD $\bar{10}$, TxD $\bar{11}$	Output	These are serial data output pins.
Reference voltage input	VREF	Input	This is a reference voltage input pin for A-D converter.
A-D converter	AN $\bar{0}$ to AN $\bar{7}$	Input	These are analog input pins for A-D converter.
I/O port	P $\bar{0}$ to P $\bar{7}$, P $\bar{10}$ to P $\bar{17}$, P $\bar{30}$ to P $\bar{33}$, P $\bar{37}$, P $\bar{45}$	Input/Output	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P $\bar{10}$ to P $\bar{17}$ also function as LED drive ports.
Input port	P $\bar{46}$, P $\bar{47}$	Input	These are input only pins.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

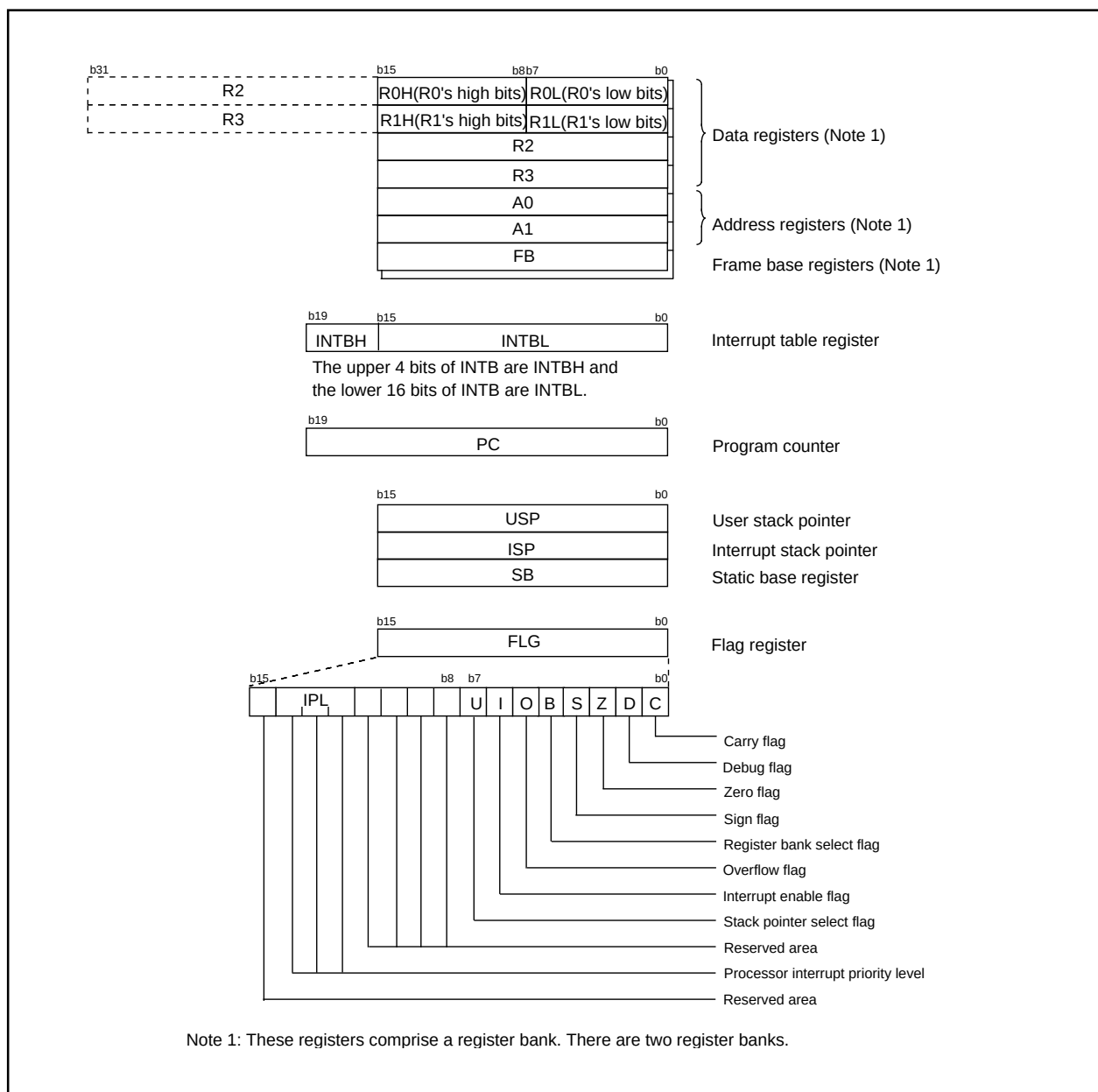


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 00000₁₆ to FFFFF₁₆.

The internal ROM is allocated in a lower address direction beginning with address 0FFFF₁₆. For example, a 16-Kbyte internal ROM is allocated to the addresses from 0C000₁₆ to 0FFFF₁₆.

The fixed interrupt vector table is allocated to the addresses from 0FFDC₁₆ to 0FFFF₁₆. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400₁₆. For example, a 1-Kbyte internal RAM is allocated to the addresses from 00400₁₆ to 007FF₁₆. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated. Special function registers (SFR) are allocated to the addresses from 00000₁₆ to 002FF₁₆. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.

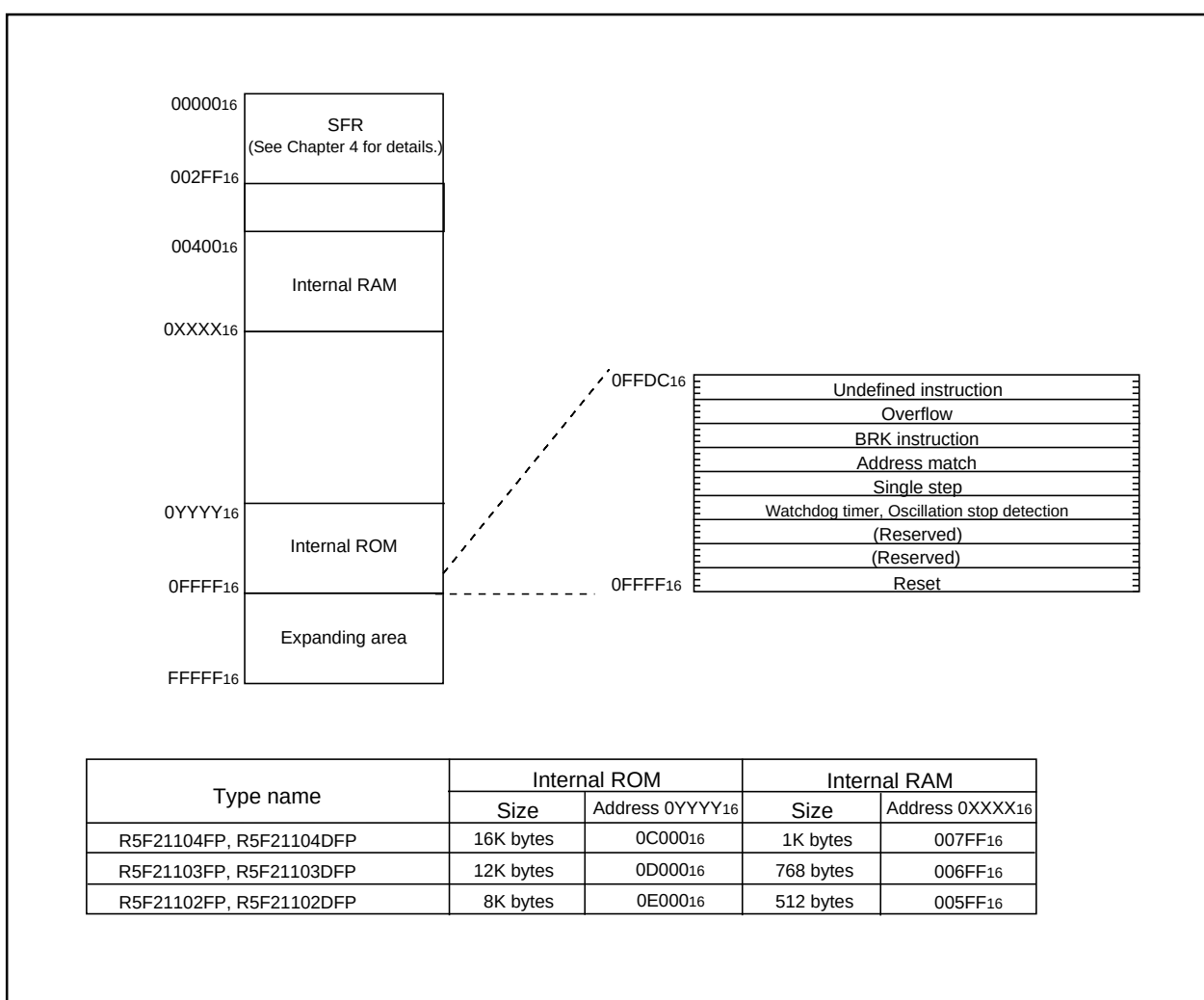


Figure 3.1 Memory Map

4. Special Function Register (SFR)

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	0016
0005 ₁₆	Processor mode register 1	PM1	0016
0006 ₁₆	System clock control register 0	CM0	011010002
0007 ₁₆	System clock control register 1	CM1	001000002
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX002
000A ₁₆	Protect register	PRCR	00XXX0002
000B ₁₆			
000C ₁₆	Oscillation stop detection register	OCD	000001002
000D ₁₆	Watchdog timer reset register	WDTR	XX16
000E ₁₆	Watchdog timer start register	WDTS	XX16
000F ₁₆	Watchdog timer control register	WDC	000XXXXX2
0010 ₁₆	Address match interrupt register 0	RMAD0	0016
0011 ₁₆			0016
0012 ₁₆			X016
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	0016
0015 ₁₆			0016
0016 ₁₆			X016
0017 ₁₆			
0018 ₁₆			
0019 ₁₆			
001A ₁₆			
001B ₁₆			
001C ₁₆			
001D ₁₆			
001E ₁₆	INT0 input filter select register	INT0F	XXXXX0002
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			

X : Undefined

Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆			
0049 ₁₆			
004A ₁₆			
004B ₁₆			
004C ₁₆			
004D ₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E ₁₆	A-D conversion interrupt control register	ADIC	XXXXX0002
004F ₁₆			
0050 ₁₆			
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 ₁₆	INT2 interrupt control register	INT2IC	XXXXX0002
0056 ₁₆	Timer X interrupt control register	TXIC	XXXXX0002
0057 ₁₆	Timer Y interrupt control register	TYIC	XXXXX0002
0058 ₁₆	Timer Z interrupt control register	TZIC	XXXXX0002
0059 ₁₆	INT1 interrupt control register	INT1IC	XXXXX0002
005A ₁₆	INT3 interrupt control register	INT3IC	XXXXX0002
005B ₁₆	Timer C interrupt control register	TCIC	XXXXX0002
005C ₁₆			
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E ₁₆			
005F ₁₆			
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

X : Undefined

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Address	Register	Symbol	After reset
0080 ₁₆	Timer Y, Z mode register	TYZMR	00 ₁₆
0081 ₁₆	Prescaler Y	PREY	FF ₁₆
0082 ₁₆	Timer Y secondary	TYSC	FF ₁₆
0083 ₁₆	Timer Y primary	TYPR	FF ₁₆
0084 ₁₆	Timer Y, Z waveform output control register	PUM	00 ₁₆
0085 ₁₆	Prescaler Z	PREZ	FF ₁₆
0086 ₁₆	Timer Z secondary	TZSC	FF ₁₆
0087 ₁₆	Timer Z primary	TZPR	FF ₁₆
0088 ₁₆			
0089 ₁₆			
008A ₁₆	Timer Y, Z output control register	TYZOC	00 ₁₆
008B ₁₆	Timer X mode register	TXMR	00 ₁₆
008C ₁₆	Prescaler X	PREX	FF ₁₆
008D ₁₆	Timer X register	TX	FF ₁₆
008E ₁₆	Count source set register	TCSS	00 ₁₆
008F ₁₆			
0090 ₁₆	Timer C register	TC	00 ₁₆
0091 ₁₆			00 ₁₆
0092 ₁₆			
0093 ₁₆			
0094 ₁₆			
0095 ₁₆			
0096 ₁₆	External input enable register	INTEN	00 ₁₆
0097 ₁₆			
0098 ₁₆	Key input enable register	KIEN	00 ₁₆
0099 ₁₆			
009A ₁₆	Timer C control register 0	TCC0	00 ₁₆
009B ₁₆	Timer C control register 1	TCC1	00 ₁₆
009C ₁₆	Capture register	TM0	XX ₁₆
009D ₁₆			XX ₁₆
009E ₁₆			
009F ₁₆			
00A0 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
00A1 ₁₆	UART0 bit rate generator	U0BRG	XX ₁₆
00A2 ₁₆	UART0 transmit buffer register	U0TB	XX ₁₆
00A3 ₁₆			XX ₁₆
00A4 ₁₆	UART0 transmit/receive control register 0	U0C0	00001000 ₂
00A5 ₁₆	UART0 transmit/receive control register 1	U0C1	00000010 ₂
00A6 ₁₆	UART0 receive buffer register	U0RB	XX ₁₆
00A7 ₁₆			XX ₁₆
00A8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
00A9 ₁₆	UART1 bit rate generator	U1BRG	XX ₁₆
00AA ₁₆	UART1 transmit buffer register	U1TB	XX ₁₆
00AB ₁₆			XX ₁₆
00AC ₁₆	UART1 transmit/receive control register 0	U1C0	00001000 ₂
00AD ₁₆	UART1 transmit/receive control register 1	U1C1	00000010 ₂
00AE ₁₆	UART1 receive buffer register	U1RB	XX ₁₆
00AF ₁₆			XX ₁₆
00B0 ₁₆	UART transmit/receive control register 2	UCON	00 ₁₆
00B1 ₁₆			
00B2 ₁₆			
00B3 ₁₆			
00B4 ₁₆			
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆			
00B9 ₁₆			
00BA ₁₆			
00BB ₁₆			
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X : Undefined

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Address	Register	Symbol	After reset
00C0 ₁₆	A-D register	AD	XX ₁₆
00C1 ₁₆			XX ₁₆
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆	A-D control register 2	ADCON2	00 ₁₆
00D5 ₁₆			
00D6 ₁₆	A-D control register 0	ADCON0	00000XXX ₂
00D7 ₁₆	A-D control register 1	ADCON1	00 ₁₆
00D8 ₁₆			
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆			
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆	Port P0 register	P0	XX ₁₆
00E1 ₁₆	Port P1 register	P1	XX ₁₆
00E2 ₁₆	Port P0 direction register	PD0	00 ₁₆
00E3 ₁₆	Port P1 direction register	PD1	00 ₁₆
00E4 ₁₆			
00E5 ₁₆	Port P3 register	P3	XX ₁₆
00E6 ₁₆			
00E7 ₁₆	Port P3 direction register	PD3	00 ₁₆
00E8 ₁₆	Port P4 register	P4	XX ₁₆
00E9 ₁₆			
00EA ₁₆	Port P4 direction register	PD4	00 ₁₆
00EB ₁₆			
00EC ₁₆			
00ED ₁₆			
00EE ₁₆			
00EF ₁₆			
00F0 ₁₆			
00F1 ₁₆			
00F2 ₁₆			
00F3 ₁₆			
00F4 ₁₆			
00F5 ₁₆			
00F6 ₁₆			
00F7 ₁₆			
00F8 ₁₆			
00F9 ₁₆			
03FA ₁₆			
00FB ₁₆			
00FC ₁₆	Pull-up control register 0	PUR0	00XX0000 ₂
00FD ₁₆	Pull-up control register 1	PUR1	XXXXXX0X ₂
00FE ₁₆	Port P1 drivability control register	DRR	00 ₁₆
00FF ₁₆			
01B3 ₁₆	Flash memory control register 4	FMR4	0100000X ₂
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1	FMR1	0100XX0X ₂
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0	FMR0	XX000001 ₂

X : Undefined

Blank columns are all reserved space. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V _{CC}	Supply voltage	V _{CC} =AV _{CC}	-0.3 to 6.5	V
AV _{CC}	Analog supply voltage	V _{CC} =AV _{CC}	-0.3 to 6.5	V
V _I	Input voltage		-0.3 to V _{CC} +0.3	V
V _O	Output voltage		-0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _{opr} =25 °C	300	mW
T _{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T _{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V _{CC}	Supply voltage			2.7	5.0	5.5	V
AV _{CC}	Analog supply voltage			—	V _{CC}	—	V
V _{SS}	Supply voltage			—	0	—	V
AV _{SS}	Analog supply voltage			—	0	—	V
V _{IH}	"H" input voltage			0.8V _{CC}	—	V _{CC}	V
V _{IL}	"L" input voltage			0	—	0.2V _{CC}	V
I _{OH} (sum)	"H" peak all output currents	Sum of all pins' I _{OH} (peak)		—	—	-60.0	mA
I _{OH} (peak)	"H" peak output current			—	—	-10.0	mA
I _{OH} (avg)	"H" average output current			—	—	-5.0	mA
I _{OL} (sum)	"L" peak all output currents	Sum of all pins' I _{OL} (peak)		—	—	60	mA
I _{OL} (peak)	"L" peak output current	Except P10 to P17		—	—	10	mA
		P10 to P17	Drive ability HIGH	—	—	30	mA
		P10 to P17	Drive ability LOW	—	—	10	mA
I _{OL} (avg)	"L" average output current	Except P10 to P17		—	—	5	mA
		P10 to P17	Drive ability HIGH	—	—	15	mA
		P10 to P17	Drive ability LOW	—	—	5	mA
f (X _{IN})	Main clock input oscillation frequency		3.0V ≤ V _{CC} ≤ 5.5V	0	—	16	MHz
			2.7V ≤ V _{CC} < 3.0V	0	—	10	MHz

Note

1: Referenced to V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.

2: The mean output current is the mean value within 100ms.

Table 5.3 A-D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = V_{CC}$			10	Bit
—	Absolute accuracy	10 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0V$			± 3	LSB
		8 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0V$			± 2	LSB
		10 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3V$			± 5	LSB
		8 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3V$			± 2	LSB
R_{LADDER}	Ladder resistance		$V_{REF} = V_{CC}$	10		40	k Ω
t_{CONV}	Conversion time	10 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0V$	3.3			μs
		8 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0V$	2.8			μs
V_{REF}	Reference voltage			2.0		V_{CC}	V
V_{IA}	Analog input voltage			0		V_{ref}	V
—	A-D operation clock frequency ²	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

Note

- 1: Referenced to $V_{CC} = AV_{CC} = 2.7$ to $5.5V$ at $T_{opr} = -20$ to $85 \text{ }^{\circ}C$ / -40 to $85 \text{ }^{\circ}C$ unless otherwise specified.
- 2: When f_{AD} is 10 MHz more, divide the f_{AD} and make A-D operation clock frequency ($\emptyset AD$) lower than 10 MHz.
- 3: When the V_{CC} is less than $4.2V$, divide the f_{AD} and make A-D operation clock frequency ($\emptyset AD$) lower than $f_{AD}/2$.

Table 5.4 Flash Memory Version Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase cycle		100	—	—	cycle
—	Byte program time	$V_{CC} = 5.0V$, $T_{opr} = 25 \text{ }^{\circ}C$	—	50	400	μs
—	Block erase time	$V_{CC} = 5.0V$, $T_{opr} = 25 \text{ }^{\circ}C$	—	0.4	9	s
—	Time delay from suspend request until erase suspend		—	—	8	ms
—	Program, Erase voltage		2.7	—	5.5	V
—	Read voltage		2.7	—	5.5	V
—	Program, Erase temperature		0	—	60	$^{\circ}C$
—	Data-retention duration	$T_{opr} = 55 \text{ }^{\circ}C$	—	—	20	year

Note

- 1: Referenced to $V_{CC1} = AV_{CC} = 2.7$ to $5.5V$ at $T_{opr} = 0$ to $60 \text{ }^{\circ}C$ unless otherwise specified.

Table 5.5 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Min.	Standard		Unit
				Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on ²				2	ms
$t_{d(R-S)}$	STOP release time ³				150	μs

Note

- 1: The measuring condition is $V_{CC} = AV_{CC} = 2.7$ to $5.5V$ and $T_{opr} = 25 \text{ }^{\circ}C$.
- 2: This shows the waiting time till the internal power supply generating circuit is stabilized during powering-on.
- 3: This shows the time till BCLK starts from the interrupt acknowledgement to cancel stop mode.

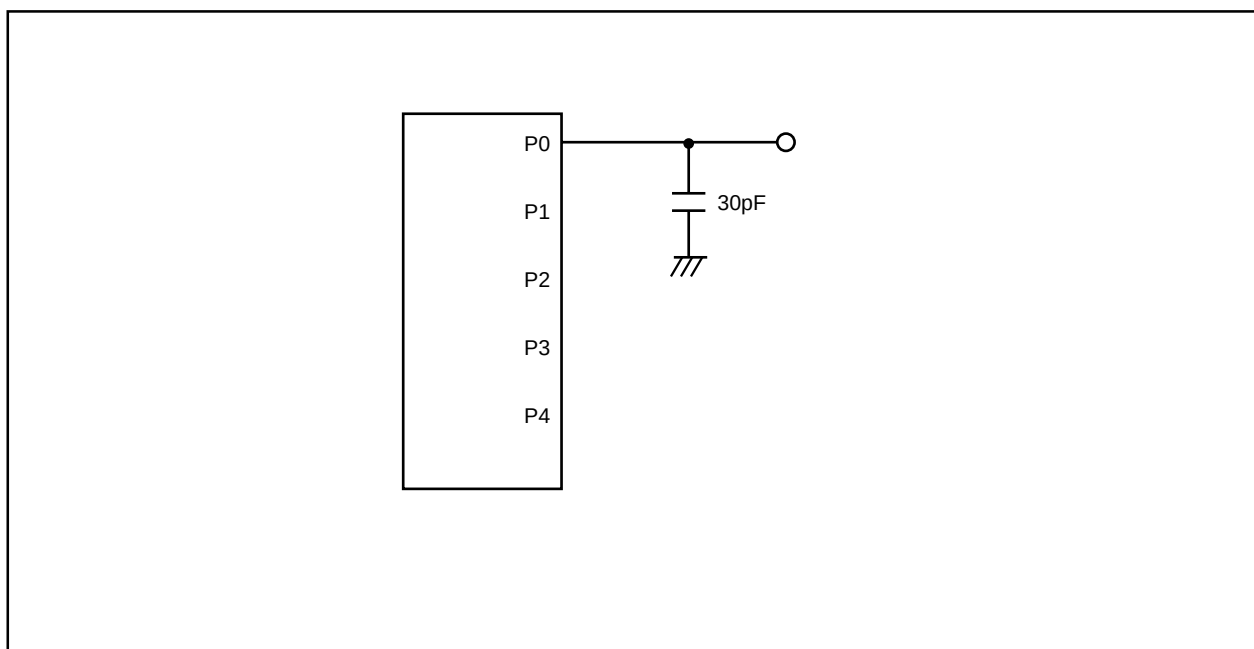
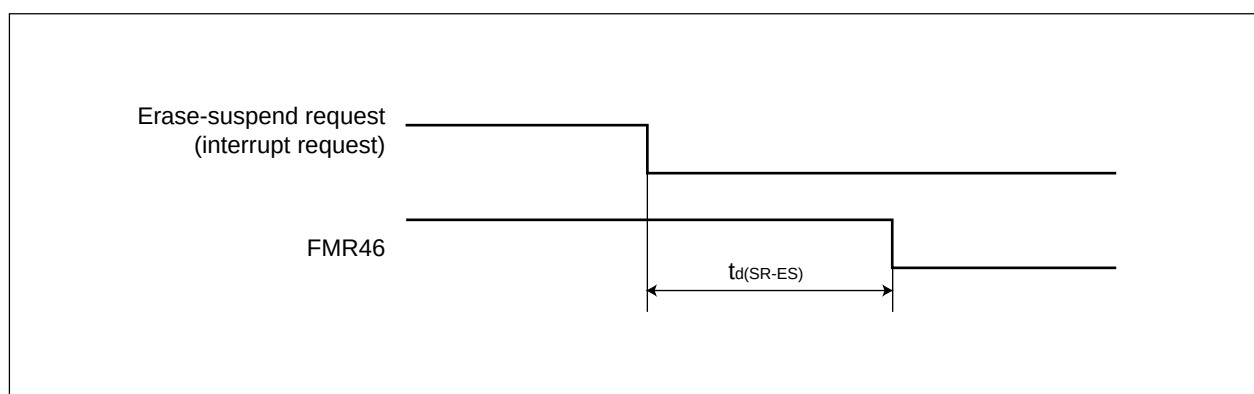
**Figure 5.1 Port P0 to P4 measurement circuit****Figure 5.2 Time delay from Suspend Request until Erase Suspend**

Table 5.6 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-5mA	Vcc-2.0		Vcc	V
			IOH=-200μA	Vcc-0.3		Vcc	V
	XOUT		Drive ability HIGH IOH=-1 mA	Vcc-2.0		Vcc	V
			Drive ability LOW IOH=-500μA	Vcc-2.0		Vcc	V
VOL	"L" output voltage	P10 to P17 Except XOUT	IOH= 5 mA			2.0	V
			IOH= 200 μA			0.45	V
	P10 to P17		Drive ability HIGH IOH= 10 mA			2.0	V
			Drive ability LOW IOH= 5 mA			2.0	V
	XOUT		Drive ability HIGH IOH= 1 mA			2.0	V
			Drive ability LOW IOH=500μA			2.0	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1		0.2		1.0	V
		RESET		0.2		2.2	V
IiH	"H" input current		Vi=5V			5.0	μA
IiL	"L" input current		Vi=0V			-5.0	μA
RPULLUP	Pull-up resistance		Vi=0V	30	50	167	kΩ
RfXIN	Feedback resistance	XIN			1.0		MΩ
fRING	Ring oscillator frequency			40	125	250	kHz
V _{RAM}	RAM retention voltage		At stop mode	2.0			V

Note

1 : Referenced to Vcc=AVcc=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

Table 5.7 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition	Min.	Standard Typ.	Max.	Unit
I _{CC}	Power supply current (V _{CC} =3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V _{SS}	High-speed mode	X _{IN} =16 MHz (square wave) Ring oscillator on=125 kHz No division	8	14	mA
			X _{IN} =10 MHz (square wave) Ring oscillator on=125 kHz No division	5		mA
		Medium-speed mode	X _{IN} =16 MHz (square wave) Ring oscillator on=125 kHz Division by 8	3		mA
			X _{IN} =10 MHz (square wave) Ring oscillator on=125 kHz Division by 8	2		mA
		Ring oscillator mode	Main clock off Ring oscillator on=125 kHz Division by 8	0.4	2.0	mA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed ² Peripheral clock operation	40	80	μA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed ² Peripheral clock off	38	76	μA
		Stop mode	Main clock off Ring oscillator off CM10="1" Peripheral clock off	0.8	3.0	μA

Note

- 1: The power supply current measuring is executed using the measuring program on flash memory.
 2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: Vcc = 5V, Vss = 0V at Ta = 25 °C) [Vcc=5V]**Table 5.8 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	62.5		ns
tWH(XIN)	XIN input HIGH pulse width	30		ns
tWL(XIN)	XIN input LOW pulse width	30		ns

Table 5.9 CNTR0 input, CNTR1 input, INT2 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	100		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	40		ns

Table 5.10 TCIN input, INT3 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	400 ¹		ns
tWH(TCIN)	TCIN input HIGH pulse width	200 ²		ns
tWL(TCIN)	TCIN input LOW pulse width	200 ²		ns

Note

1 : Use the greater value, either (1/ digital filter clock frequency x 6) or min. value.

2 : Use the greater value, either (1/ digital filter clock frequency x 3) or min. value.

Table 5.11 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input HIGH pulse width	100		ns
tw(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.12 External interrupt INT0 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	INT0 input HIGH pulse width	250 ¹		ns
tw(INL)	INT0 input LOW pulse width	250 ²		ns

Note

1 : When the INT0 input filter select bit selects the digital filter, use the INT0 input HIGH pulse width to the greater value, either (1/ digital filter clock frequency x 3) or min. value.

2 : When the INT0 input filter select bit selects the digital filter, use the INT0 input LOW pulse width to the greater value, either (1/ digital filter clock frequency x 3) or min. value.

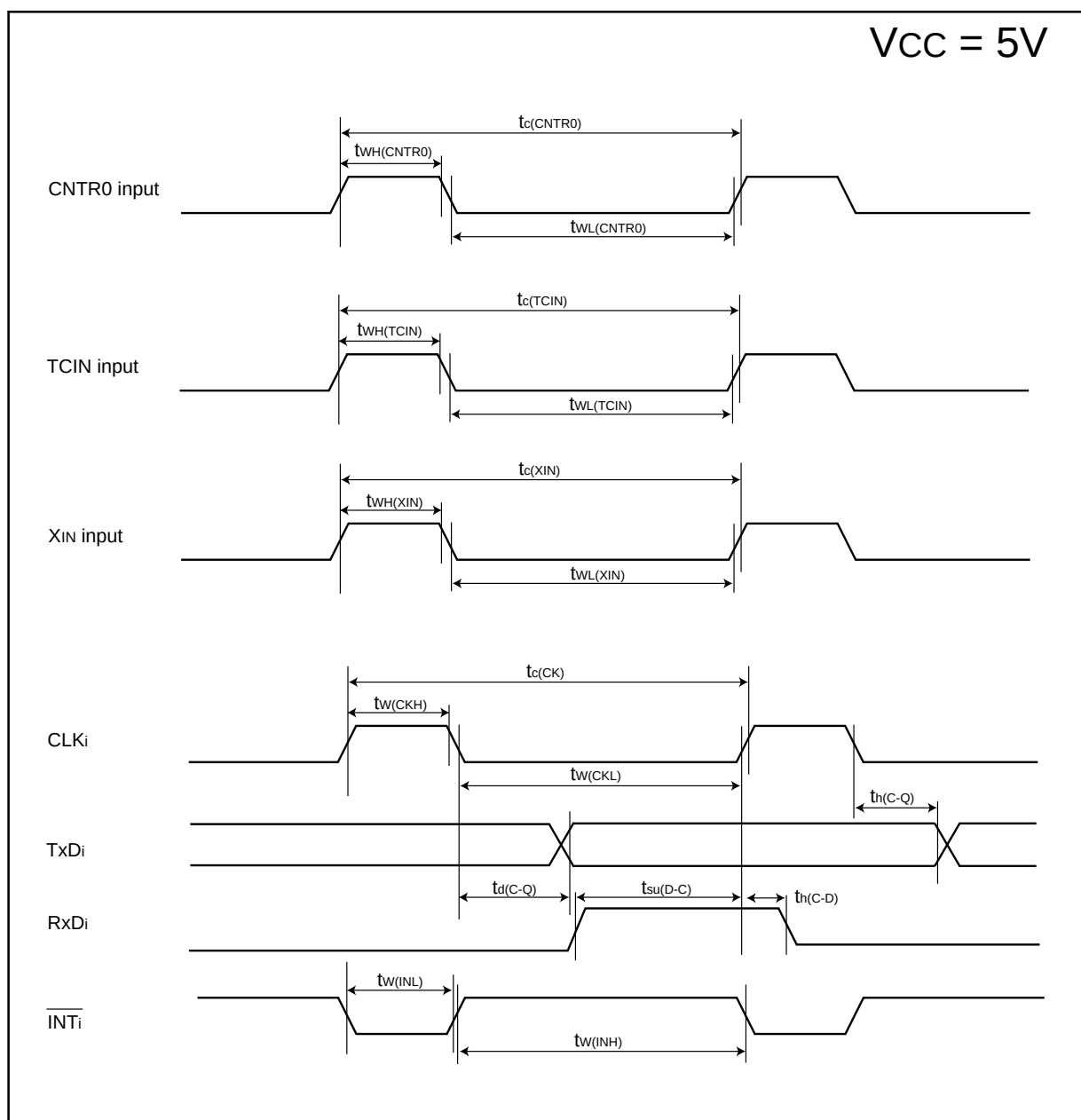
Figure 5.3 $V_{CC}=5V$ timing diagram

Table 5.13 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-1mA	Vcc-0.5		Vcc	V
		XOUT	Drive ability HIGH IOH=-0.1 mA	Vcc-0.5		Vcc	V
			Drive ability LOW IOH=-50 μA	Vcc-0.5		Vcc	V
VOL	"L" output voltage	P10 to P17 Except XOUT	IOH= 1 mA			0.5	V
		P10 to P17	Drive ability HIGH IOH= 2 mA			0.5	V
			Drive ability LOW IOH= 1 mA			0.5	V
		XOUT	Drive ability HIGH IOH= 0.1 mA			0.5	V
			Drive ability LOW IOH=50 μA			0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RXD0, RXD1		0.2		0.8	V
		RESET		0.2		1.8	V
IiH	"H" input current		Vi=3V			4.0	μA
IiL	"L" input current		Vi=0V			-4.0	μA
RPULLUP	Pull-up resistance		Vi=0V	66	160	500	kΩ
RiXIN	Feedback resistance	XIN			3.0		MΩ
fRING	Ring oscillator frequency			40	125	250	kHz
VRAM	RAM retention voltage		At stop mode	2.0			V

Note

1 : Referenced to Vcc=AVcc=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

Table 5.14 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition		Min.	Standard Typ.	Max.	Unit
I _{CC}	Power supply current (V _{CC1} =2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V _{SS}	High-speed mode	X _{IN} =16 MHz (square wave) Ring oscillator on=125 kHz No division		7	12	mA
			X _{IN} =10 MHz (square wave) Ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X _{IN} =16 MHz (square wave) Ring oscillator on=125 kHz Division by 8		2.5		mA
			X _{IN} =10 MHz (square wave) Ring oscillator on=125 kHz Division by 8		1.6		mA
		Ring oscillator mode	Main clock off Ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed ² Peripheral clock operation		37	74	μA
		Wait mode	Main clock off Ring oscillator on=125 kHz When a WAIT instruction is executed ² Peripheral clock off		35	70	μA
		Stop mode	Main clock off Ring oscillator off CM10="1" Peripheral clock off		0.7	3.0	μA

Note

- 1: The power supply current measuring is executed using the measuring program on frash memory.
 2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: $V_{CC} = 3V$, $V_{SS} = 0V$ at $T_a = 25^\circ C$) [$V_{CC}=3V$]**Table 5.15 X_{IN} input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(X_{IN})$	X_{IN} input cycle time	143		ns
$t_{WH}(X_{IN})$	X_{IN} input HIGH pulse width	70		ns
$t_{WL}(X_{IN})$	X_{IN} input LOW pulse width	70		ns

Table 5.16 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CNTR0)$	CNTR0 input cycle time	300		ns
$t_{WH}(CNTR0)$	CNTR0 input HIGH pulse width	120		ns
$t_{WL}(CNTR0)$	CNTR0 input LOW pulse width	120		ns

Table 5.17 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(TCIN)$	TCIN input cycle time	1200 ¹		ns
$t_{WH}(TCIN)$	TCIN input HIGH pulse width	600 ²		ns
$t_{WL}(TCIN)$	TCIN input LOW pulse width	600 ²		ns

Note

1 : Use the greater value, either (1/ digital filter clock frequency x 6) or min. value.

2 : Use the greater value, either (1/ digital filter clock frequency x 3) or min. value.

Table 5.18 Serial I/O

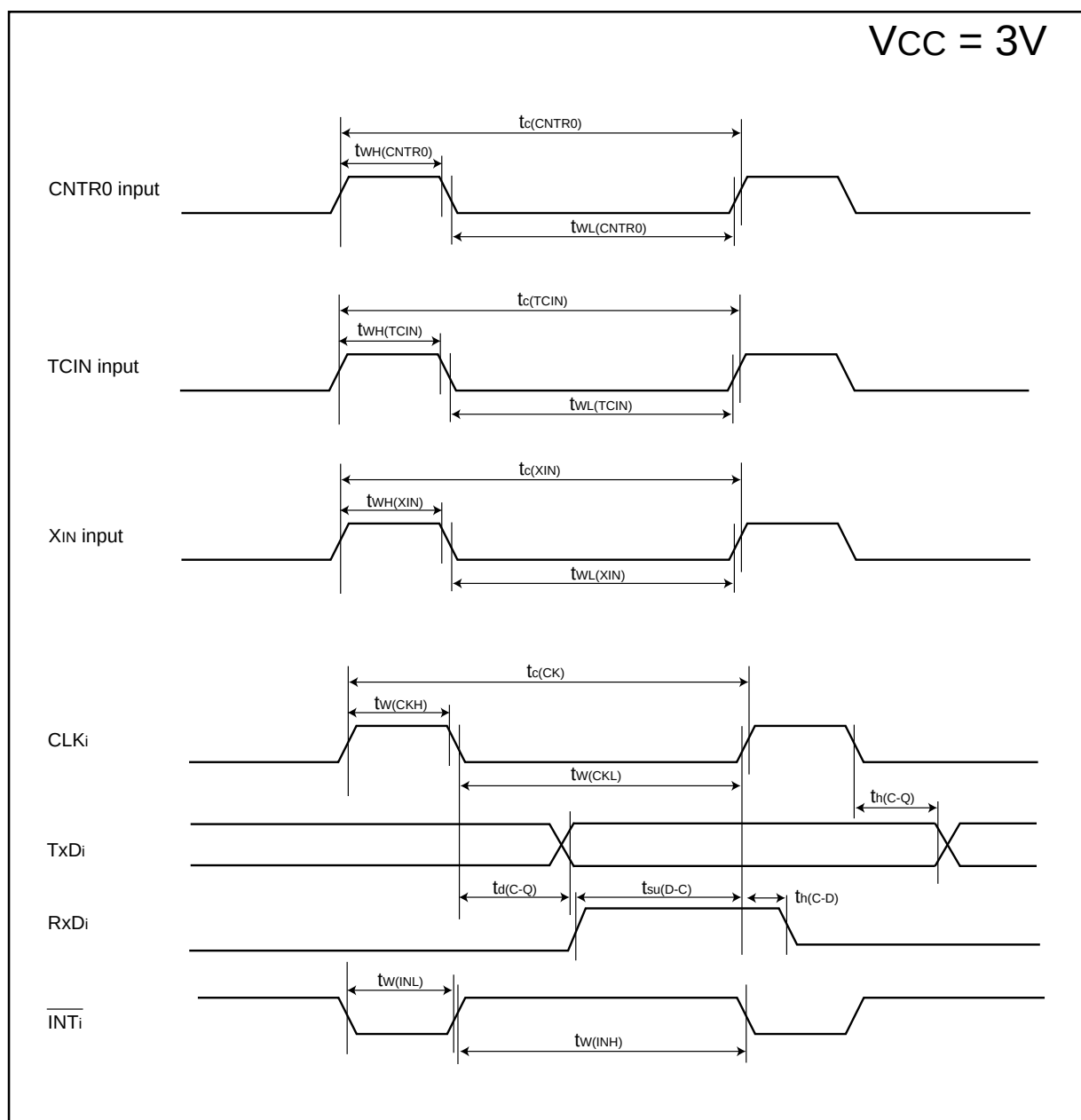
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CLK)$	CLKi input cycle time	300		ns
$t_{W}(CLKH)$	CLKi input HIGH pulse width	150		ns
$t_{W}(CLKL)$	CLKi input LOW pulse width	150		ns
$t_d(C-Q)$	TxDi output delay time		160	ns
$t_h(C-Q)$	TxDi hold time	0		ns
$t_{su}(D-C)$	RxDi input setup time	55		ns
$t_h(C-D)$	RxDi input hold time	90		ns

Table 5.19 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W}(\overline{INTH})$	$\overline{INT0}$ input HIGH pulse width	380 ¹		ns
$t_{W}(\overline{INTL})$	$\overline{INT0}$ input LOW pulse width	380 ²		ns

Note

1 : When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input HIGH pulse width to the greater value, either (1/ digital filter clock frequency x 3) or min. value.2 : When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input LOW pulse width to the greater value, either (1/ digital filter clock frequency x 3) or min. value.

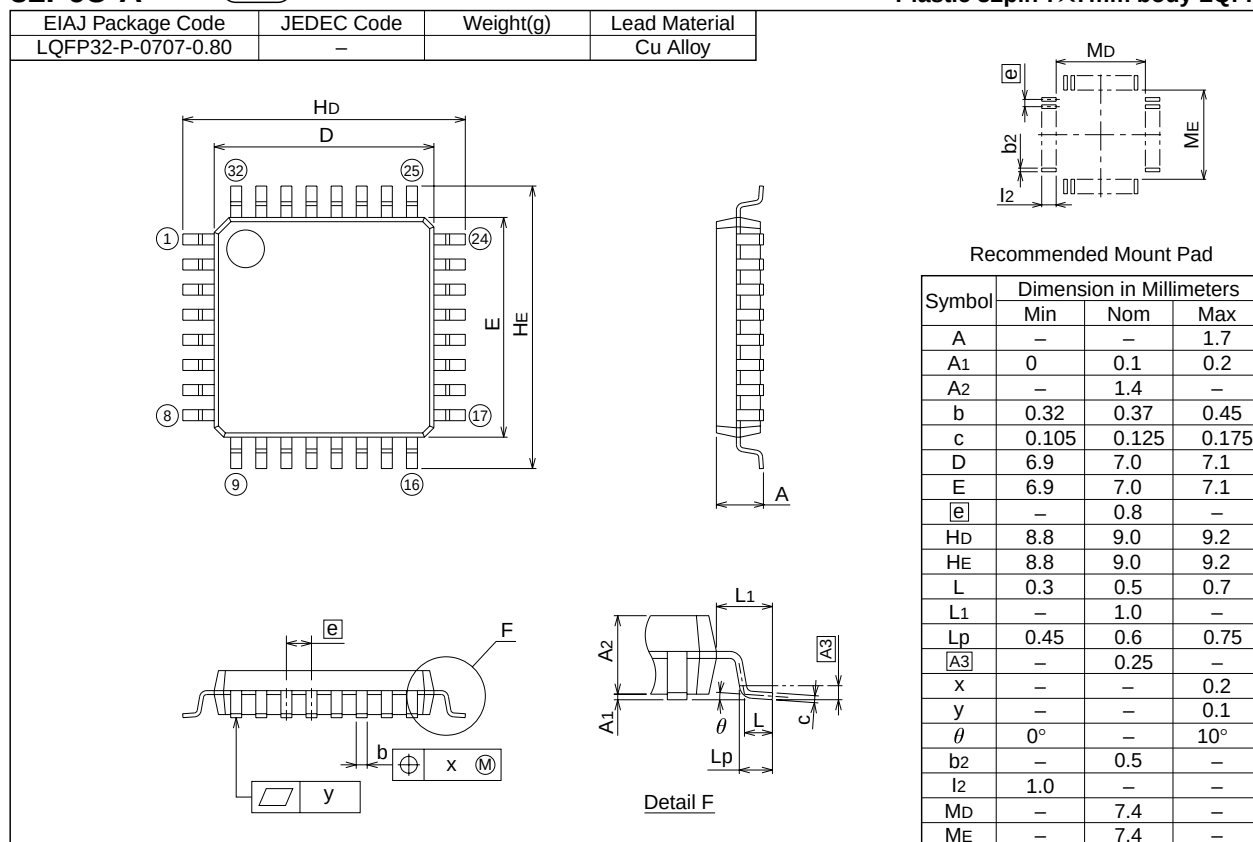
Figure 5.4 $V_{CC}=3V$ timing diagram

Package Dimensions

32P6U-A

(MMP)

Plastic 32pin 7X7mm body LQFP



REVISION HISTORY	R8C/10 Group Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jun. 19, 2003		First edition issued
1.10	Sep. 08, 2003	2 5 6 12 14	Table 1.1: Shortest instruction execution time and $f(X_{IN})$ changed Figure 1.3: Pin name changed from TXOUT to $\overline{CNTR0}$ Table 1.3: Pin name changed from TXOUT to $\overline{CNTR0}$ The value of Time C register after reset changed Chapter "5. Electrical Characteristics" added
1.20	Oct. 31, 2003	2 6 14 15 16 18 19 20 21 22 23 24	Table 1.1: Power consumption values added Table 1.3: Resistor value for CNVss and MODE deleted Table 5.2: Note 3 and Note 4 deleted tsamp in Table 5.3 deleted Figure 5.1 added Table 5.7: Vcc changed from "4.2 to 5.5V" to "3.3V to 5.5V", ring oscillator changed from "on 100kHz" to "125kHz", $X_{IN}=5\text{MHz}$ deleted and $X_{IN}=10\text{MHz}$ added in high-speed mode and medium-speed mode, data added and modified Table 5.8 to Table 5.12 added Figure 5.2 added Table 5.13: Note 1, $f(BCLK)=5\text{ MHz}$ changed to 10 MHz Table 5.14: ring oscillator changed from "on 100kHz" to "125kHz", $X_{IN}=5\text{MHz}$ deleted and $X_{IN}=10\text{MHz}$ added in high-speed mode and medium-speed mode, data added and modified Table 5.15 to Table 5.19 added Figure 5.3 added
1.30	Dec 05, 2003	4 15	Table 1.2 : ** deleted Table 5.4 revised
1.30	Dec 05, 2003	15 16	Table 5.4 revised Figure 5.2 added

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