MB8171-55, MB8171-70

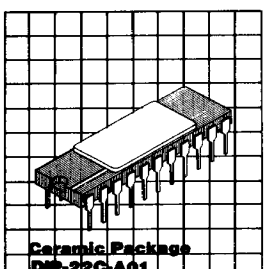
65,536-Bit Static Random Access Memory with Separate Data Input, Data Output and Automatic Power Down

Description

The Fujitsu MB8171 is a 65,536 word x 1-bit static random access memory fabricated with N-channel Silicon gate MOS technology. It uses fully static circuitry throughout and threrefore requires no clocks or refreshing to operate.

The MB8171 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.

All pins are TTL compatible and a single +5 volt power supply is required.



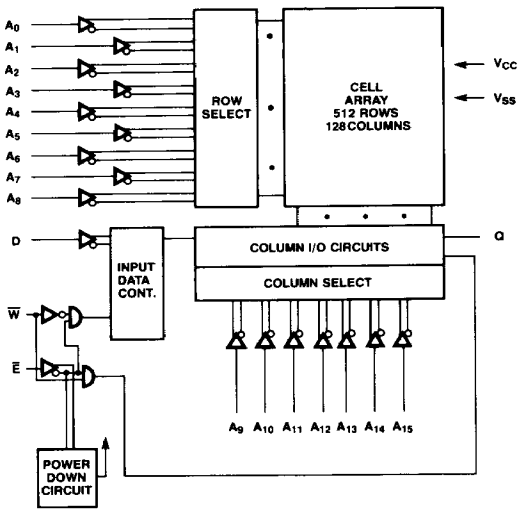
Ceramic Package
DIP-22C-A01

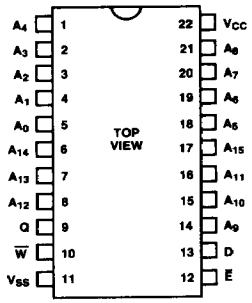
Features

- Organization: 65,536 words x 1-bit
- Static operation: no clocks or refresh required
- Fast access time: TAVQV = TELQV = 55 ns max. (MB8171-55) TAVQV = TELQV = 70 ns max. (MB8171-70)
- Single +5V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Chip enable for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- Standard 22-pin Ceramic package (300 mil.)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB8171 Block Diagram and Pin Assignments





TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	Q	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin with respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Temperature under bias	T_{BIAS}	−10 to +85	°C
Storage temperature	T_{STG}	−65 to +150	°C
Power dissipation	P_D	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−3.0**		0.8	V
Input high voltage	V_{IH}	2.0		6.0	V
Ambient temperature*	T_A	0		70	°C

Note: * The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/s.
** −3.0 V Min. Pulse width less than 20 ns. (V_{IL} Min. = −0.5 V at DC level)

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)*	C_{IN}		5	pF
$\overline{E}$ capacitance (V_{IN} = 0V)*	$C_{\overline{E}}$		9	pF
Output capacitance (V_{OUT} = 0V)*	C_{OUT}		6	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC} V_{CC} = max.		I_{LI}	−10	0.01	10	μA
Output leakage current	$\overline{E}$ = V_{IH}, V_{OUT} = 0V to 4.5V V_{CC} = max.		I_{LO}	−50	0.1	50	μA
Power supply current	$\overline{E}$ = V_{IL} V_{CC} = max. I_{OUT} = 0 mA	T_A = 25°C T_A = 0°C	I_{CC}		90	 125	mA
Standby current	V_{CC} = min. to max. $\overline{E}$ = V_{IH}		I_{SB}		27	35	mA
Output low voltage	I_{OL} = 16 mA		V_{OL}			0.45	V
Output high voltage	I_{OH} = −4 mA		V_{OH}	2.4			V
Peak power on current	V_{CC} = 0V to V_{CC} min.* $\overline{E}$ = lower of V_{CC} or V_{IH} min.		I_{PO}			40	mA

Note: * A pull-up resistor to V_{CC} on the $\overline{E}$ input is required to keep the device deselected. Otherwise, power-on current approaches I_{CC} active.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

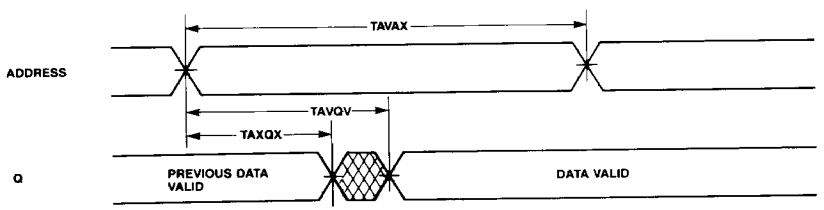
Read Cycle

Parameter	Symbol	MB8171-55 Min	MB8171-55 Max	MB8171-70 Min	MB8171-70 Max	Unit
Read cycle time	TAVAX	55		70		ns
Address access time	TAVQV		55		70	ns
Chip enable access time	TELQV		55		70	ns
Output hold from address change	TAXQX	5		5		ns
Chip enable to output in low-Z*1,2	TELQX	10		10		ns
Chip enable to output in high-Z*1,2	TEHQZ	0	30	0	40	ns
Chip enable to power up time	TELIH	0		0		ns
Chip enable to power down	TEHIL		30		35	ns

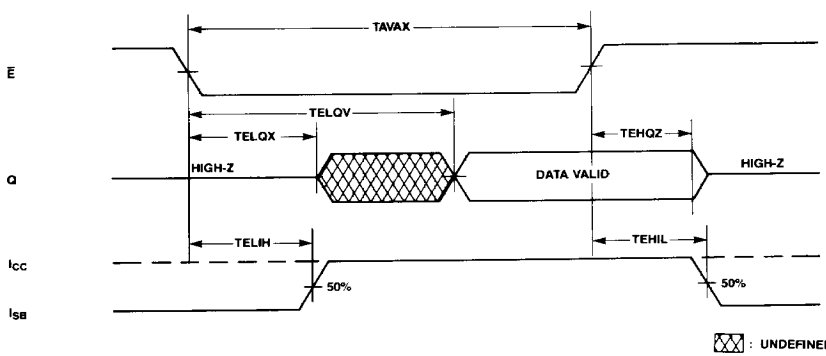
Notes: *1 Transition is measured at the point of ±500 mV from steady state voltage.

Read Cycle Timing Diagrams

Read Cycle: Address Controlled[*1 *2]



Read Cycle: $\overline{E}$ Controlled[*2 *3]



NOTES: *1 $\overline{E}$ IS LOW.
*2 $\overline{W}$ IS HIGH TO READ CYCLES.
*3 ADDRESS VALID PRIOR TO OR COINCIDENT WITH $\overline{E}$ TRANSITION LOW.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

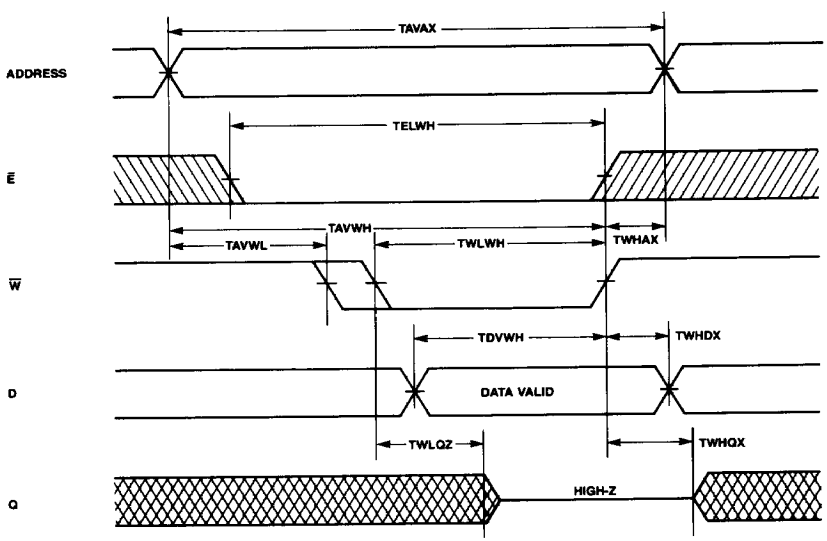
Write Cycle

Parameter	Symbol	MB8171-55 Min	MB8171-55 Max	MB8171-70 Min	MB8171-70 Max	Unit
Write cycle time	TAVAX	55		70		ns
Chip enable to end of write	TELWH	45		55		ns
Address valid to end of write	TAVWH	45		55		ns
Address setup time	TAVWL	5		10		ns
Address setup time	TAVEL	0		0		ns
Write pulse width	TWLWH	35		45		ns
Data valid to end of write	TDVWH	35		45		ns
Write recovery time	TWHAX	5		10		ns
Write recovery time	TEHAX	10		15		ns
Data hold time	TWHDX	0		0		ns
Data hold time	TEHDX	5		5		ns
Write enable to output in high-Z*1,2	TWLQZ	0	30	0	35	ns
Output active from end of write*1,2	TWHQX	0		0		ns

Notes: *1 Transition is measured at the point of ±500 mV from steady state voltage.

Write Cycle Timing Diagrams

Write Cycle: $\overline{W}$ Controlled*1 *2



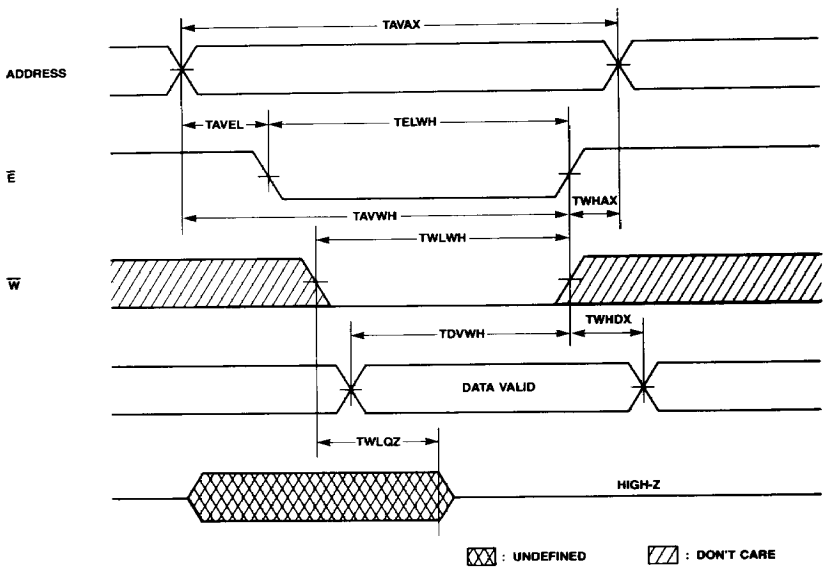
NOTES: *1 Ē OR W MUST BE HIGH DURING ADDRESS TRANSITIONS.
*2 IF Ē GOES HIGH SIMULTANEOUSLY WITH W̄ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.

: UNDEFINED

AC Characteristics
(continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagram

Write Cycle: $\overline{E}$ Controlled[*1]

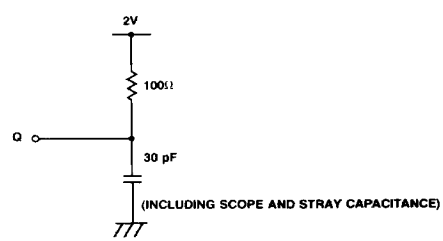


NOTES: *1 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

AC Test Conditions

Input pulse levels:	0.8V to 2.2V
Input pulse rise and fall times:	5 ns
Timing measurement reference levels:	Input: 1.5V
	Output: 1.5V

Output Load:



Package Dimensions
Dimensions in inches
(millimeters)

22-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-22C-A01)