TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

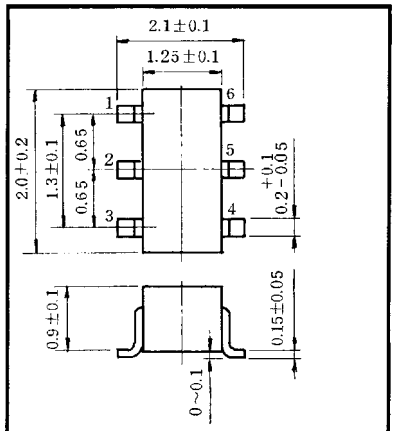
# S S M 6 P 0 5 F U

Power Management Switch

High Speed Switching Applications

- Small package
- Low on resistance : $R_{on}$ = 3.3 Ω (max) (@$V_{GS}$ = −4 V)
  : $R_{on}$ = 4.0 Ω (max) (@$V_{GS}$ = −2.5 V)
- Low gate threshold voltage

Unit in mm




1. SOURCE 1 4. SOURCE 2
2. GATE 1 5. GATE 2
3. DRAIN 2 6. DRAIN 1

| | |
|---|---|
| US6 | |
| JEDEC | — |
| EIAJ | — |
| TOSHIBA | 2-2J1C |

Weight : 6.8mg

## Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

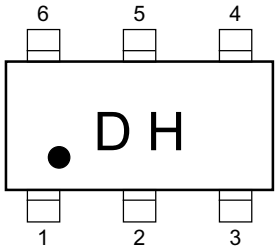
| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-Source voltage | | $V_{DS}$ | −20 | V |
| Gate-Source voltage | | $V_{GSS}$ | ±12 | V |
| Drain current | DC | $I_D$ | −200 | mA |
| | Pulse | $I_{DP}$ | −400 | |
| Drain power dissipation (Ta = 25°C) | | $P_D$ (Note1) | 300 | mW |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55~150 | °C |

Note1: Total rating, mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.32 $mm^2$ × 6)

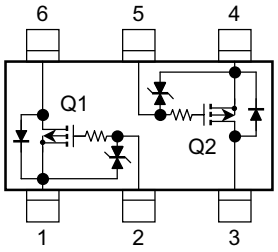
## Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

## Marking




## Equivalent Circuit (top view)



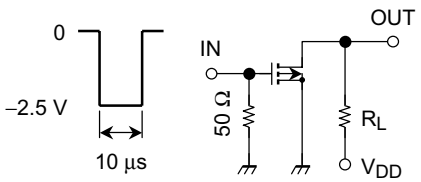

## Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±12 V, $V_{DS}$ = 0 | — | — | ±1 | μA |
| Drain-Source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = –1 mA, $V_{GS}$ = 0 | –20 | — | — | V |
| Drain cut-off current | | $I_{DSS}$ | $V_{DS}$ = –20 V, $V_{GS}$ = 0 | — | — | –1 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = –3 V, $I_D$ = –0.1 mA | –0.6 | — | –1.1 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = –3 V, $I_D$ = –50 mA (Note2) | 100 | — | — | mS |
| Drain-Source ON resistance | | $R_{DS\ (ON)}$ | $I_D$ = –100 mA, $V_{GS}$ = –4 V (Note2) | — | 2.1 | 3.3 | Ω |
| | | | $I_D$ = –50 mA, $V_{GS}$ = –2.5 V (Note2) | — | 3.2 | 4.0 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = –3 V, $V_{GS}$ = 0, f = 1 MHz | — | 27 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 7 | — | pF |
| Output capacitance | | $C_{oss}$ | | — | 21 | — | pF |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = –3 V, $I_D$ = –50 mA, | — | 70 | — | ns |
| | Turn-off time | $t_{off}$ | $V_{GS}$ = 0~–2.5 V | — | 70 | — | |

Note2: Pulse test

## Switching Time Test Circuit (Q1, Q2 common)

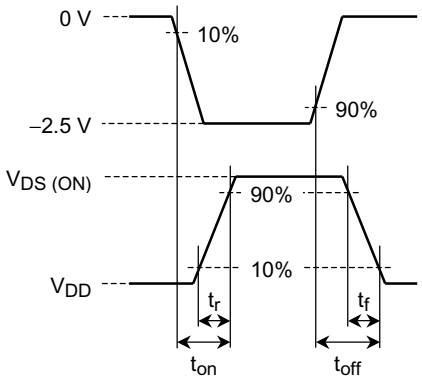
### (a) Test circuit




$V_{DD}$ = –3 V
Duty ≦ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
($Z_{out}$ = 50 Ω)
Common Source
Ta = 25°C

### (b) $V_{IN}$

### (c) $V_{OUT}$



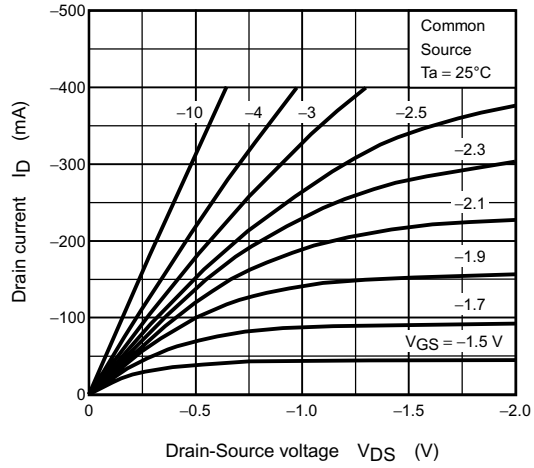

## Precaution

$V_{th}$ can be expressed as voltage between gate and source when low operating current value is $I_D$ = –100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires higher voltage than $V_{th}$ and $V_{GS\ (off)}$ requires lower voltage than $V_{th}$. (Relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$ )

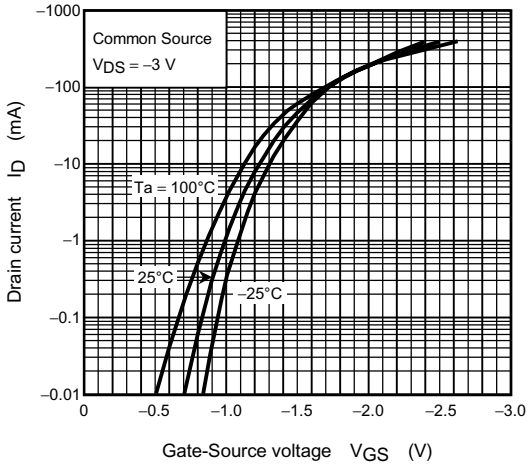
Please take this into consideration for using the device. $V_{GS}$ recommended voltage of –2.5 V or higher to turn on this product.

(Q1, Q2 common)

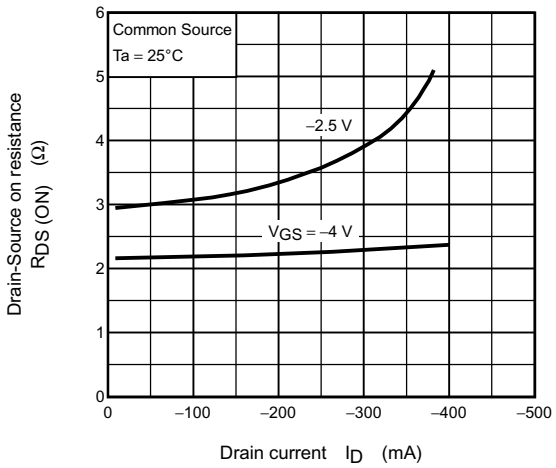
$I_D - V_{DS}$



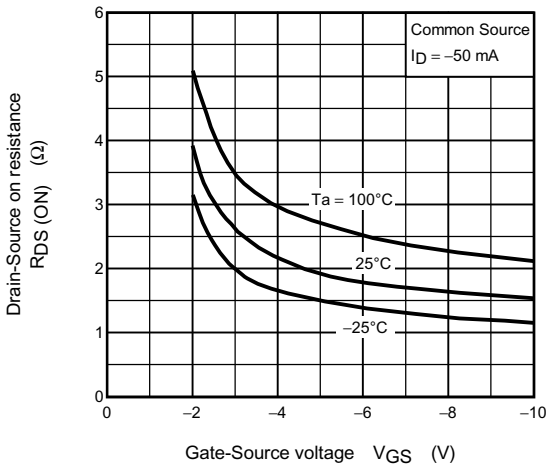

$I_D - V_{GS}$



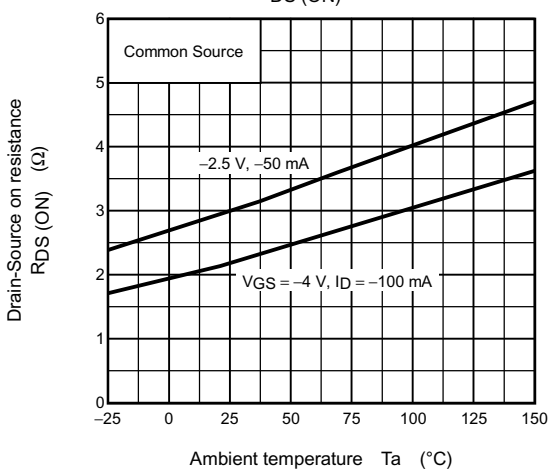

$R_{DS\ (ON)} - I_D$



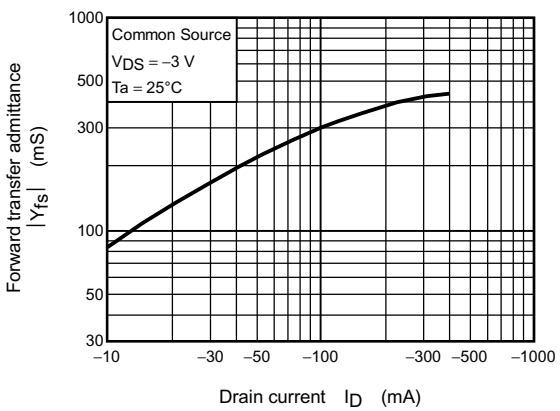

$R_{DS\ (ON)} - V_{GS}$




$R_{DS\ (ON)} - Ta$

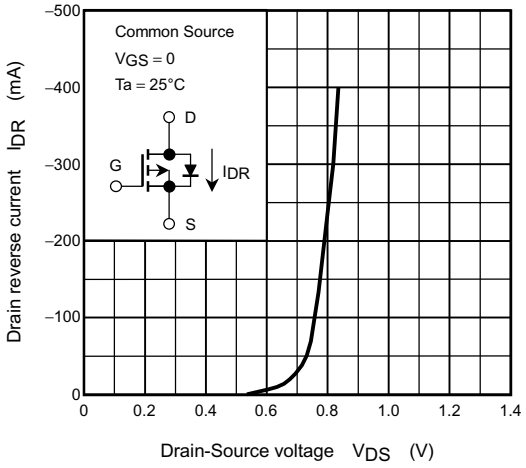



$|Y_{fs}| - I_D$

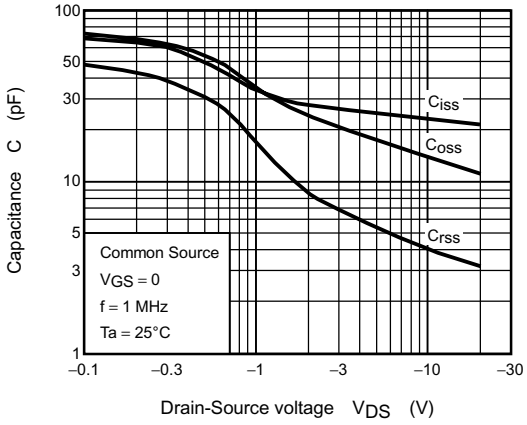


(Q1, Q2 common)

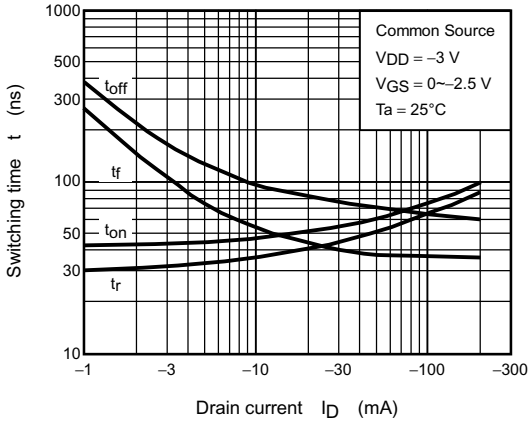
$I_{DR} - V_{DS}$



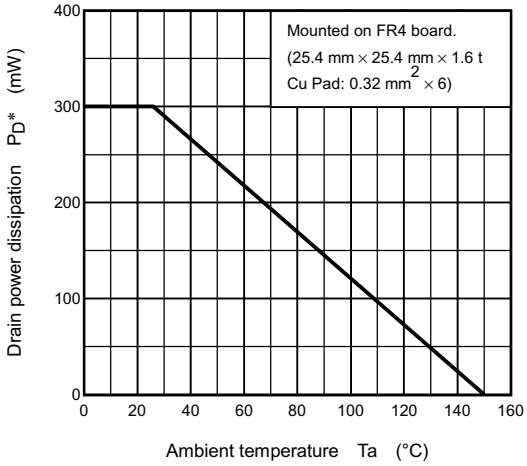

$C - V_{DS}$




$t - I_D$




$P_D^* - Ta$




*: Total rating