

# 4V Drive Pch+Pch MOS FET

## SP8J1

### ●Structure

Silicon P-channel MOS FET

### ●Features

- 1) Low On-resistance. (40mΩ at 4.5V)
- 2) High Power Package. ( $P_D=2.0W$ )
- 3) High speed switching.
- 4) Low voltage drive. (4 V)

### ●Applications

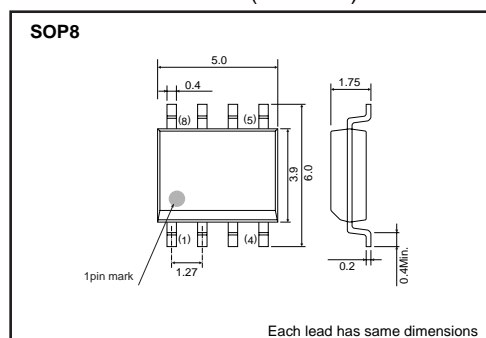
Power switching

DC-DC converter

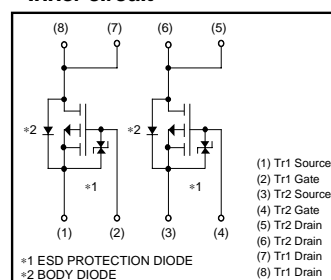
### ●Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8J1		○

### ●External dimensions (Unit : mm)



### ●Inner circuit



### ●Absolute maximum ratings ( $T_a=25^{\circ}C$ )

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit
Drain-source voltage	$V_{DS}$	-30	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Drain current	Continuous	$I_D$	A
	Pulsed	$I_{DP}$ *1	A
Source current (Body diode)	Continuous	$I_S$	A
	Pulsed	$I_{SP}$ *1	A
Total power dissipation	$P_D$ *2	2.0	W
Channel temperature	$T_{ch}$	150	$^{\circ}C$
Range of Storage temperature	$T_{stg}$	-55 to +150	$^{\circ}C$

\*1  $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$

\*2 Mounted on a ceramic board

### ●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}$ *	62.5	$^{\circ}C / W$

\* Mounted on a ceramic board.

## Transistors

## ●Electrical characteristics (Ta=25°C)

&lt;It is the same characteristics for Tr1 and Tr2.&gt;

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	—	—	$\pm 10$	$\mu A$	$V_{GS}=\pm 20V$ , $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -1mA$ , $V_{GS}=0V$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1	$\mu A$	$V_{DS} = -30V$ , $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	-1.0	—	-2.5	V	$V_{DS} = -10V$ , $I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	30	42	$m\Omega$	$I_D = -5.0A$ , $V_{GS} = -10V$
		—	40	56	$m\Omega$	$I_D = -2.5A$ , $V_{GS} = -4.5V$
		—	45	63	$m\Omega$	$I_D = -2.5A$ , $V_{GS} = -4.0V$
Forward transfer admittance	$ Y_{fs} $ *	4.5	—	—	S	$V_{DS} = -10V$ , $I_D = -2.5A$
Input capacitance	$C_{iss}$	—	1400	—	pF	$V_{DS} = -10V$
Output capacitance	$C_{oss}$	—	300	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	$C_{rss}$	—	230	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	15	—	ns	$I_D = -2.5A$
Rise time	$t_r$ *	—	30	—	ns	$V_{DD} = -15V$
Turn-off delay time	$t_{d(off)}$ *	—	80	—	ns	$V_{GS} = -10V$
Fall time	$t_f$ *	—	40	—	ns	$R_L=6\Omega$
Total gate charge	$Q_g$ *	—	16	—	nC	$V_{DD} = -15V$
Gate-source charge	$Q_{gs}$ *	—	3.5	—	nC	$V_{GS} = -5V$
Gate-drain charge	$Q_{gd}$ *	—	6.5	—	nC	$I_D = -5.0A$

\*Pulsed

## ●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	$V_{SD}$	—	—	-1.2	V	$I_S = -1.6A$ , $V_{GS}=0V$

## Transistors

## ●Electrical characteristic curves

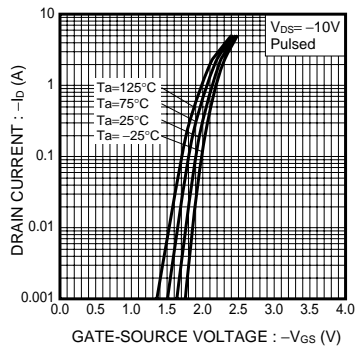


Fig.1 Typical Transfer Characteristics

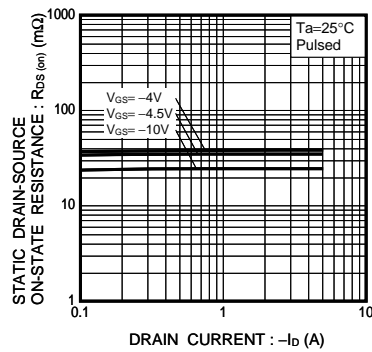


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

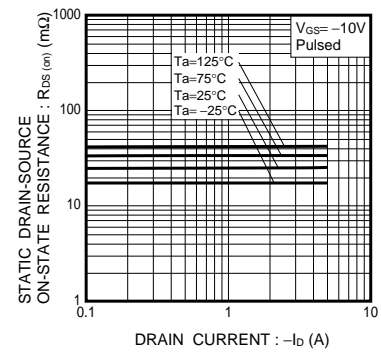


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

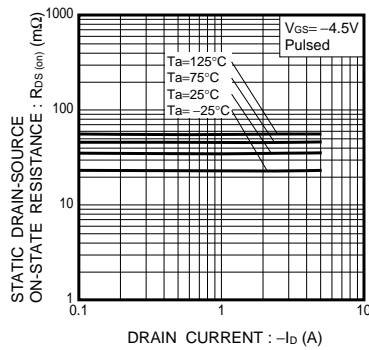


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

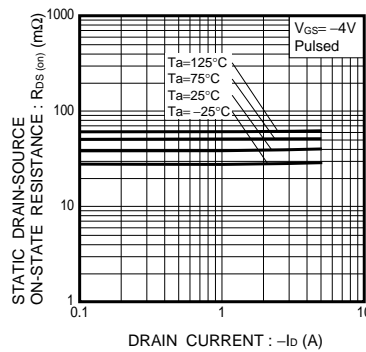


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

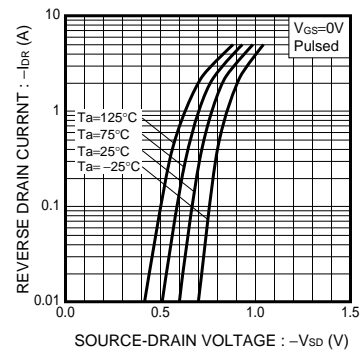


Fig.6 Reverse Drain Current Source-Drain Current

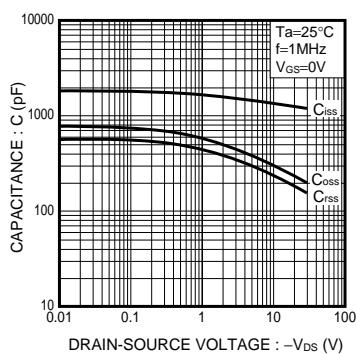


Fig.7 Typical Capacitance vs. Drain-Source Voltage

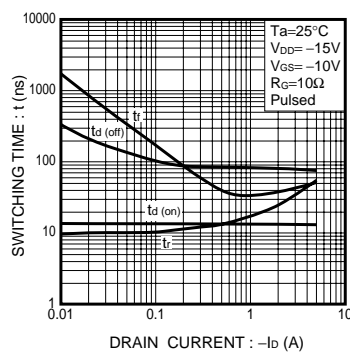


Fig.8 Switching Characteristics

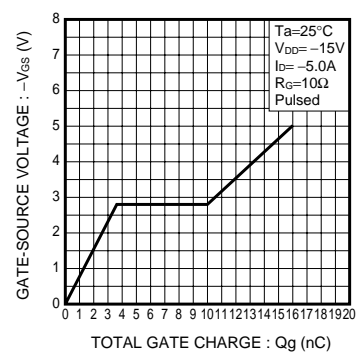


Fig.9 Dynamic Input Characteristics

## Transistors

### ●Measurement circuits

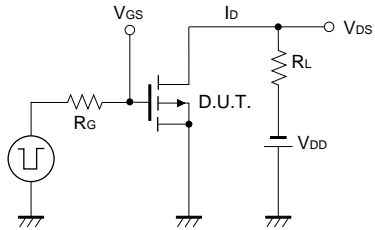


Fig.10 Switching Time Test Circuit

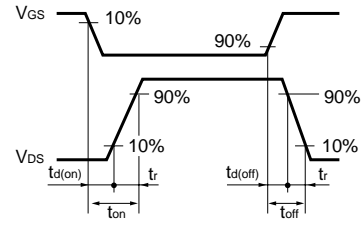


Fig.11 Switching Time Waveforms

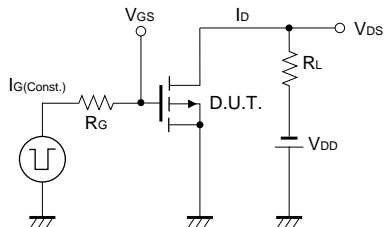


Fig.12 Gate Charge Test Circuit

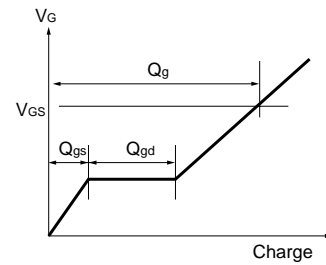


Fig.13 Gate Charge Waveform

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