

LOW EMI CURRENT SENSE HIGH SIDE SWITCH

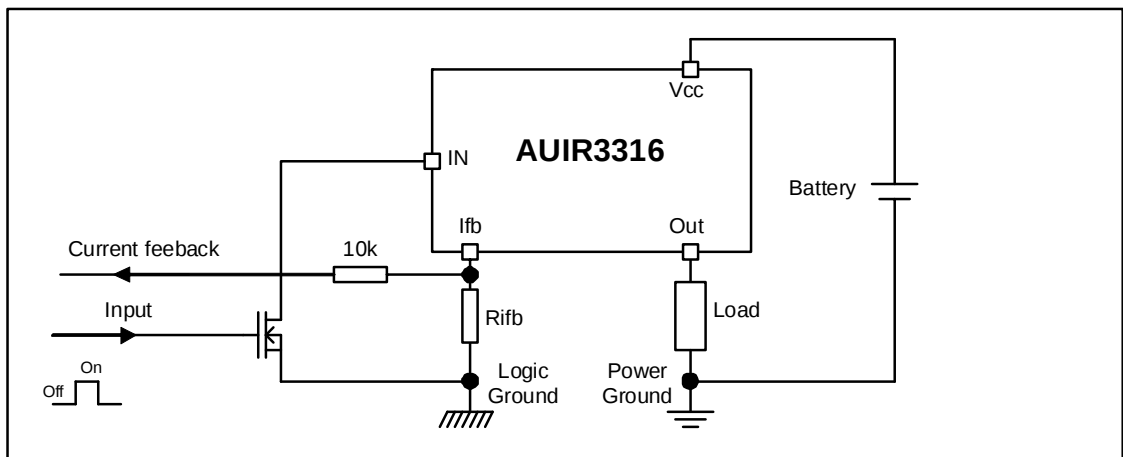
Features

- Load current feedback
- Programmable over current shutdown
- Active clamp
- ESD protection
- Input referenced to Vcc
- Over temperature shutdown
- Switching time optimized for low EMI
- Reverse battery protection

Description

The AUIR3316(S) is a fully protected 4 terminals high side switch. The input signal is referenced to Vcc. When the input voltage $V_{cc} - V_{in}$ is higher than the specified threshold, the output power Mosfet is turned on. When the $V_{cc} - V_{in}$ is lower than the specified V_{il} threshold, the output Mosfet is turned off. A current proportional to the power Mosfet current is sourced to the Ifb pin. Over current shutdown occurs when $V_{ifb} - V_{in} > 4.7V$. The current shutdown threshold is adjusted by selecting the proper R_{ifb}. Either over current and over temperature latches off the switch. The device is reset by pulling the input pin high. Other integrated protections (ESD, reverse battery, active clamp) make the switch very rugged in automotive environment.

Typical Connection



Product Summary

Rds(on)	7 mΩ max.
Vcc op.	6 to 26V
Current Ratio	8800
Prog. Ishutdown	10 to 90A
Vclamp	40V

Packages



TO-220
AUIR3316



D²Pak
Pin 4 and 5 fused
AUIR3316S

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q100 ^{††})	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D2PAK-5L	MSL1, 260°C (per IPC/JEDEC J-STD-020)
		TO220-5L	Not applicable
ESD	Machine Model	Class M4 (450V) (per AEC-Q100-003)	
	Human Body Model	Class H3A (4,500 V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (1000 V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

^{††} Exceptions to AEC-Q100 requirements are noted in the qualification report.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to Vcc lead. (Tj=-40°..150°C, Vcc=6..26V Tambient=25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units
Vcc-Vin	Maximum Vcc voltage	-16	37	V
Vcc-Vin cont.	Maximum continuous Vcc voltage	-16	26	
Vcc-Vfb	Maximum lfb voltage	-16	33	
Vcc-Vout	Maximum output voltage	-0.3	37	
Ids cont.	Maximum body diode continuous current Rth=60°C/W (1) Tambient=25°C	—	2.8	A
Ids pulsed	Maximum body diode pulsed current (1)	—	100	
Pd	Maximum power dissipation Rth=60°C/W Tambient=25°C	—	2	W
Tj max.	Max. storage & operating temperature junction temperature	-40	150	°C
Min Rfb	Minimum on the resistor on lfb pin	0.3	—	kΩ
lfb max.	Max. lfb current	-50	50	mA

(1) Limited by junction temperature. Pulsed is also limited by wiring

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
Rth1	Thermal resistance junction to ambient D ² -Pak Std footprint	60	—	°C/W
Rth2	Thermal resistance junction to case D ² -Pak	0.7	—	
Rth2	Thermal resistance junction to case TO220	0.7	—	

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
Iout	Continuous output current	—	23 7	A
	Tambient=85°C, Rth=5°C/W, Tj=125°C			
	Tambient=85°C, Rth=60°C/W, Tj=125°C			
Rifb	Recommended lfb resistor (2)(3)	0.5	3.5	kΩ
Pulse min.	Minimum turn-on pulse width	1	—	ms
Fmax.	Maximum operating frequency	—	200	Hz

(2) If Rifb is too low, the device can be damaged.

(3) If Rifb is too high, the device may not switch on.

Protection Characteristics

 $T_j = -40^{\circ}\text{C} \dots 150^{\circ}\text{C}$, $V_{cc} = 6 \dots 26\text{V}$, $R_{ifb} = 500 \text{ to } 5\text{k}\Omega$

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{fb-Vin@I_{sd}}	Over-current shutdown threshold	3.8	4.7	5.9	V	
T _{sd}	Over temperature threshold	—	165	—	°C	See fig. 5
OV	Over voltage protection (not latched)	26	29	33	V	
I _{sdf}	Fixed over current shutdown	90	120	150	A	V _{fb} <V _{fb-Vin@I_{sd}}
I _{sd_1k}	Programmable over current shutdown 1k	30	40	53		R _{ifb} =1kΩ
t _{reset}	Time to reset protection	—	50	500	μs	See fig. 5
Min. pulse	Min. pulse width (no WAIT state)	—	900	2000		T _j =25°C
WAIT	WAIT function timer	0.4	1	2	ms	See fig. 4 and 5
R _{ds(on) rev.}	Reverse battery On state resistance, T _j =25°C	4	6.7	10	mΩ	V _{cc-Vin} =-14V, I _{out} =30A
	T _j =125°C	—	10	15		

Static Electrical Characteristics

 $T_j = -40^{\circ}\text{C} \dots 150^{\circ}\text{C}$, $V_{cc} = 6 \dots 26\text{V}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{cc op.}	Operating Voltage range	6	—	26	V	
I _{cc off}	Supply leakage current	—	1.5	5	μA	V _{in} =V _{cc} , V _{cc-Vout} =14V, V _{cc-Vifb} =14V, T _j =25°C
I _{in, on}	On state I _N positive current	1.5	3	6	mA	V _{cc-Vin} =14V, T _j =25°C
V _{ih}	High level Input threshold voltage (4)	—	5.4	6.3	V	
V _{il}	Low level Input threshold voltage (4)	4	4.9	5.8		
V _{hyst}	Input hysteresis V _{ih} -V _{il}	0.2	0.4	1.5		
I _{out}	Drain to source leakage current	—	1.2	5	μA	V _{in} =V _{cc} , V _{cc-Vifb} =0V, V _{cc-Vout} =14V, T _j =25°C
R _{ds(on)}	On state resistance (5) T _j =25°C	4	5.5	7	mΩ	I _{out} =30A, V _{cc-Vin} =14V
	On state resistance (5) T _j =25°C	4	6	10		I _{out} =17A, V _{cc-Vin} =6V
	On state resistance (5)(6) T _j =150°C	7	10.5	13.5		I _{out} =30A, V _{cc-Vin} =14V
V _{clamp1}	V _{cc} to V _{out} clamp voltage 1	36	39	—	V	I _{out} =50mA
V _{clamp2}	V _{cc} to V _{out} clamp voltage 2	—	40	43		I _{out} =30A, T _j =25°C

(4) Input thresholds are measured directly between the input pin and the tab. Any parasitic resistance in common between the load current path and the input signal path can significantly affect the thresholds.

(5) R_{ds(on)} is measured between the tab and the Out pin, 5mm away from the package.

(6) Guaranteed by design

Switching Electrical Characteristics

 $V_{cc} = 14\text{V}$, Resistive load=0.5Ω, T_j=25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
tdon	Turn on delay time to 10% Vcc	30	120	300	μs	See figure 2
tr1	Rise time to Vcc-Vout=5V	20	50	125		
tr2	Rise time to Vcc-Vout=0.1Vcc	30	80	200		
Eon	Turn on energy	—	14	—	mJ	
tdoff	Turn off delay time	30	140	350	μs	
tf	Fall time to Vout=10% of Vcc	35	100	250		
Eoff	Turn off energy	—	7	—	mJ	

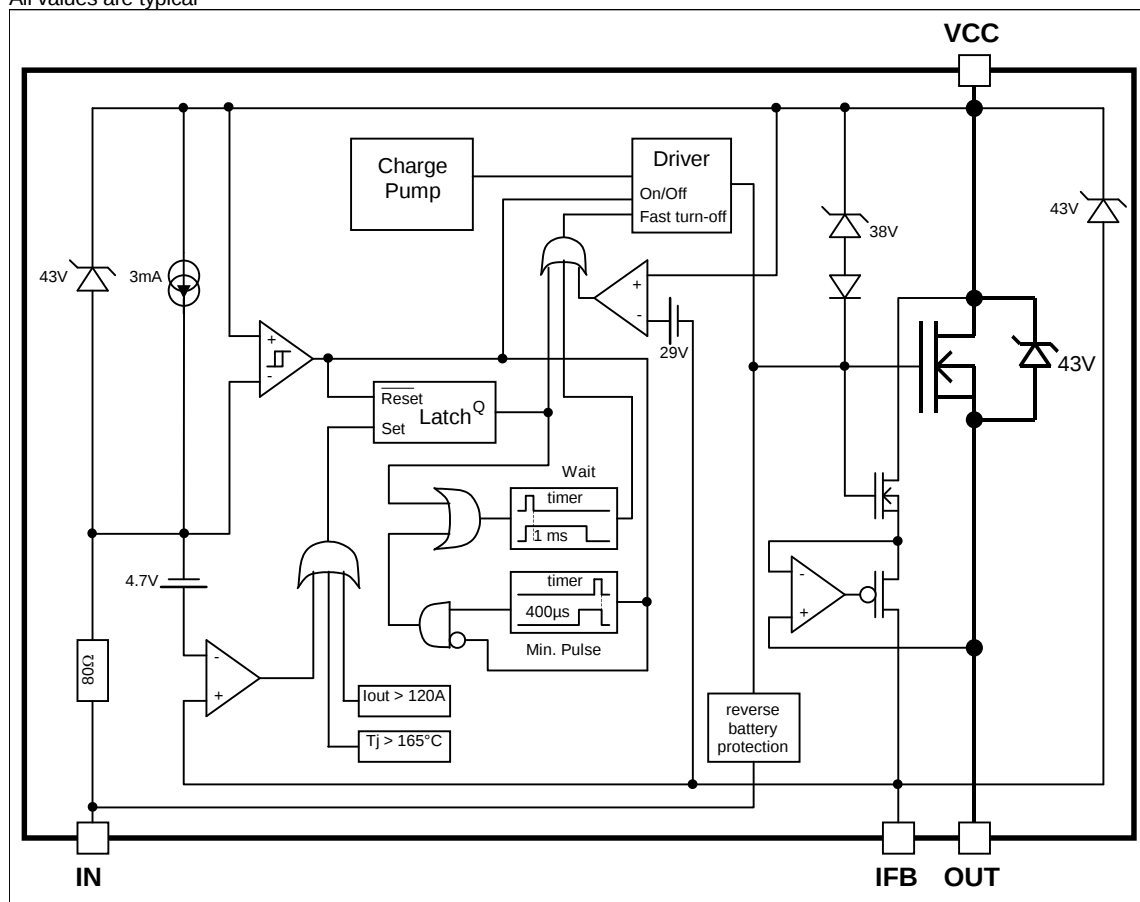
Current Sense Characteristics

$T_j = -40^{\circ}\text{C}..150^{\circ}\text{C}$, $V_{cc} = 6..26\text{V}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ratio	I Load/I _{fb} current ratio	8,200	8,800	9,950	—	R _{fb} =500Ω, I _{out} =60A
Ratio_TC	I Load/I _{fb} variation aver temperature(6)	-5	—	+5	%	T _j =-40°C to 150°C
Offset	Load current diagnostic offset	-0.2	0	+0.25	A	I _{out} =2A
trst	I _{fb} response time (low signal)	—	1	—	μs	90% of the I _{out} step

Functional Block Diagram

All values are typical



Lead Assignments

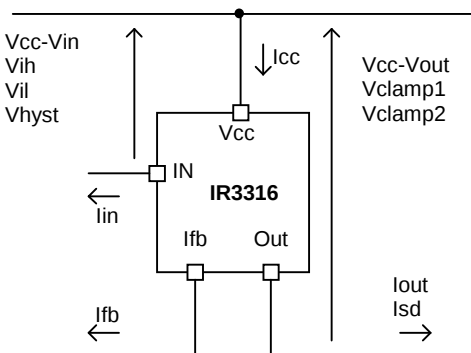
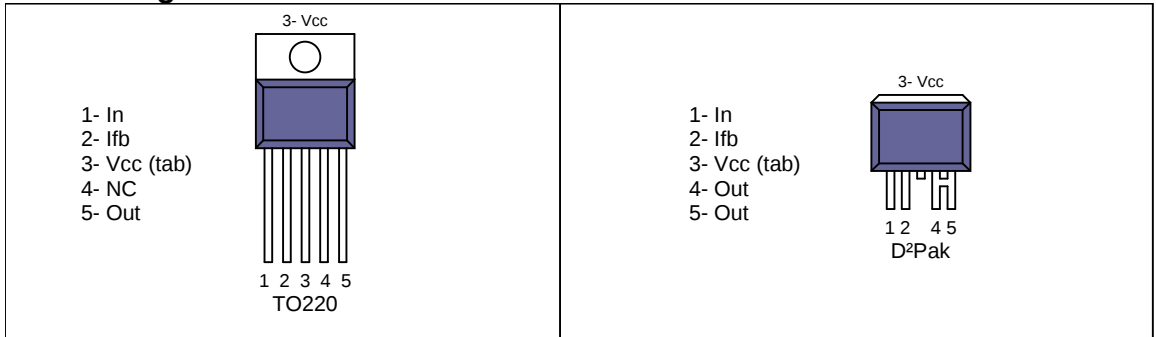


Figure 1 – Voltages and current definitions

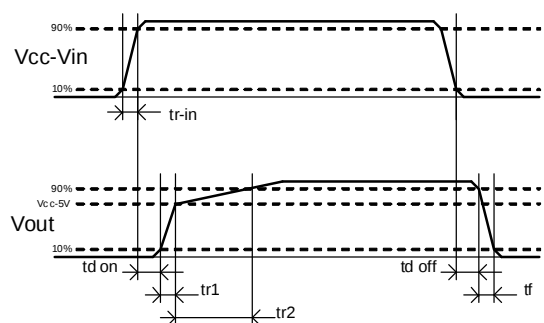


Figure 2 – Switching time definitions

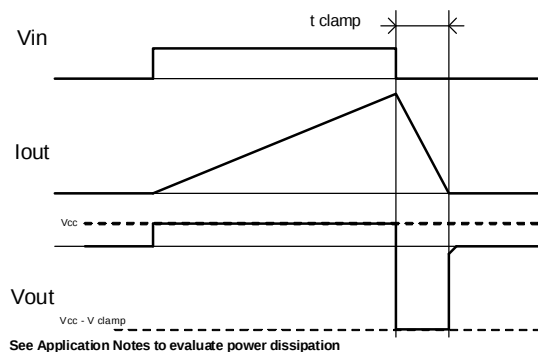


Figure 3 – Active clamp waveforms

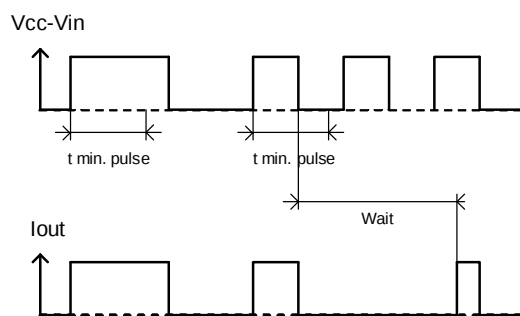


Figure 4 – Min. pulse and Wait function

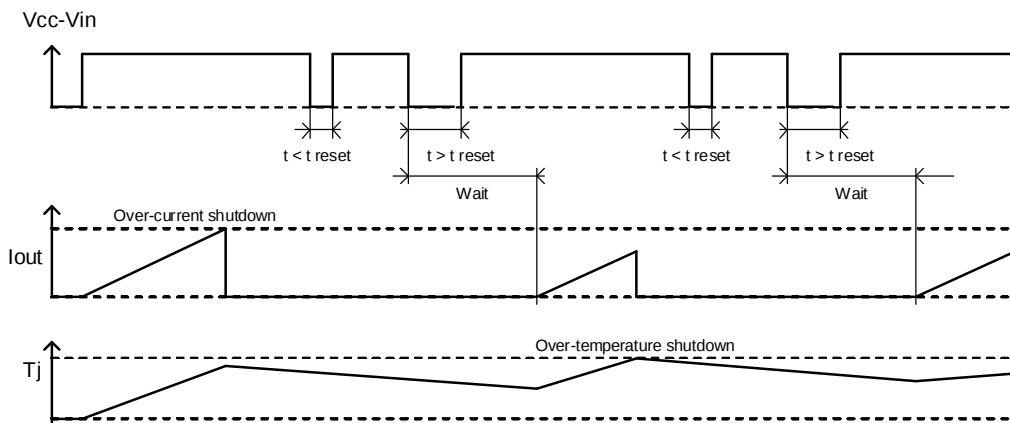


Figure 5 – Protection Timing Diagrams

All curves are typical characteristics. Operation in hatched areas is not recommended. $T_j=25^{\circ}\text{C}$, $R_{\text{fcb}}=500\Omega$, $V_{\text{cc}}=14\text{V}$ (unless otherwise specified).

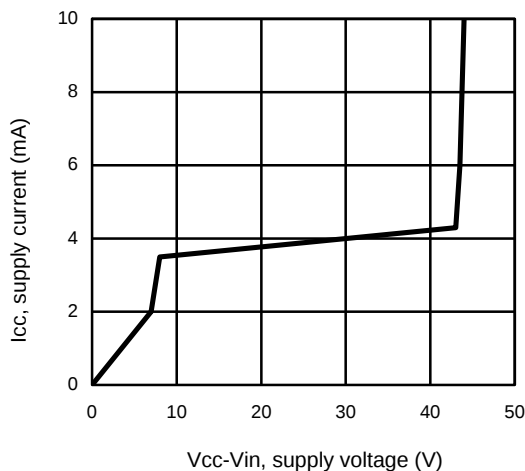


Figure 6 – Icc (mA) Vs Vcc-Vin (V)

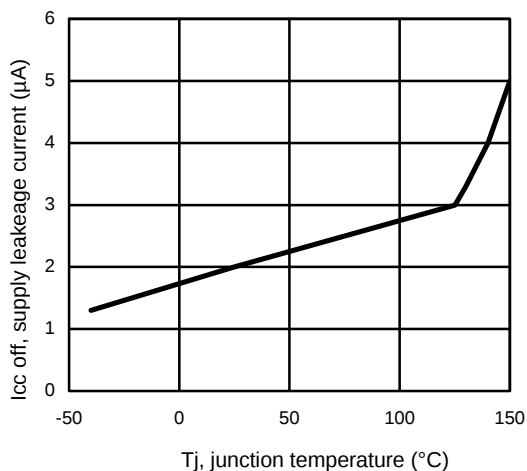


Figure 7 – Icc off (µA) Vs Tj (°C)

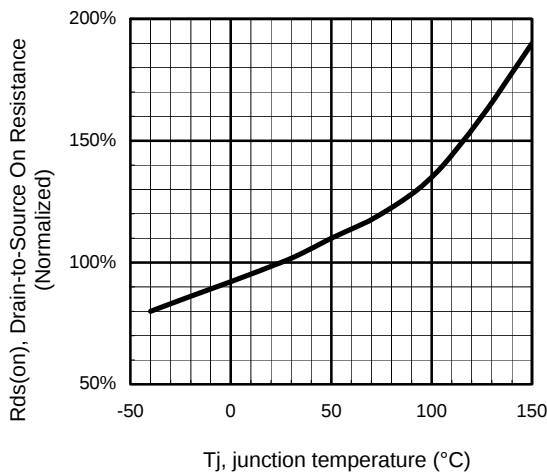


Figure 8 - Normalized Rds(on) (%) Vs Tj (°C)

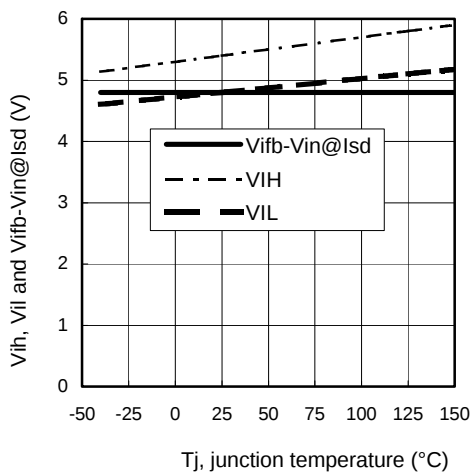


Figure 9 – Vih, Vil and Vifb-Vin@Isd (V) Vs Tj (°C)

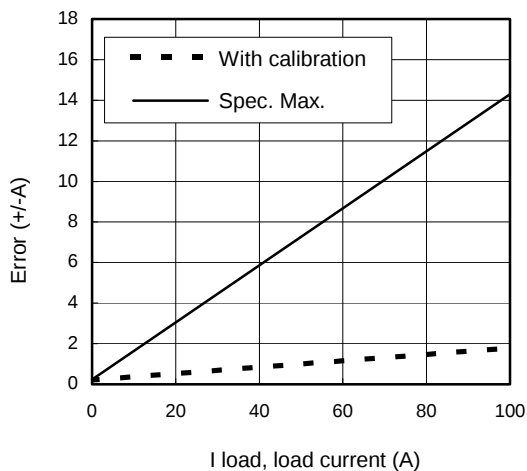


Figure 10 – Error (+/- A) Vs I load (A)

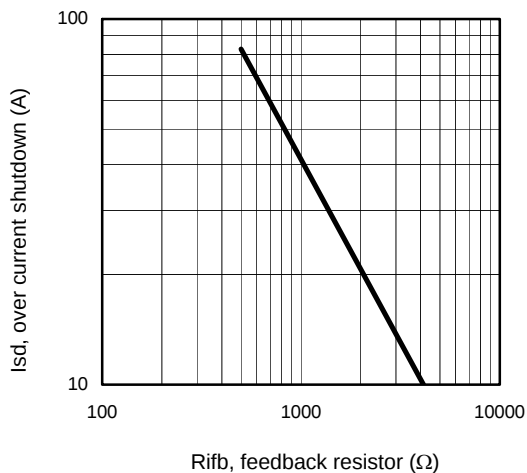


Figure 11 – Ids (A) Vs Rifb (Ω)

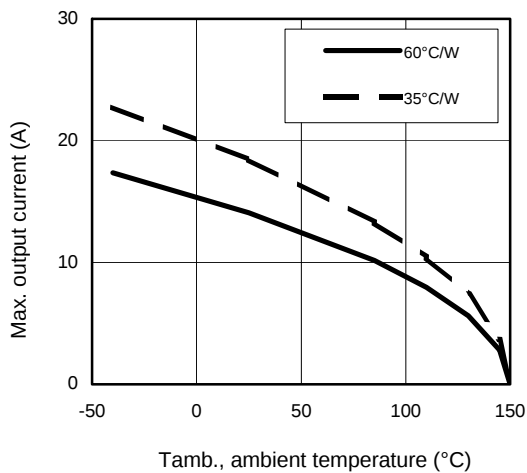


Figure 12 – Max. iout (A) Vs Tamb. (°C)

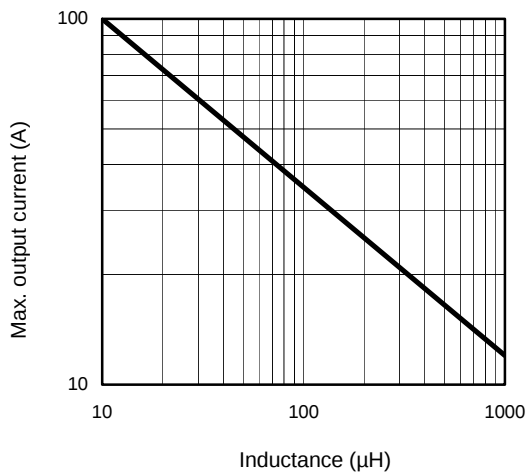


Figure 13 – Max. iout (A) Vs inductance (μH)

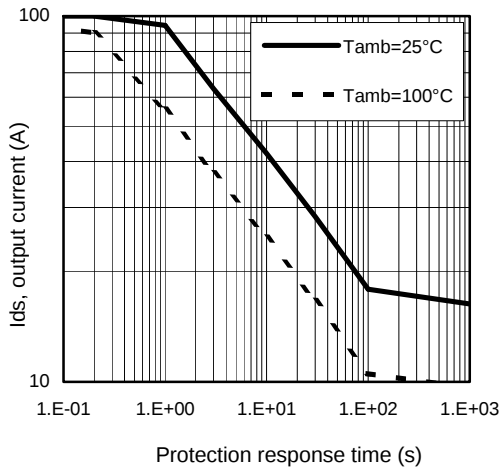


Figure 14 – Ids (A) Vs over temperature protection response time (s)

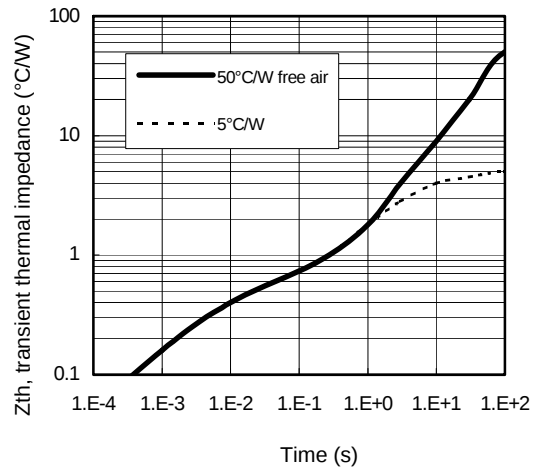
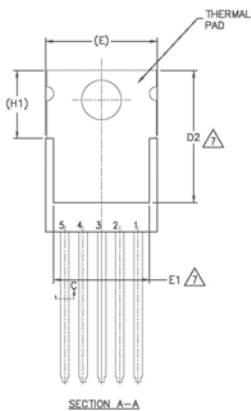
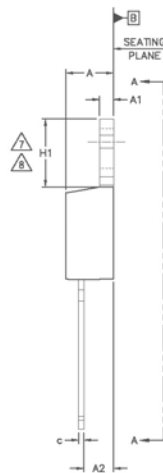
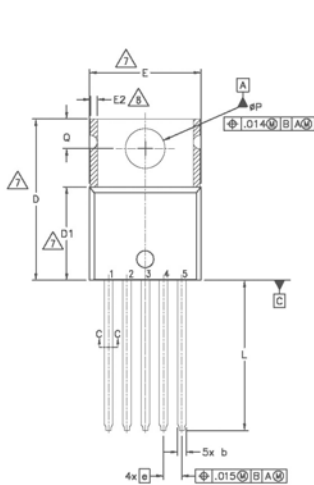


Figure 15 – Transient thermal impedance (°C/W) Vs time (s)

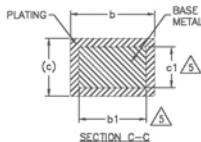
Case Outline - TO220 - 5 Leads



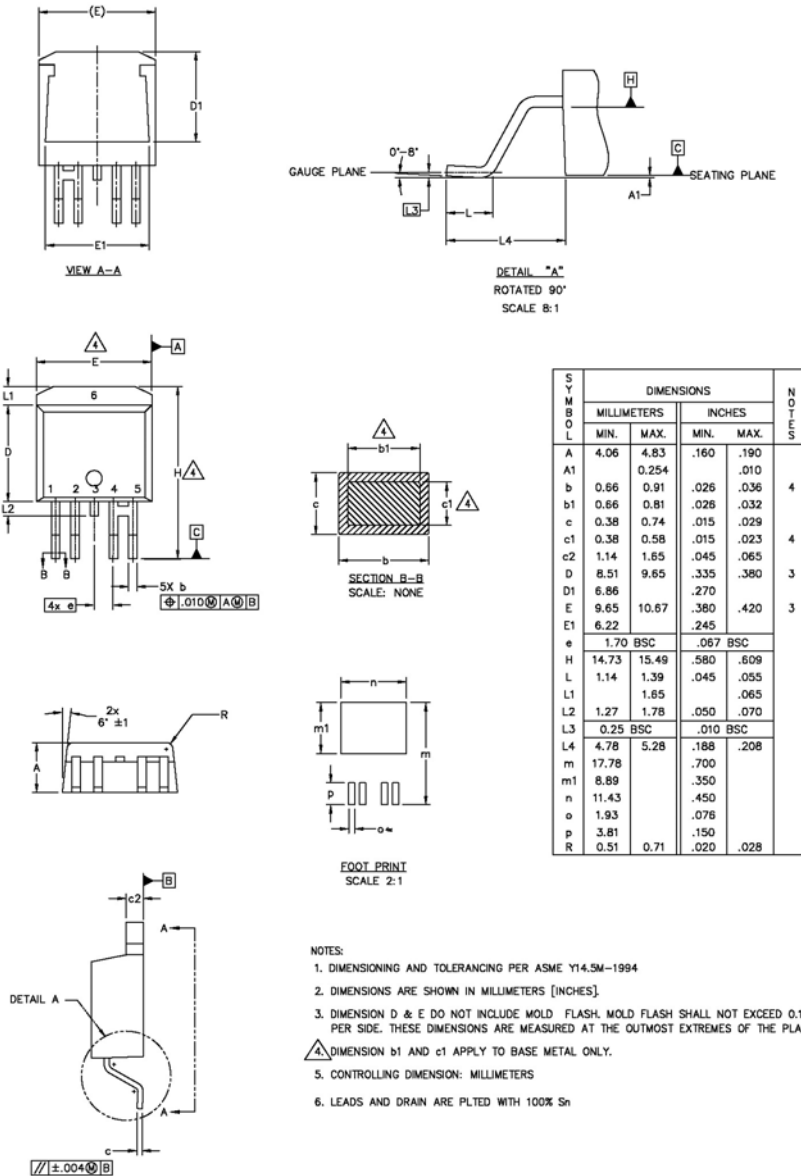
L O U S E - 0 1	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	5
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.64	0.89	.025	.035	
b1	0.64	0.84	.025	.033	
c	0.36	0.61	.014	.024	4
c1	0.36	0.56	.014	.022	
D	14.22	16.51	.560	.650	7
D1	8.38	9.02	.330	.355	
D2	12.88	14.68	.507	.577	4, 7
E	9.65	10.67	.380	.420	
E1	6.86	8.89	.270	.350	7
E2	—	0.76	—	.030	
e	1.70 BSC		.067 BSC		7, 8
H1	5.84	6.86	.230	.270	
L	12.70	14.73	.500	.580	
φP	3.53	3.73	.139	.147	
Q	2.54	3.05	.100	.120	

NOTES:

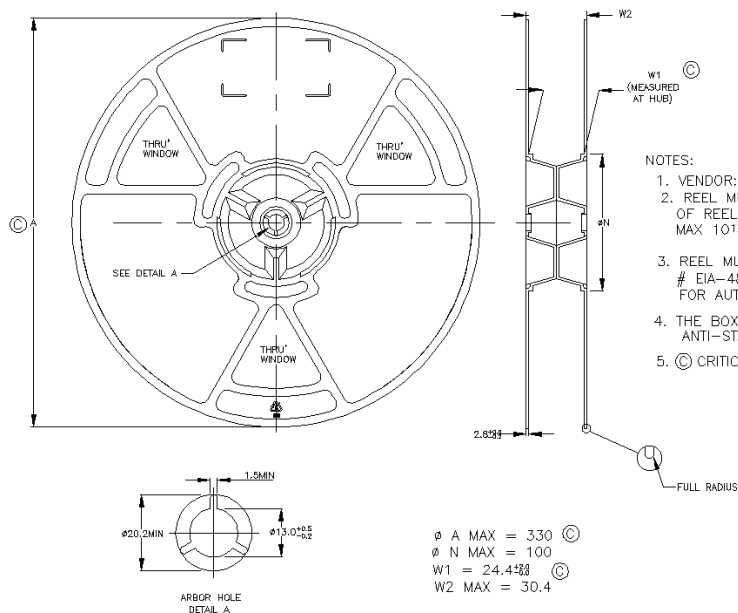
- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1.
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.
- 10.- LEADS AND DRAIN ARE PLATED WITH 100% Sn



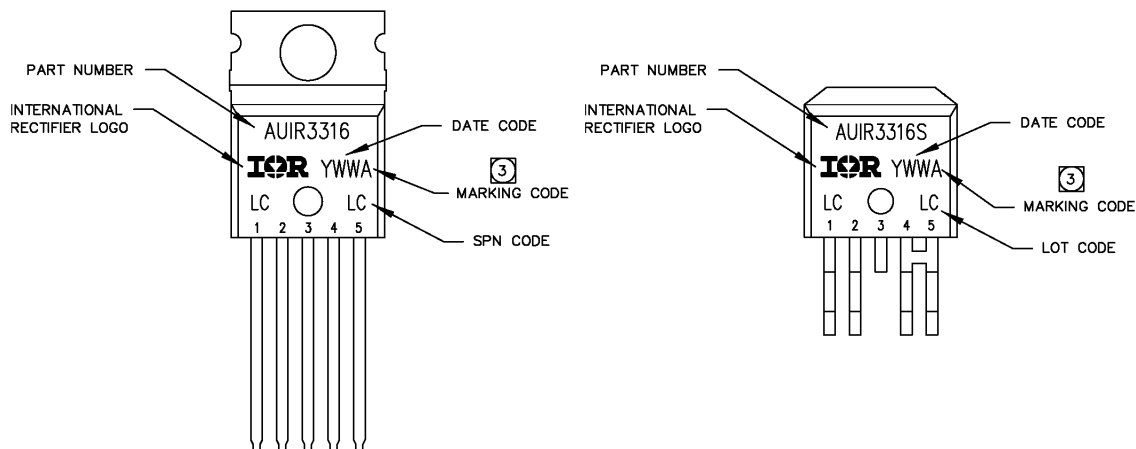
Case Outline - D2PAK - 5 Leads



Tape & Reel - D2PAK – 5 leads



Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIR3316	TO220 – 5Leads	Tube	50	AUIR3316
	D2-Pak-5-Leads	Tube	50	AUIR3316S
		Tape and reel left	800	AUIR3316STRL
		Tape and reel right	800	AUIR3316STRR

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For technical support, please contact IR's Technical Assistance Center

<http://www.irf.com/technical-info/>

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Revision History

Revision	Date	Notes/Changes
A	01/09/2006	First release
B	22/01/2007	Pbf release
C	16/04/2008	TO220 release
D	14/12/2009	AU release
E	14/11/2010	Change description