CY7C1347C/GVT71128DA36
CY7C1327C/GVT71256DA18

256K x 18/128K x 36 Synchronous-Pipelined Cache RAM

Features

- **Fast access times: 2.5 and 3.5 ns**
- **Fast clock speed: 250, 225, 200, and 166 MHz**
- **1-ns set-up time and hold time**
- **Fast OE access times: 2.5 ns and 3.5 ns**
- **Optimal for depth expansion (one cycle chip deselect to eliminate bus contention)**
- **3.3V –5% and +10% power supply**
- **3.3V or 2.5V I/O supply**
- **5V tolerant inputs except I/Os**
- **Clamp diodes to V_{SS} at all inputs and outputs**
- **Common data inputs and data outputs**
- **Byte Write Enable and Global Write control**
- **Three chip enables for depth expansion and address pipeline**
- **Address, data, and control registers**
- **Internally self-timed Write Cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down for portable applications**
- **JTAG boundary scan**
- **JEDEC standard pinout**
- **Low profile 119-lead, 14-mm x 22-mm BGA (Ball Grid Array) and 100-pin TQFP packages**

Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1347C/GVT71128DA36 and CYC7C1327C/GVT71256DA18 SRAMs integrate 131,072x36 and 262,144x18 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable (CE), depth-expansion Chip Enables (CE2 and CE2), Burst Control Inputs (ADSC, ADSP, and ADV), Write Enables (BWa, BWb, BWc, BWd, and BWE), and Global Write (GW).

Asynchronous inputs include the Output Enable (OE) and Burst Mode Control (MODE). The data outputs (Q), enabled by OE, are also asynchronous.

Addresses and chip enables are registered with either Address Status Processor (ADSP) or Address Status Controller (ADSC) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin (ADV).

Address, data inputs, and write controls are registered on-chip to initiate self-timed Write cycle. Write cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. BWa controls DQa. BWb controls DQb. BWc controls DQc. BWd controls DQd. BWa, BWb, BWc, and BWd can be active only with BWE being LOW. GW being LOW causes all bytes to be written. The x18 version only has 18 data inputs/outputs (DQa and DQb) along with BWa and BWb (no BWc, BWd, DQc, and DQd).

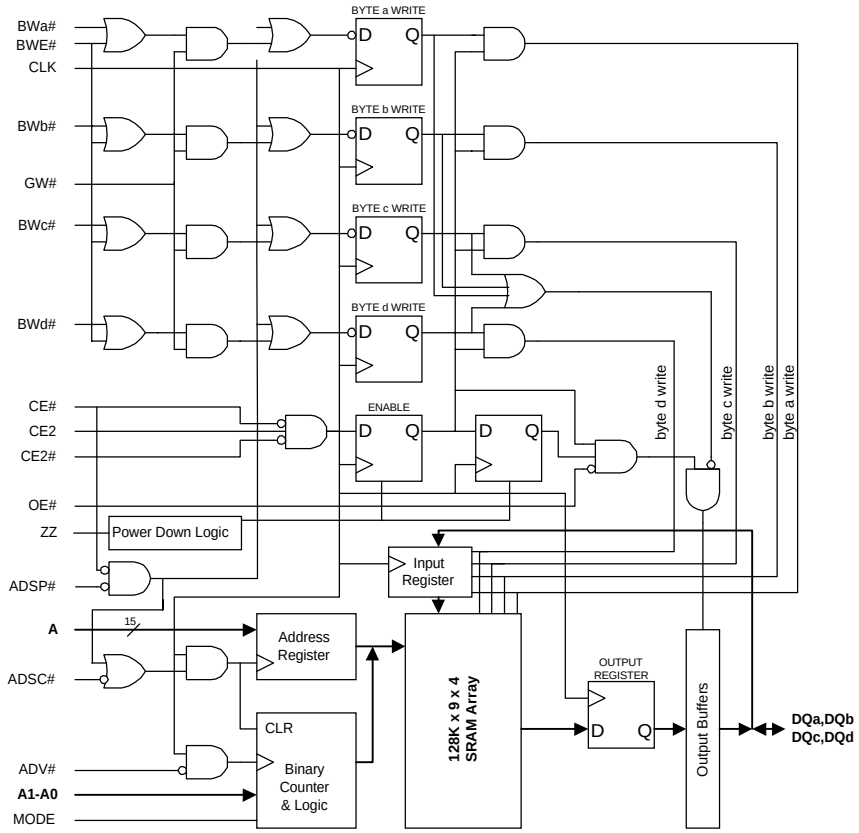
Four pins are used to implement JTAG test capabilities: Test Mode Select (TMS), Test Data-in (TDI), Test Clock (TCK), and Test Data-out (TDO). The JTAG circuitry is used to serially shift data to and from the device. JTAG inputs use LVTTL/LVCMOS levels to shift data during this testing mode of operation.

The CY7C1347C/GVT71128DA36 and CY7C1327C/GVT71256DA18 operate from a +3.3V power supply. All inputs and outputs are LVTTL compatible

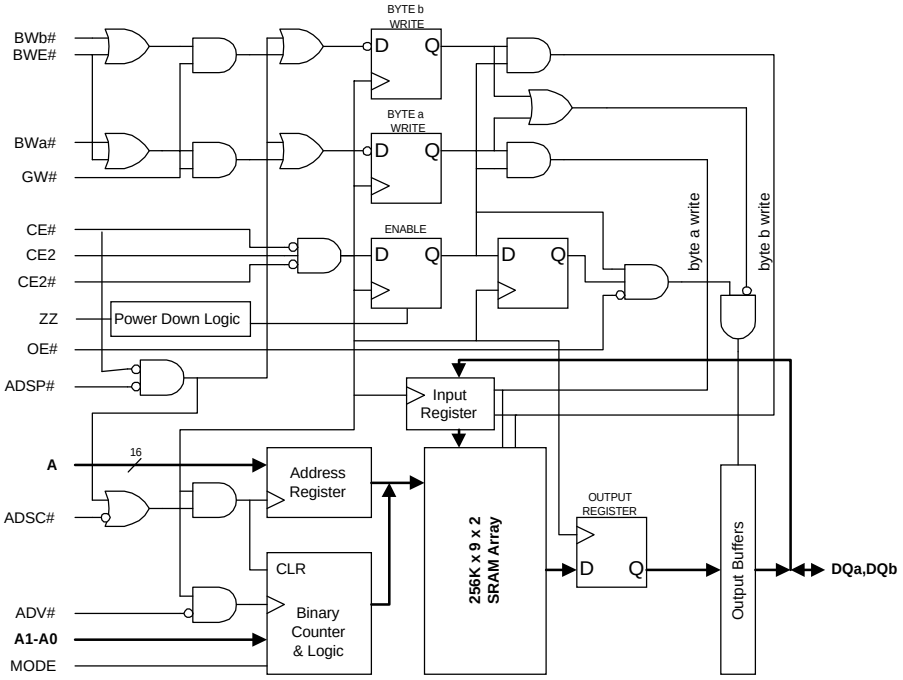
Selection Guide

	7C1347C-250 71128DA36-4 7C1327C-250 71256DA18-4	**7C1347C-225 71128DA36-4.4 7C1327C-225 71256DA18-4.4**	**7C1347C-200 71128DA36-5 7C1327C-200 71256DA18-5**	**7C1347C-166 71128DA36-6 7C1327C-166 71256DA18-6**
Maximum Access Time (ns)	2.5	2.5	2.5	3.5
Maximum Operating Current (mA)	450	400	360	300
Maximum CMOS Standby Current (mA)	10	10	10	10

Functional Block Diagram—128Kx36[1]



Functional Block Diagram—256Kx18[1]

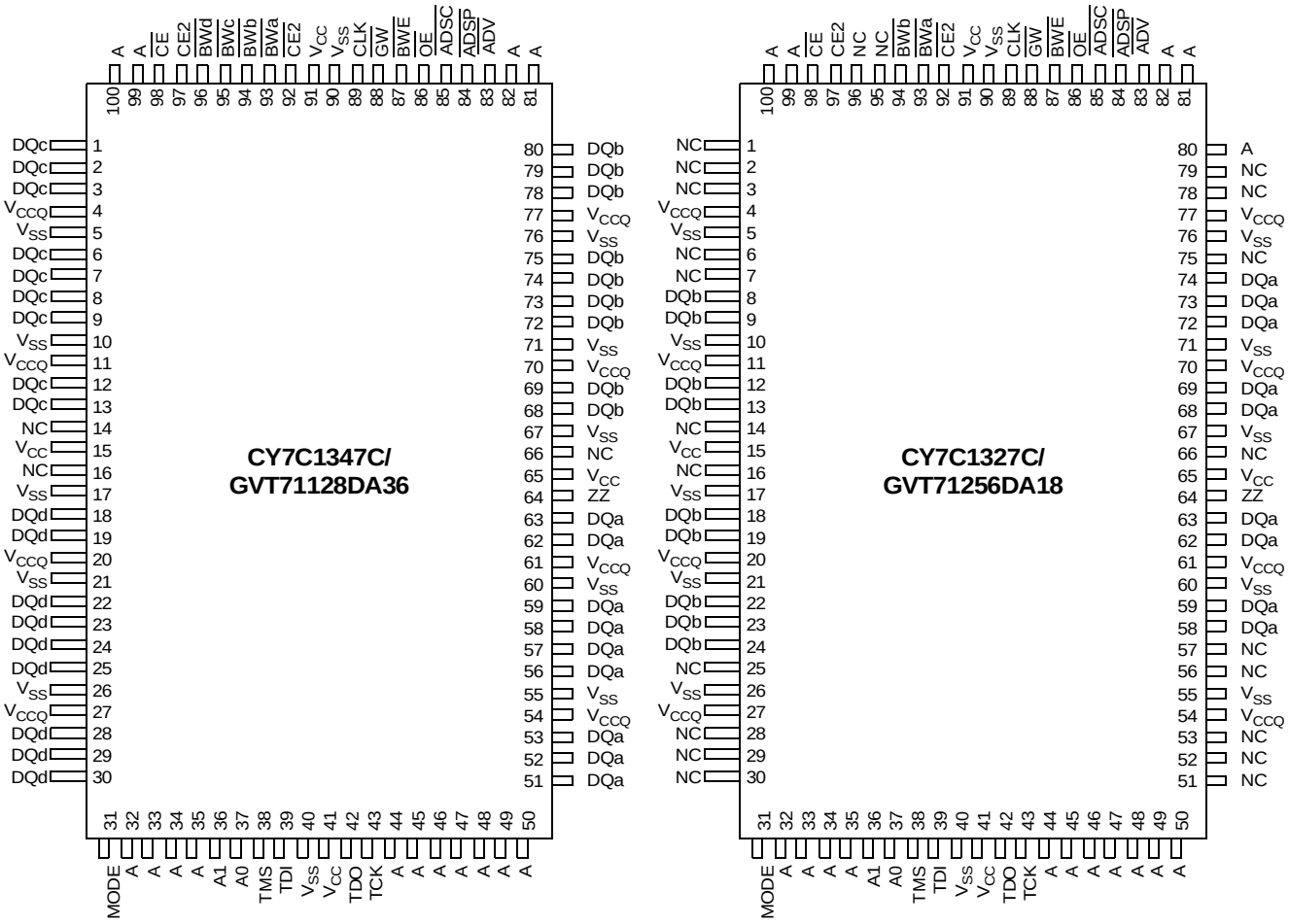


Note:

1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

Pin Configurations

100-Pin TQFP
Top View



Pin Configurations (continued)

119-Ball BGA
Top View
CY7C1347C/GVT71128DA36

	1	2	3	4	5	6	7
A	V_{CCQ}	A	A	$\overline{ADSP}$	A	A	V_{CCQ}
B	NC	CE2	A	$\overline{ADSC}$	A	$\overline{CE2}$	NC
C	NC	A	A	V_{CC}	A	A	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{CE}$	V_{SS}	DQb	DQb
F	V_{CCQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{CCQ}
G	DQc	DQc	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{GW}$	V_{SS}	DQb	DQb
J	V_{CCQ}	V_{CC}	NC	V_{CC}	NC	V_{CC}	V_{CCQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{CCQ}	DQd	V_{SS}	$\overline{BWE}$	V_{SS}	DQa	V_{CCQ}
N	DQd	DQd	V_{SS}	A1	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	A0	V_{SS}	DQa	DQa
R	NC	A	MODE	V_{CC}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{CCQ}	TMS	TDI	TCK	TDO	NC	V_{CCQ}

256Kx18

	1	2	3	4	5	6	7
A	V_{CCQ}	A	A	$\overline{ADSP}$	A	A	V_{CCQ}
B	NC	CE2	A	$\overline{ADSC}$	A	$\overline{CE2}$	NC
C	NC	A	A	V_{CC}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{CE}$	V_{SS}	NC	DQa
F	V_{CCQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa	V_{CCQ}
G	NC	DQb	$\overline{BWb}$	$\overline{ADV}$	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQa	NC
J	V_{CCQ}	V_{CC}	NC	V_{CC}	NC	V_{CC}	V_{CCQ}
K	NC	DQb	V_{SS}	CLK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	NC	$\overline{BWa}$	DQa	NC
M	V_{CCQ}	DQb	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{CCQ}
N	DQb	NC	V_{SS}	A1	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	A0	V_{SS}	NC	DQa
R	NC	A	MODE	V_{CC}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{CCQ}	TMS	TDI	TCK	TDO	NC	V_{CCQ}

128K X 36 Pin Descriptions

X36 BGA Pins	X36 QFP Pins	Name	Type	Description
4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 3T, 4T, 5T	37 36 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50	A0 A1 A	Input-Synchronous	Addresses: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
5L 5G 3G 3L	93 94 95 96	$\overline{BWa}$ $\overline{BWb}$ $\overline{BWc}$ $\overline{BWd}$	Input-Synchronous	Byte Write: A byte write is LOW for a Write cycle and HIGH for a Read cycle. $\overline{BWa}$ controls DQa. $\overline{BWb}$ controls DQb. $\overline{BWc}$ controls DQc. $\overline{BWd}$ controls DQd. Data I/O are high impedance if either of these inputs are LOW, conditioned by $\overline{BWE}$ being LOW.
4M	87	$\overline{BWE}$	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the set-up and hold times around the rising edge of CLK.
4H	88	$\overline{GW}$	Input-Synchronous	Global Write: This active LOW input allows a full 36-bit Write to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the set-up and hold times around the rising edge of CLK.
4K	89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
4E	98	$\overline{CE}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device and to gate $\overline{ADSP}$.
6B	92	$\overline{CE2}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.
2U 3U 4U	38 39 43	TMS TDI TCK	Input	IEEE 1149.1 test inputs. LVTTL-level inputs.
5U	42	TDO	Output	IEEE 1149.1 test output. LVTTL-level output.
1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 5R, 7R, 1T, 2T, 6T, 6U	14, 16, 66	NC	-	No Connect: These signals are not internally connected.

256K X 18 Pin Descriptions

X18 BGA Pins	X18 QFP Pins	Name	Type	Description
4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	37 36 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44, 49, 50	A0 A1 A	Input-Synchronous	Addresses: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
5L 3G	93 94	$\overline{BWa}$ $\overline{BWb}$	Input-Synchronous	Byte Write Enables: A byte write enable is LOW for a Write cycle and HIGH for a Read cycle. $\overline{BWa}$ controls DQa. $\overline{BWb}$ controls DQb. Data I/O are high impedance if either of these inputs are LOW, conditioned by $\overline{BWE}$ being LOW.
4M	87	$\overline{BWE}$	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CLK.

256K X 18 Pin Descriptions

X18 BGA Pins	X18 QFP Pins	Name	Type	Description
4H	88	$\overline{GW}$	Input-Synchronous	Global Write: This active LOW input allows a full 18-bit Write to occur independent of the BWE and WEn lines and must meet the set-up and hold times around the rising edge of CLK.
4K	89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
4E	98	$\overline{CE}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device and to gate ADSP.
6B	92	$\overline{CE2}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.
2B	97	CE2	input-Synchronous	Chip enable: This active HIGH input is used to enable the device.
4F	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
4G	83	$\overline{ADV}$	Input-Synchronous	Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
4A	84	$\overline{ADSP}$	Input-Synchronous	Address Status Processor: This active LOW input, along with $\overline{CE}$ being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
4B	85	$\overline{ADSC}$	Input-Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A Read or Write cycle is initiated depending upon write control inputs.
3R	31	MODE	Input-Static	Mode: This input selects the burst sequence. A LOW on this pin selects Linear Burst. A NC or HIGH on this pin selects Interleaved Burst.

Burst Address Table (MODE = NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

Burst Address Table (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

Truth Table[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Partial Truth Table for READ/WRITE[9]

FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE one byte	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

Note:

2. X means "don't care." H means logic HIGH. L means logic LOW.
   For X36 product, WRITE = L means [$\overline{BWE}$ + $\overline{BWa}$*$\overline{BWb}$*$\overline{BWc}$*$\overline{BWd}$]*GW equals LOW. WRITE = H means [$\overline{BWE}$ + $\overline{BWa}$*$\overline{BWb}$*$\overline{BWc}$*$\overline{BWd}$]*GW equals HIGH.
   For X18 product, WRITE = L means [$\overline{BWE}$ + $\overline{BWa}$*$\overline{BWb}$]*GW equals LOW. WRITE = H means [$\overline{BWE}$ + $\overline{BWa}$*$\overline{BWb}$]*GW equals HIGH.
3. BWa enables write to DQa. BWb enables write to DQb. BWc enables write to DQc. BWd enables write to DQd.
4. All inputs except OE must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
5. Suspending burst generates wait cycle.
6. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required set-up time plus High-Z time for $\overline{OE}$ and staying HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP LOW along with chip being selected always initiates a READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting $\overline{WRITE}$ LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.
9. For X18 product, there are only BWa and BWb.

IEEE 1149.1 Serial Boundary Scan (JTAG)

Overview

This device incorporates a serial boundary scan access port (TAP). This port is designed to operate in a manner consistent with IEEE Standard 1149.1-1990 (commonly referred to as JTAG), but does not implement all of the functions required for IEEE 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the critical speed path of the device. Nevertheless, the device supports the standard TAP controller architecture (the TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with IEEE Standard 1149.1 compliant TAPs. The TAP operates using LVTTL/LVCMOS logic level signaling.

Disabling the JTAG Feature

It is possible to use this device without using the JTAG feature. To disable the TAP controller without interfering with normal operation of the device, TCK should be tied LOW (V_{SS}) to prevent clocking the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be pulled up to VCC through a resistor. TDO should be left unconnected. Upon power-up the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port (TAP)

TCK - Test Clock (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS - Test Mode Select (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TDI - Test Data In (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to *Figure 1*, TAP Controller State Diagram). It is allowable to leave this pin unconnected if it is not used in an application. The pin is pulled up internally, resulting in a logic HIGH level. TDI is connected to the most significant bit (MSB) of any register. (See *Figure 2*.)

TDO - Test Data Out (OUTPUT)

The TDO output pin is used to serially clock data-out from the registers. The output that is active depending on the state of the TAP state machine (refer to *Figure 1*, TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO. TDO is connected to the least significant bit (LSB) of any register. (See *Figure 2*.)

Performing a TAP Reset

The TAP circuitry does not have a reset pin ($\overline{TRST}$, which is optional in the IEEE 1149.1 specification). A RESET can be performed for the TAP controller by forcing TMS HIGH (V_{CC}) for five rising edges of TCK and pre-loads the instruction register with the IDCODE command. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

At power-up, the TAP is reset internally to ensure that TDO is in a High-Z state.

Test Access Port (TAP) Registers

Overview

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected, it is connected between the TDI and TDO pins.

Instruction Register

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The parallel outputs of the instruction register are automatically preloaded with the IDCODE instruction upon power-up or whenever the controller is placed in the test-logic reset state. When the TAP controller is in the Capture-IR state, the two least significant bits of the serial instruction register are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

The bypass register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the device TAP to another device in the scan chain with minimum delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The Boundary scan register is connected to all the input and bidirectional I/O pins (not counting the TAP pins) on the device. This also includes a number of NC pins that are reserved for future needs. There are a total of 70 bits for x36 device and 51 bits for x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the device I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order table describes the order in which the bits are connected. The first column defines the bit’s position in the boundary scan register. The MSB of the register is connected to TDI, and LSB is connected to TDO. The second column is the signal name and the third column is the bump number. The third column is the TQFP pin number and the fourth column is the BGA bump number.

Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the device as described in the Identification Register Definitions table.

TAP Controller Instruction Set

Overview

There are two classes of instructions defined in the IEEE Standard 1149.1-1990; the standard (public) instructions and device specific (private) instructions. Some public instructions are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the device or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction sets for this device are listed in the following tables.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this device.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the device responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between two instructions. Unlike SAMPLE/PRELOAD instruction, EXTEST places the device outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in the instruction upon power-up and at any time the TAP controller is placed in the test-logic reset state.

SAMPLE-Z

If the High-Z instruction is loaded in the instruction register, all output pins are forced to a High-Z state and the boundary scan register is connected between TDI and TDO pins when the TAP controller is in a Shift-DR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory instruction. The PRELOAD portion of the command is not implemented in this device, so the device TAP controller is not fully IEEE 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded in the instruction register and the TAP controller is in the Capture-DR state, a snap shot of the data in the device's input and I/O buffers is loaded into the boundary scan register. Because the device system clock(s) are independent from the TAP clock (TCK), it is possible for the TAP to attempt to capture the input and I/O ring contents while the buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be expected. To guarantee that the boundary scan register will capture the correct value of a signal, the device input signals must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}). The device clock input(s) need not be paused for any other TAP operation except capturing the input and I/O ring contents into the boundary scan register.

Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the Update-DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP controller is in the Shift-DR state, the bypass register is placed between TDI and TDO. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

Reserved

Do not use these instructions. They are reserved for future use.

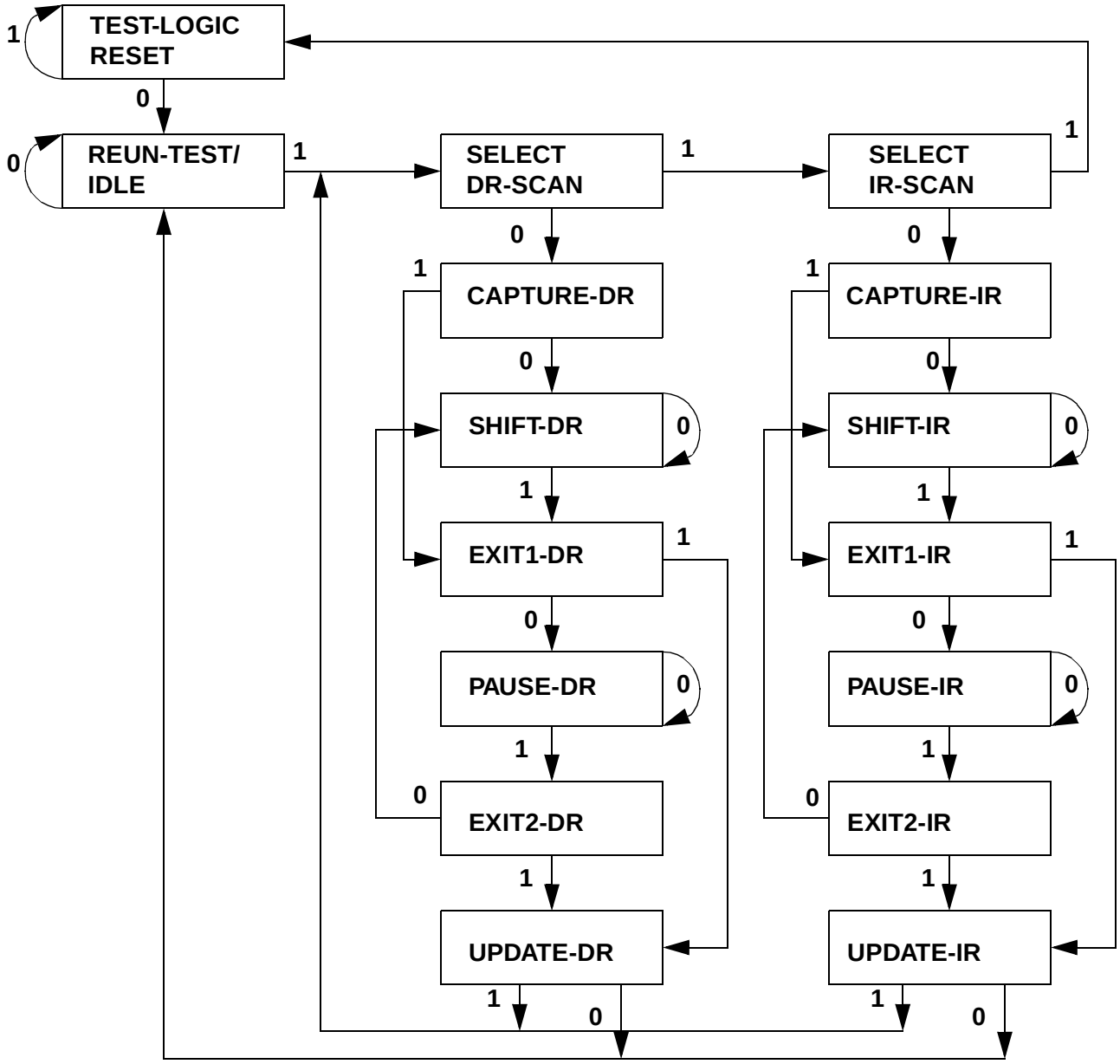


Figure 1. TAP Controller State Diagram[10]

Note:
10. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

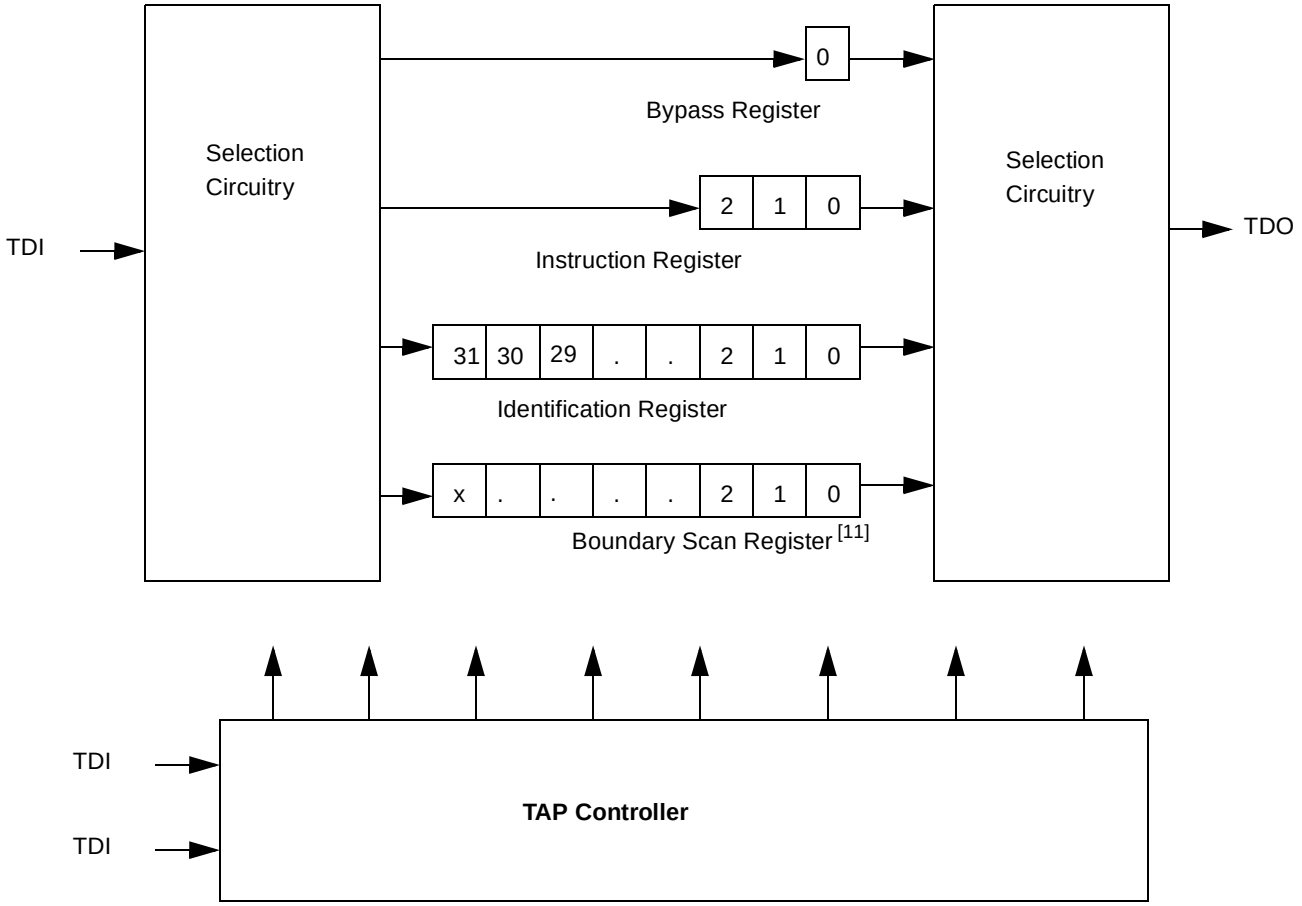


Figure 2. TAP Controller Block Diagram

TAP DC Electrical Characteristics (20°C ≤ T_j ≤ 110°C; V_{CC} = 3.3V –0.2V and +0.3V unless otherwise noted)

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IH}	Input High (Logic 1) Voltage[12, 13]		2.0	V_{CC} + 0.3	V
V_{Il}	Input Low (Logic 0) Voltage[12, 13]		–0.3	0.8	V
IL_I	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	–5.0	5.0	µA
IL_I	TMS and TDI Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	–30	30	µA
IL_O	Output Leakage Current	Output disabled, 0V ≤ V_{IN} ≤ V_{CCQ}	–5.0	5.0	µA
V_{OLC}	LVCMOS Output Low Voltage[12, 14]	I_{OLC} = 100 µA		0.2	V
V_{OHC}	LVCMOS Output High Voltage[12, 14]	I_{OHC} = 100 µA	V_{CC} – 0.2		V
V_{OLT}	LVTTL Output Low Voltage[12]	I_{OLT} = 8.0 mA		0.4	V
V_{OHT}	LVTTL Output High Voltage[12]	I_{OHT} = 8.0 mA	2.4		V

Notes:
11. X = 69 for the x36 configuration. X = 50 for the x18 configuration.
12. All Voltage referenced to V_{SS} (GND).
13. Overshoot: $V_{IH}(AC) \leq V_{CC}+1.5V$ for $t \leq t_{KHKH}/2$, Undershoot: $V_{IL}(AC) \geq -0.5V$ for $t \leq t_{KHKH}/2$, Power-up: $V_{IH} \leq 3.6V$ and $V_{CC} \leq 3.135V$ and $V_{CCQ} \leq 1.4V$ for $t \leq 200$ ms. During normal operation, V_{CCQ} must not exceed V_{CC}. Control input signals (such as R/$\overline{W}$, ADV/$\overline{LD}$, etc.) may not have pulse widths less than t_{KHKL} (min.).
14. This parameter is sampled.

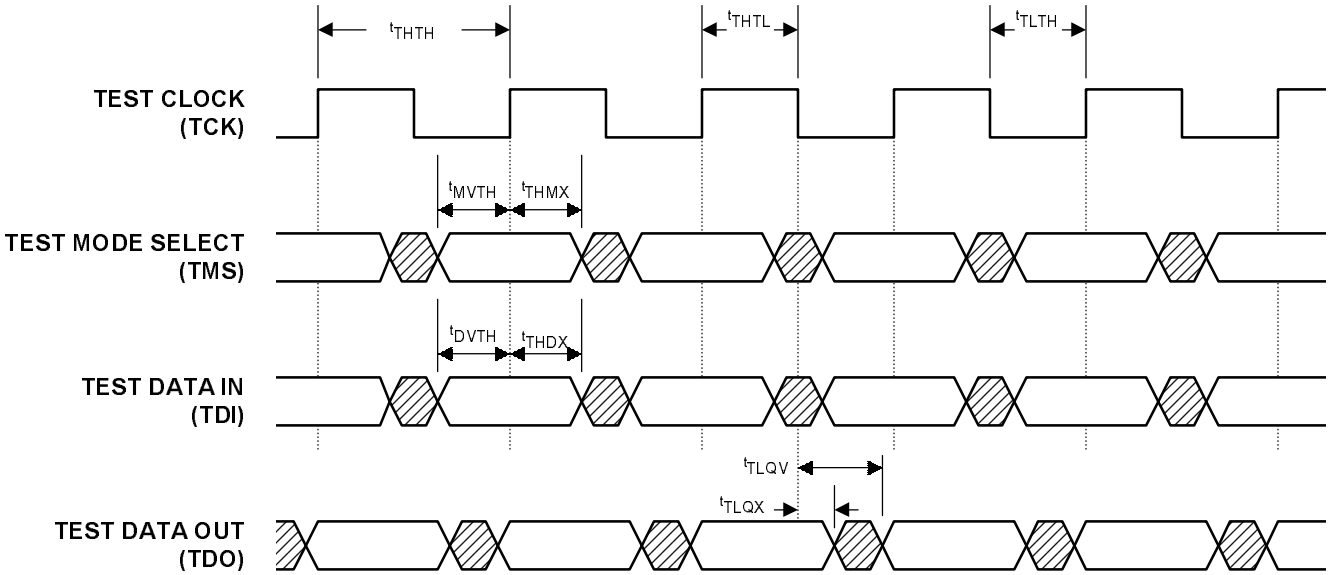
TAP AC Switching Characteristics Over the Operating Range[15, 16]

Parameter	Description	Min.	Max	Unit
Clock				
t_{THTH}	Clock Cycle Time	20		ns
f_{TF}	Clock Frequency		50	MHz
t_{THTL}	Clock HIGH Time	8		ns
t_{TLTH}	Clock LOW Time	8		ns
Output Times				
t_{TLQX}	TCK LOW to TDO Unknown	0		ns
t_{TLQV}	TCK LOW to TDO Valid		10	ns
t_{DVTH}	TDI Valid to TCK HIGH	5		ns
t_{THDX}	TCK HIGH to TDI Invalid	5		ns
Set-up Times				
t_{MVTH}	TMS Set-up	5		ns
t_{CS}	Capture Set-up	5		ns
Hold Times				
t_{THMX}	TMS Hold	5		ns
t_{CH}	Capture Hold	5		ns

Notes:
15. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
16. Test conditions are specified using the load in TAP AC Test Conditions.

TAP Timing and Test Conditions

(a)



Identification Register Definitions

Instruction Field	512K x 18	Description
REVISION NUMBER (31:28)	XXXX	Reserved for revision number.
DEVICE DEPTH (27:23)	00111	Defines depth of words.
DEVICE WIDTH (22:18)	00011	Defines width of bits.
RESERVED (17:12)	XXXXXX	Reserved for future use.
CYPRESS JEDEC ID CODE (11:1)	00011100100	Allows unique identification of DEVICE vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (x18)
Instruction	3
Bypass	1
ID	32
Boundary Scan	51

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state. This instruction is not IEEE 1149.1-compliant.
IDCODE	001	Preloads ID register with vendor ID code and places it between TDI and TDO. This instruction does not affect device operations.
SAMPLE-Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state.
RESERVED	011	Do not use these instructions; they are reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not affect device operations. This instruction does not implement IEEE 1149.1 PRELOAD function and is therefore not 1149.1-compliant.
RESERVED	101	Do not use these instructions; they are reserved for future use.
RESERVED	110	Do not use these instructions; they are reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This instruction does not affect device operations.

Boundary Scan Order (128K x 36)

Bit#	Signal Name	TQFP	Bump ID
1	A	44	2R
2	A	45	3T
3	A	46	4T
4	A	47	5T
5	A	48	6R
6	A	49	3B
7	A	50	5B
8	DQa	51	6P
9	DQa	52	7N
10	DQa	53	6M
11	DQa	56	7L
12	DQa	57	6K
13	DQa	58	7P
14	DQa	59	6N
15	DQa	62	6L
16	DQa	63	7K
17	ZZ	64	7T
18	DQb	68	6H
19	DQb	69	7G
20	DQb	72	6F
21	DQb	73	7E
22	DQb	74	6D
23	DQb	75	7H
24	DQb	78	6G
25	DQb	79	6E
26	DQb	80	7D
27	A	81	6A
28	A	82	5A
29	$\overline{ADV}$	83	4G
30	$\overline{ADSP}$	84	4A
31	$\overline{ADSC}$	85	4B
32	$\overline{OE}$	86	4F
33	$\overline{BWE}$	87	4M
34	$\overline{GW}$	88	4H
35	CLK	89	4K

Boundary Scan Order (128K x 36)

Bit#	Signal Name	TQFP	Bump ID
36	$\overline{CE_2}$	92	6B
37	$\overline{BWa}$	93	5L
38	$\overline{BWb}$	94	5G
39	$\overline{BWc}$	95	3G
40	$\overline{BWd}$	96	3L
41	CE_2	97	2B
42	$\overline{CE}$	98	4E
43	A	99	3A
44	A	100	2A
45	DQc	1	2D
46	DQc	2	1E
47	DQc	3	2F
48	DQc	6	1G
49	DQc	7	2H
50	DQc	8	1D
51	DQc	9	2E
52	DQc	12	2G
53	DQc	13	1H
54	NC	14	5R
55	DQd	18	2K
56	DQd	19	1L
57	DQd	22	2M
58	DQd	23	1N
59	DQd	24	2P
60	DQd	25	1K
61	DQd	28	2L
62	DQd	29	2N
63	DQd	30	1P
64	MODE	31	3R
65	A	32	2C
66	A	33	3C
67	A	34	5C
68	A	35	6C
69	A1	36	4N
70	A0	37	4P

Boundary Scan Order (256K x 18)

Bit#	Signal Name	TQFP	Bump ID
1	A	44	2R
2	A	45	2T
3	A	46	3T
4	A	47	5T
5	A	48	6R
6	A	49	3B
7	A	50	5B
8	DQa	58	7P
9	DQa	59	6N
10	DQa	62	6L
11	DQa	63	7K
12	ZZ	64	7T
13	DQa	68	6H
14	DQa	69	7G
15	DQa	72	6F
16	DQa	73	7E
17	DQa	74	6D
18	A	80	6T
19	A	81	6A
20	A	82	5A
21	$\overline{ADV}$	83	4G
22	$\overline{ADSP}$	84	4A
23	$\overline{ADSC}$	85	4B
24	$\overline{OE}$	86	4F
25	$\overline{BWE}$	87	4M
26	$\overline{GW}$	88	4H
27	CLK	89	4K
28	$\overline{CE2}$	92	6B
29	$\overline{BWa}$	93	5L
30	$\overline{BWb}$	94	3G
31	CE2	97	2B
32	$\overline{CE}$	98	4E

Boundary Scan Order (256K x 18)

Bit#	Signal Name	TQFP	Bump ID
33	A	99	3A
34	A	100	2A
35	DQb	8	1D
36	DQb	9	2E
37	DQb	12	2G
38	DQb	13	1H
39	NC	14	5R
40	DQb	18	2K
41	DQb	19	1L
42	DQb	22	2M
43	DQb	23	1N
44	DQb	24	2P
45	MODE	31	3R
46	A	32	2C
47	A	33	3C
48	A	34	5C
49	A	35	6C
50	A1	36	4N
51	A0	37	4P

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS}.....–0.5V to +4.6V

V_{IN} .....–0.5V to V_{CC}+0.5V

Storage Temperature (plastic) .....–55°C to +150°

Junction Temperature .....+150°

Power Dissipation.....1.0W

Short Circuit Output Current.....50 mA

Operating Range

Range	Ambient Temperature[17]	V_{DD}
Com'l	0°C to +70°C	3.3V –5%/+10%

Note:

17. T_A is the case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IHD}	Input High (Logic 1) Voltage[12, 18]	Data Inputs (DQx)	2.0	V_{CC}+0.3	V
V_{IH}		All Other Inputs	2.0	4.6	V
V_{II}	Input Low (Logic 0) Voltage[12, 18]		–0.5	0.8	V
IL_I	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	–5	5	µA
IL_I	MODE and ZZ Input Leakage Current[19]	$0V \le V_{IN} \le V_{CC}$	–30	30	µA
IL_O	Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	–5	5	µA
V_{OH}	Output High Voltage[12]	I_{OH} = –5.0 mA	2.4		V
V_{OL}	Output Low Voltage[12]	I_{OL} = 8.0 mA		0.4	V
VCC	Supply Voltage[12]		3.135	3.6	V
VCCQ	I/O Supply Voltage[12]		3.135	V_{CC}	V

Parameter	Description	Conditions	Typ.	-4	-4.4	-5	-6	Unit
I_{CC}	Power Supply Current: Operating[20, 21, 22]	Device selected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; cycle time $\ge t_{KC}$ min.; V_{CC} = Max.; outputs open	150	450	400	360	300	mA
I_{SB2}	CMOS Standby[21, 22]	Device deselected; V_{CC} = Max.; all inputs $\le V_{SS}$ + 0.2 or $\ge V_{CC}$ – 0.2; all inputs static; CLK frequency = 0	5	10	10	10	10	mA
I_{SB3}	TTL Standby[21, 22]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; all inputs static; V_{CC} = Max.; CLK frequency = 0	10	20	20	20	20	mA
I_{SB4}	Clock Running[21, 22]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; V_{CC} = Max.; CLK cycle time $\ge t_{KC}$ min.	40	140	125	110	90	mA

Capacitance[14]

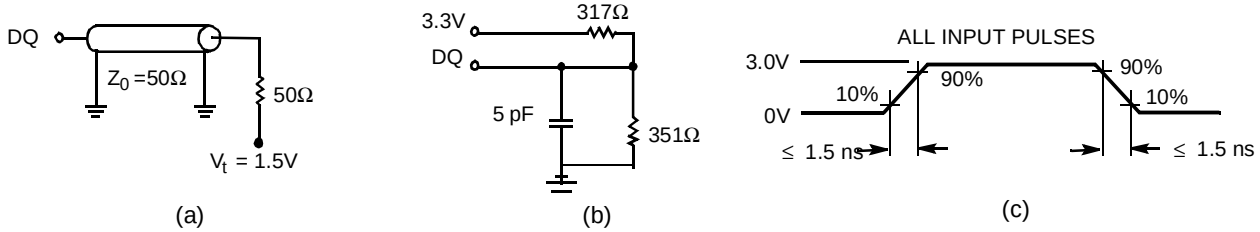
Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	5	7	pF
C_O	Input/Output Capacitance (DQ)		7	8	pF

Thermal Resistance

Description	Test Conditions	Symbol	TQFP Typ.	Unit
Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer PCB	Θ_{JA}	25	°C/W
Thermal Resistance (Junction to Case)		Θ_{JC}	9	°C/W

Notes:
18. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{KC}/2$.
Undershoot: $V_{IL} \le -2.0V$ for $t \le t_{KC}/2$.
19. Output loading is specified with C_L = 5 pF as in AC Test Loads.
20. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
21. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.
22. Typical values are measured at 3.3V, 25°C, and 20-ns cycle time.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[23]

Parameter	Description	-4 250 MHz		-4.4 225 MHz		-5 200 MHz		-6 166 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock										
t_{KC}	Clock Cycle Time	4.0		4.4		5.0		6.0		ns
t_{KH}	Clock HIGH Time	1.6		1.7		2.0		2.4		ns
t_{KL}	Clock LOW Time	1.6		1.7		2.0		2.4		ns
Output Times										
t_{KQ}	Clock to Output Valid		2.5		2.5		2.5		3.5	ns
t_{KQX}	Clock to Output Invalid	1.25		1.25		1.25		1.25		ns
t_{KQLZ}	Clock to Output in Low-Z[14, 19, 24]	0		0		0		0		ns
t_{KQHZ}	Clock to Output in High-Z[14, 19, 24]	1.25	3.0	1.25	3.0	1.25	3.0	1.25	4.0	ns
t_{OEQ}	OE to Output Valid[25]		2.5		2.5		2.5		3.5	ns
t_{OELZ}	OE to Output in Low-Z[14, 19, 24]	0		0		0		0		ns
t_{OEHZ}	OE to Output in High-Z[14, 19, 24]		2.5		2.5		2.5		3.5	ns
Set-up Times										
t_S	Address, Controls, and Data In[26]	1.0		1.0		1.0		1.0		ns
Hold Times										
t_H	Address, Controls, and Data In[26]	1.0		1.0		1.0		1.0		ns

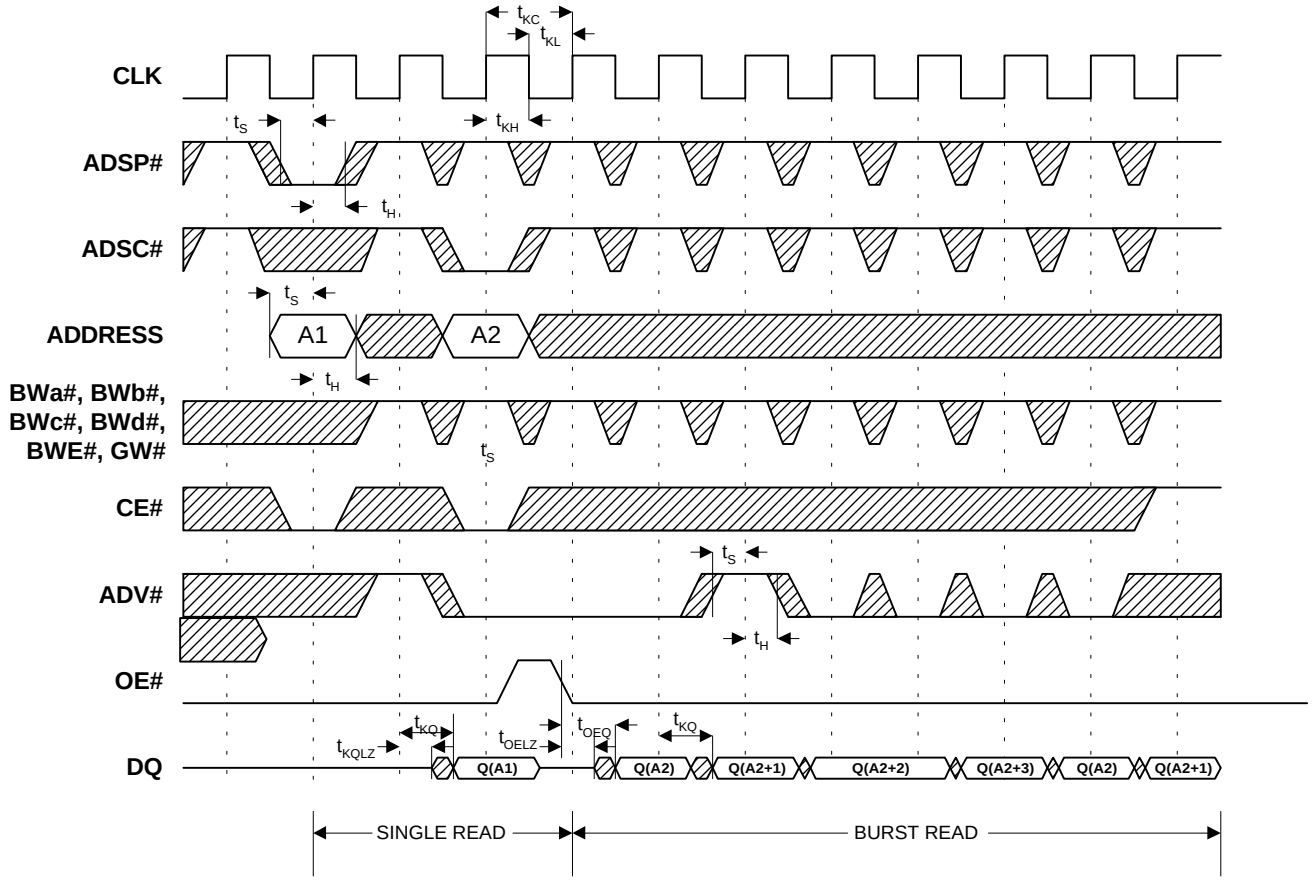
Typical Output Buffer Characteristics

Output High Voltage	Pull-Up Current			Output Low Voltage	Pull-Down Current	
V_{OH} (V)	I_{OH} (mA) Min.	I_{OH} (mA) Max.		V_{OL} (V)	I_{OL} (mA) Min.	I_{OL} (mA) Max.
–0.5	–38	–105		–0.5	0	0
0	–38	–105		0	0	0
0.8	–38	–105		0.4	10	20
1.25	–26	–83		0.8	20	40
1.5	–20	–70		1.25	31	63
2.3	0	–30		1.6	40	80
2.7	0	–10		2.8	40	80
2.9	0	0		3.2	40	80
3.4	0	0		3.4	40	80

Notes:
23. Test conditions as specified with the output loading as shown in part (a) of AC Test Loads unless otherwise noted.
24. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
25. OE is a “don’t care” when a byte write enable is sampled LOW.
26. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for “don’t care” as defined in the truth table.

Switching Waveforms

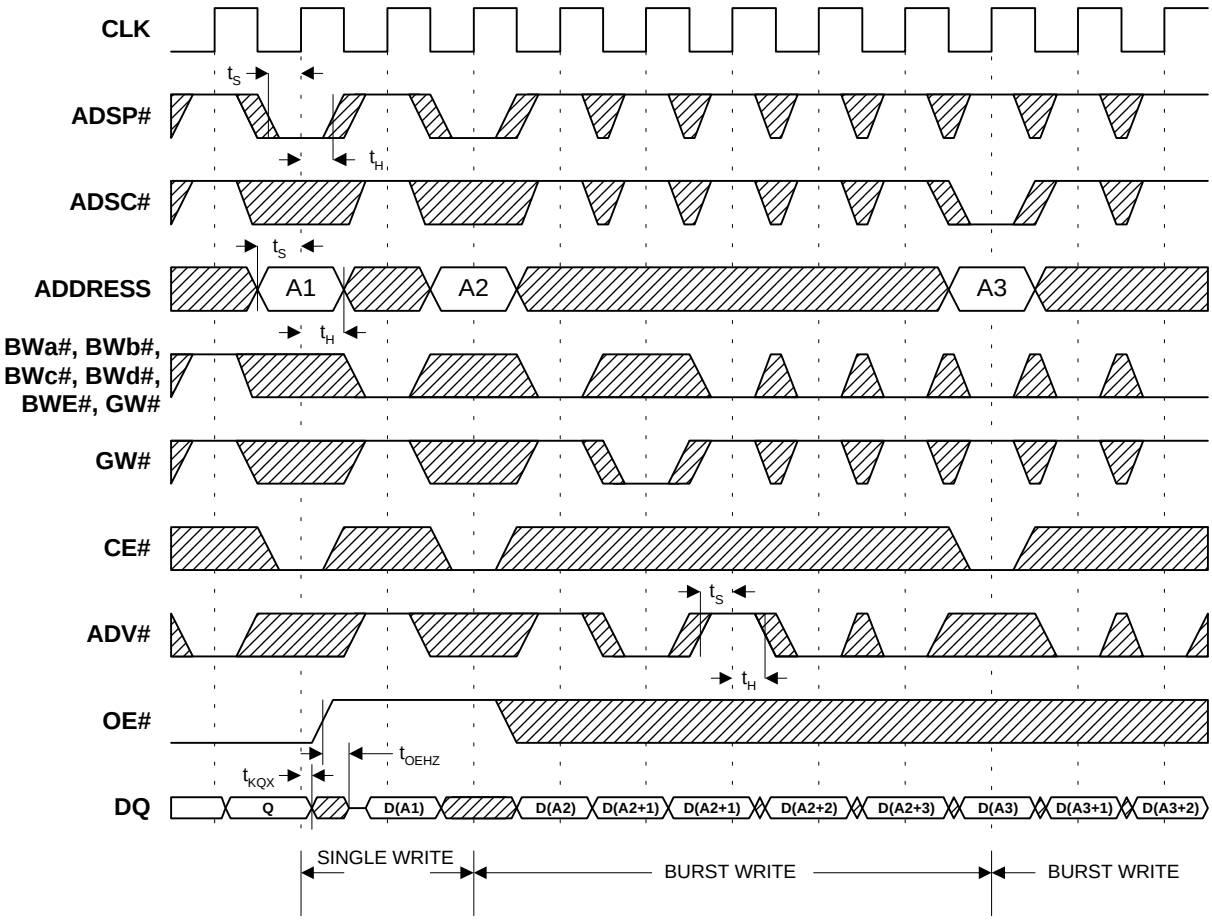
Read Timing[27, 28]



Notes:
27. $\overline{CE}$ active in this timing diagram means that all chip enables $\overline{CE}$, CE2, and $\overline{CE2}$ are active.
28. For X18 product, there are only BWa and BWb for byte write control.

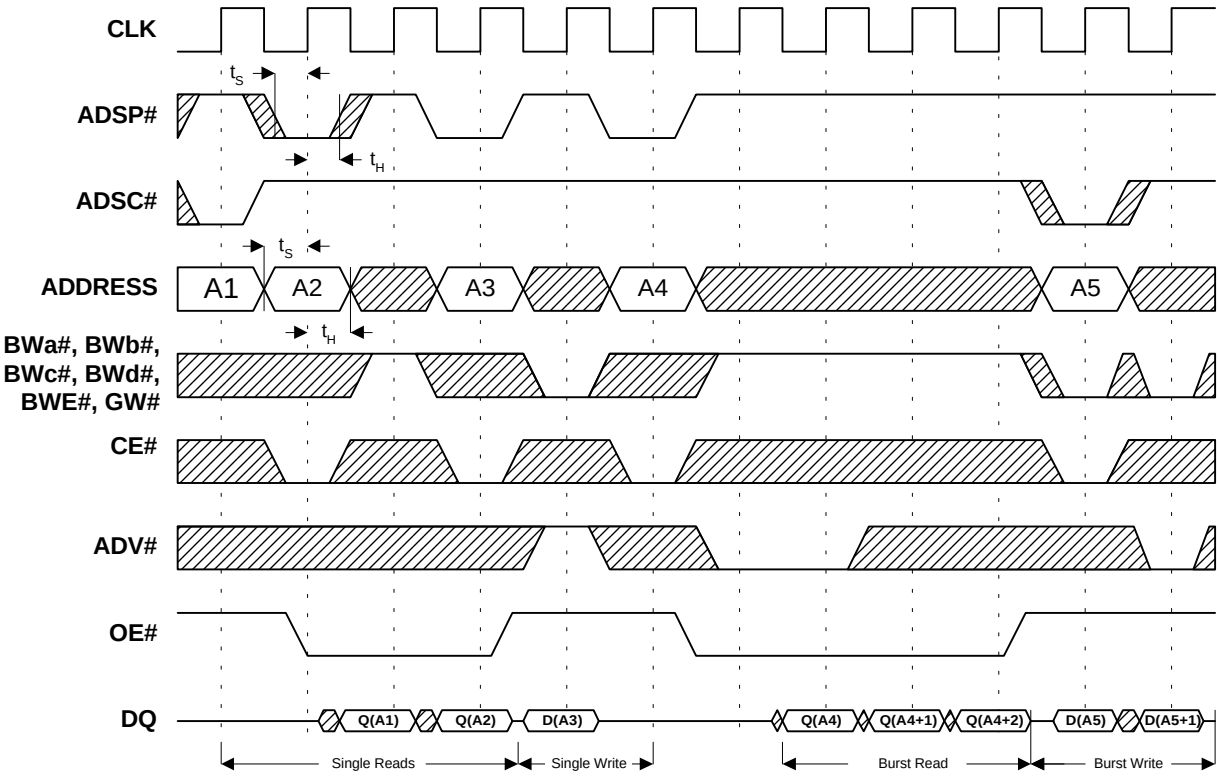
Switching Waveforms (continued)

Write Timing[27, 28]



Switching Waveforms (continued)

Read/Write Timing[27, 28]



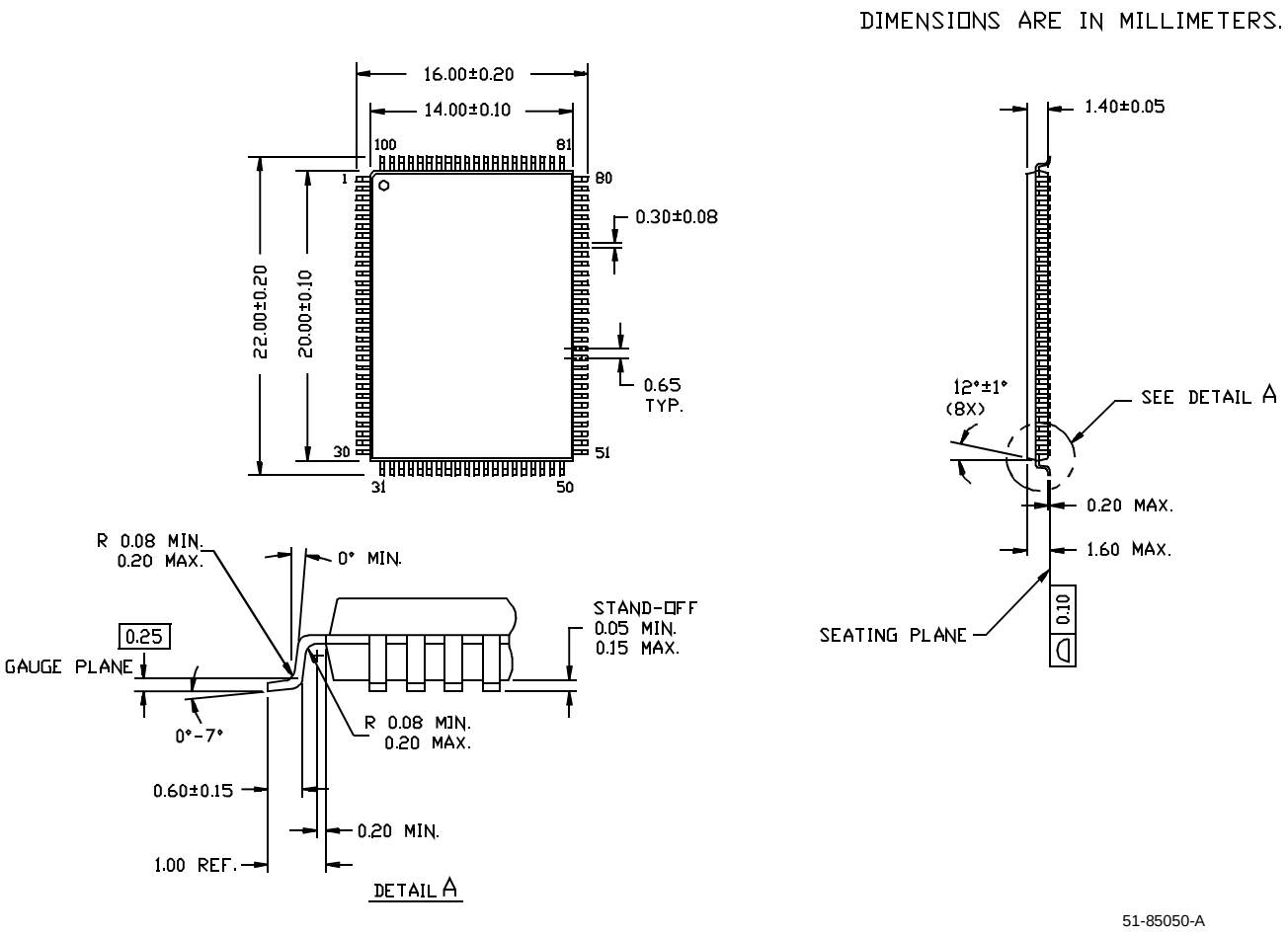
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CY7C1347C-250AC/ GVT71128DA36T-4	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1347C-250BGC/ GVT71128DA36B-4	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
225	CY7C1347C-225AC/ GVT71128DA36T-4.4	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
	CY7C1347C-225BGC/ GVT71128DA36B-4.4	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
200	CY7C1347C-200AC/ GVT71128DA36T-5	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
	CY7C1347C-200BGC/ GVT71128DA36B-5	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
166	CY7C1347C-166AC/ GVT71128DA36T-6	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
	CY7C1347C-16BGC/ GVT71128DA36B-6	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
250	CY7C1327C-250AC/ GVT71256DA18T-4	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1327C-250BGC/ GVT71256DA18B-4	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
225	CY7C1327C-225AC/ GVT71256DA18T-4.4	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
	CY7C1327C-225BGC/ GVT71256DA18B-4.4	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
200	CY7C1327C-200AC/ GVT71256DA18T-5	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
	CY7C1327C-200BGC/ GVT71256DA18B-5	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	
166	CY7C1327C-166AC/ GVT71256DA18T-6	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
	CY7C1327C-16BGC/ GVT71256DA18B-6	BG119	119-Lead FBGA (14 x 22 x 2.4 mm)	

Document #: 38-01000

Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



Package Diagrams (continued)

119-Lead FBGA (14 x 22 x 2.4 mm) BG119

DIMENSION IN MILLIMETERS (INCHES)