STV0974

Mobile Imaging DSP

Features

- **Supports VS6552 - 640 x 480 (VGA) color CMOS image sensor**
- **Supports VisionLink low EMI link to image sensor**
- **Specialized video processor for noise/defect filtering, color reconstruction, sharpness enhancement and radial corrections**
- **Programmable gamma correction for LCD support**
- **Programmable cropping, down-sizing by 1.5, 2, 2.5, 3, 4, 5 and 6, MMS (Multi Media Messaging Service) digital zoom**
- **JPEG compression, with programmable target file size**
- **M-JPEG operation at up to 30 frame/s at VGA resolution**
- **Programmable pixel output format including ITU-R 656 modes, RGB viewfinder modes and JPEG baseline**
- **Flashgun control**
- **Flexible host interface:**
  - 8-bit data /Hsync /Vsync video output interface and I²C camera control interface
  - 8-bit microprocessor interface with 2 Kbyte video FIFO for JPEG data, 10 Kbyte for non-JPEG data, interrupt and DMA requests
- **Multi-mode exposure control and color balance**
- **30 µW ultra low-power standby**
- **6 x 6 mm TFBGA low-footprint & lead-free package**

Description

The STV0974 is a low power digital image processor designed for the VS6552 color VGA image sensor. The STV0974 uses advanced image processing techniques to deliver high quality VGA images at up to 30 frames per second (frame/s). The sensor data received via the low EMI sensor interface is processed in real time: this includes pixel defect correction, color interpolation, image sharpness enhancement, selective noise filtering, cropping and scaling, allowing digital zoom for ViewFinder or MMS applications. Finally the image can be JPEG-compressed in real-time. The STV0974 also performs sensor housekeeping functions such as automatic exposure and white balance controls.

Applications

- **Mobile phone embedded camera system**
- **PDA embedded camera or accessory camera**
- **Wireless security camera**

Technical Specifications

Sensor	640 x 480 color CMOS (VS6552)
Frame rate (frame/s)	up to 30
Power supply	1.8 +/- 0.1 V
Power requirements	110 mW active < 30 µW standby
Package dimensions	6 mm x 6 mm x 1.2 mm
Temperature range	[-25; +70] °C

Ordering Information

Ordering code	Package
STV0974/TR	TFBGA SnPb balls
STV0974E/TR	TFBGA AFOP lead-free balls

Contents

1 Overview

The STV0974 is a mobile imaging digital signal processor which, when used with VS6552 CMOS color VGA image sensor from STMicroelectronics, performs all the required data processing to deliver good quality Viewfinder, still and live color images. The STV0974 performs high quality color processing on images, achieving JPEG compression if requested and transfers them to a baseband through one of the available interfaces.

Data is transferred from sensor to STV0974 through Low Electromagnetic Interference (EMI) interface, using the sensor data transfer protocol over LVDS.

Data is transferred from STV0974 to Baseband

- through the video output interface. In video mode, the processor streams video data in a format which closely follows the data format specified in the ITU-R656 standard.
- through the microprocessor Interface. In microprocessor mode, the video data is stored in a small FIFO before is it pulled out of the asynchronous microprocessor interface by the host system (with DMA support).

1.1 Viewfinder mode

When connected to microprocessor interface or video output interface, the STV0974 can process Viewfinder image up to 30 frame/s.

1.2 Still features

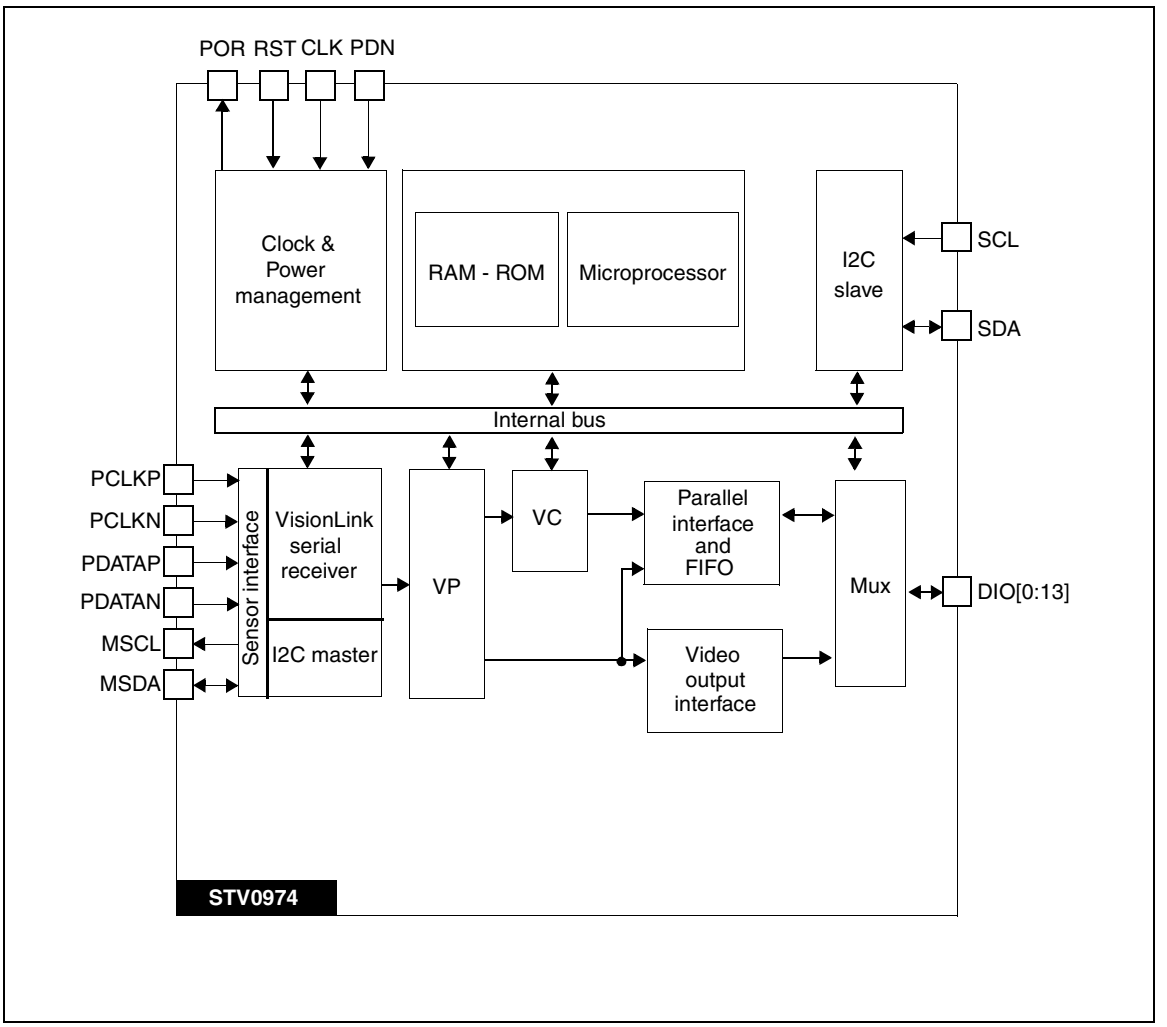
When requested by the baseband, the STV0974 captures bayer data from the sensor. Data is then color processed, down-scaled and/or compressed and sent through video output or microprocessor interface. In still mode, the first image produced has a guaranteed good exposure and color balance for single shot capture.

1.3 Live features

When connected to microprocessor interface or video output interface, the STV0974 can process live video up to 30 frame/s and eventually proceed to down-scaling and compression with on-chip Motion JPEG. Live mode is intended for capture of video sequences.

2 Functional block diagram

Figure 1: Functional block diagram



3 Signal description

Table 1: STV0974 signal description

Pin name	Type	Description
Power supplies		
VDD	PWR	Positive power supply
VCORE	PWR	Decoupling for internal core power supply
VDDPOR	PWR	Power on reset VDD supply 1.8 V
VSS	PWR	Digital ground
Sensor interface		
PDATAP, PDATAN	subLVDS In	Sensor data +, sensor data -, with internal 100 Ω termination resistor
PCLKP, PCLKN	subLVDS In	Sensor clock +, sensor clock -, with internal 100 Ω termination resistor
MSDA	I/O	Sensor I^2C data
MSCL	I/O	Sensor I^2C clock
Host interface		
POR	O	Power on reset output
RST	I	Reset input
CLK	I	System clock
PDN	I	Power down
DIO[0:11]DIO[13]	I/O	Host interface configurable I/O, see *Table 2*
DIO[12]	I/O	Flash Strobe Output (FSO)
SDA	I/O	Host I^2C data
SCL	I/O	Host I^2C clock
Test interface (ST internal use)		
TMS	I	Test mode
TCK	I	Test clock
TDI	I	Test data in
TDO	O	Test data out
Not connected		
NC		Not connected

Table 2: Host interface pins - output modes

Pin name	Microprocessor interface	Video port
DIO[0:7]	DATA[0:7]	DATA[0:7]
DIO[8]	RS	HSYNC
DIO[9]	CSN	VSYNC
DIO[10]	WRN	HCLK
DIO[11]	RDN	NC
DIO[12]	DRQ	FSO[a]
DIO[13]	IRQ	NC

a. Flash Strobe Output

4 Functional description

4.1 Overview

The processor includes a chain of dedicated video data processing blocks controlled by a microprocessor. The processing blocks perform the main video pipe processing while the microprocessor manages the interactions between the sensor, the functional blocks and the host.

The host controls and monitors the STV0974 via a set of read/write registers accessible via the I^2C interface for the streaming video mode and via the asychronous microprocessor interface for the microprocessor mode.

In video mode, the processor streams video data in a format which closely follows the data format specified in the ITU-R656 standard.

In microprocessor mode, the video data is stored in a small FIFO before is it pulled out of the asynchronous microprocessor interface by the host system (with DMA support).

4.1.1 Video pipe block description

Please refer to the block diagram (*Figure 1*).

Sensor interface This block decodes the incoming serial data stream from the sensor (raw bayer data) and converts it into a parallel form for the processing chain.

Video processor The video processor converts the raw bayer data from the sensor to RGB or YUV processed data by applying a number of filters to the data then scaling and converting the data into either one of the RGB modes or into YUV mode.

Video JPEG compressor The video compressor converts the processed data from the video processor and converts the data into JPEG format. The compression ratio applied to the image can be controlled by the microprocessor.

Streaming video output port In streaming video mode the data from either the video processor or the video compressor is enclosed in a format which closely follows the data format specified in the ITU-R656 standard.

Microprocessor interface In microprocessor interface mode, the data from the video processor or video compressor is stored in a FIFO. The interface informs the system via an IRQ or a DRQ that the FIFO is filling up. The system then has to pull some of the data from the STV0974 via the microprocessor interface.

4.1.2 Control

Register map The STV0974 is controlled via a register map that is maintained by the STV0974 microprocessor. Each register in the map has an address and contains either read or read/write data. The read only registers detail the current state of the STV0974. Read/write registers can be written to in order to modify the default behavior of the STV0974. The map is accessed via I^2C or via the microprocessor interface.

Micro processor interface In microprocessor interface mode the STV0974 register map can be accessed by writing the address of the register to the port and then reading or writing the register value.

Video output interface In streaming video mode, the STV0974 register map can be accessed via the I^2C port on the STV0974. The STV0974 is addressed by supplying the device address, register address and value to be written or read.

Microprocessor The microprocessor maintains the system interface via the register map. Any changes in system state are reflected in this map by the microprocessor and any changes commanded by the host system via this interface are then applied by the microprocessor.

When the system is commanded to change state, the microprocessor configures the functional blocks from the STV0974 and the sensor into the requested mode. The register map is updated accordingly to reflect the new state of the hardware.

The microprocessor monitors statistics gathered from the incoming image data and responds to changes in images. It adapts the functional block settings to correct for shifts in environmental conditions such as light level and illumination color temperature. The microcontroller will optimize these settings to provide the best quality image on all occasions.

4.1.3 Other functional blocks

Power management The hardware state of the STV0974 can be controlled by the power down pin (PDN). Upon the application of power to the STV0974 and PDN release, the STV0974 power-on-reset cell issues a timed reset pulse and then releases the STV0974 into its boot state.
The power-on-reset cell which output is the POR signal, is externally connected to the RST pin.

Clocks In sleep mode, the STV0974 clock is derived from the clock signal applied to the CLK pin. In all other modes, the STV0974 clock is derived from the high speed clock received from the sensor.

4.2 Sensor interface

4.2.1 Features

- Low electromagnetic interference (EMI) interface with CMOS image sensors
- High speed serial receiver, with data and clock inputs
- Up to 120 Mbit/s operation using very low voltage differential signaling (vLVDS)
- VisionLink transfer protocol
- I²C compliant master controller, 1.8 V interface, up to 400 kHz operation

4.2.2 Description

The STV0974 sensor interface is dedicated to the VS6552 image sensor that uses the VisionLink data transfer protocol over vLVDS. This includes:

- An I²C master controller supporting 1.8 V interface and 400 kHz operation. The I²C master port signals are MSDA and MSCL that require external pull-up resistors. Internally, the I²C master is a peripheral of the microprocessor control unit.
- Two vLVDS receivers for sensor data and clock signals, PDATA and PCLK differential pairs respectively. Each receiver accepts 1.8 V LVDS signals
- A VisionLink data synchronization and extraction unit, which extracts image timing references, active video and sensor status information. The extracted video stream in raw Bayer format along with active video strobes are connected to the video processing unit. The sensor status information is presented to the microprocessor control unit.

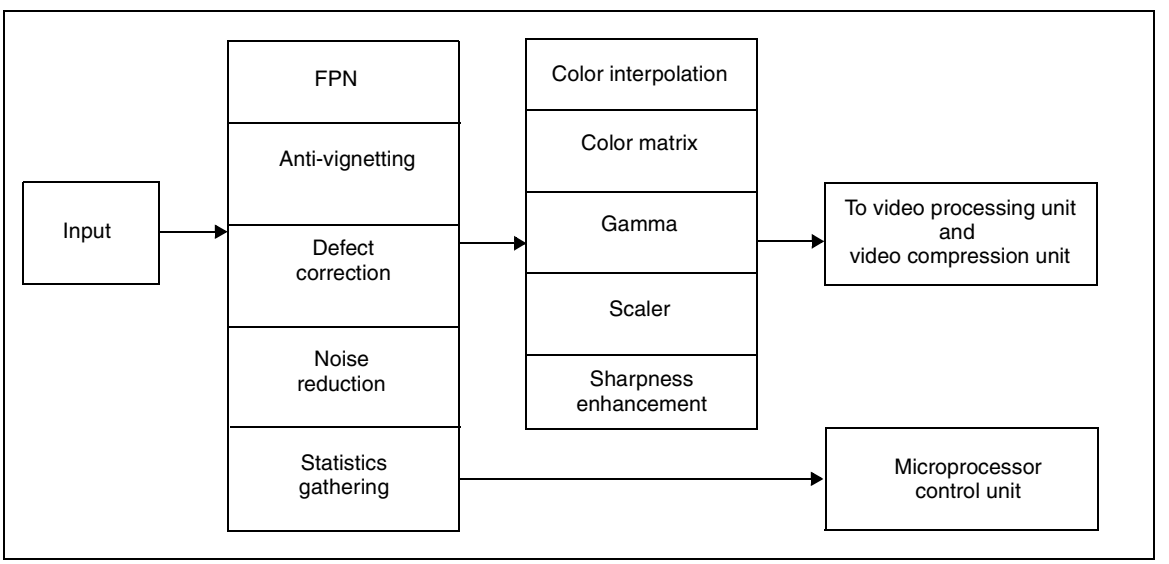
4.3 Video processing unit

4.3.1 Features

- Low-power dedicated hardware video processing unit, pipeline operation up to VGA resolution 30 Hz
- Image sensor correction stage including pixel defect correction and fixed pattern noise (FPN) cancellation
- Color interpolation stage with anti-aliasing and color matrix compensation
- Optical system compensation stage including anti vignetting and sharpness enhancement
- Noise reduction filter
- Programmable gamma and s-curve gamma for LCD support
- Full frame statistics gathering for exposure and color balance controls
- Programmable output image size (downscale by 1.5, 2, 2.5, 3, 4, 5 and 6)

4.3.2 Overview

Figure 2: Video processing unit



Fixed Pattern Noise (FPN) cancellation The FPN cancellation algorithm removes any column variability over the video area.

Statistics gathering Image statistics are gathered on the full resolution input image and forwarded to the camera control unit for exposure and color balance control loops.

Anti vignetting A radial gain is applied to the image luminance to compensate for possible luminance loss in the corners of the image due to an imperfect lens system.

Defect correction The defect correction algorithm can detect and correct any defective pixels in a sensor array.

Noise reduction filter The noise reduction filter is based on an adaptive algorithm. This algorithm performs filtering but does not affect image areas including significant information.

Color interpolation Each pixel RGB components are calculated by interpolation of the incoming Bayer pattern.

Color matrix Each pixel (RGB vector) is multiplied by a color matrix to adjust color balance. Viewfinder and live settings are independent to allow for optimization of both LCD display and capture for later viewing (i.e. on a PC).

Sharpness enhancement A sharpening two-dimensional mask is applied to Green only and from interpolation. The resulting data is added (with a gain factor) to the matrix RGB data.

Downscaler The downscaler unit extracts a rectangular region of interest and resizes the image by resampling video data. Standard image size such as CIF, QVGA and QCIF are available as well as a fully programmable custom size:

Table 3: Standard image size, VGA input

Format	Image size	Cropping	Scaling	Comments
VGA	640 x 480	None	None	
CIF	352 x 288	528 x 432	/ 1.5	82.5% of input image used, centered
QVGA	320 x 240	None	/ 2	
QCIF	176 x 144	528 x 432	/ 3	82.5% of input image used, centered
QQVGA	160 x 120	None	/ 4	
SubQCIF	128 x 96	None	/ 5	
QQCIF	88 x 72	528 x 432	/ 6	82.5% of input image used, centered
Custom	max VGA	Any	Any	See below

When custom size is selected, the crop and scale parameters are subject to the following constraints to ensure proper operation:

- Output image size must be in 8 x 8 pixels increments
- Scaling factor can be any value giving an input image size within input limits

Gamma correction A non-linear gain is applied to each pixel's RGB components to compensate for the display's non-linearity. A standard curve is available for image capture for later viewing on a PC and an S-curve is available for LCD display.

Coder The coder unit converts the internal RGB video stream to a user selectable output video format. It is based on a YUV digital video encoder with embedded synchronization codes, compliant with *[1]*, extended with the support of RGB formats for viewfinder usage, as shown in *Table 4*.

Table 4: Output video formats

Name	Format	Description
UYVY	$Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ $U_7U_6U_5U_4U_3U_2U_1U_0$ $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ $V_7V_6V_5V_4V_3V_2V_1V_0$	YUV (or YC_BC_R) 4:2:2 format as per *[1]*
RGB565	$R_4R_3R_2R_1R_0G_5G_4G_3$ $G_2G_1G_0B_4B_3B_2B_1B_0$	16-bit RGB format for direct viewfinder on 64 K color LCDs.
RGB444	$0_30_20_10_0R_3R_2R_1R_0$ $G_3G_2G_1G_0B_3B_2B_1B_0$	16-bit RGB format for direct viewfinder on 4096 color LCDs. Uses 4 bit per RGB component, the four MSB's are zero padded.
RGB332	$R_2R_1R_0G_2G_1G_0B_1B_0$	8-bit RGB format for low bit rate viewfinder usage.

Byte ordering assumes a little endian memory system, i.e. in 16-bit formats, the least significant byte is sent first. For example, the UYVY format produces the sequence U Y_0 V Y_1... as per [1].

Note: Nevertheless various options are available to suit memory system requirements:

- Byte ordering can be changed to big endian
- In YUV formats, the U and V components can be swapped
- In RGB formats, the R and B components can be swapped

YUV format processing The RGB pixel is converted to YUV coordinates according to ITU-R BT601 specification. The YUV coordinates are then rounded and clipped for an 8-bit representation. To produce a 4:2:2 digital component video, U and V components are filtered and down sampled by a factor of 2, coincident with Y sampling time.

RGB format processing Dithering: In order to avoid contouring effects on low color depth displays, the RGB components are dithered prior to truncation to the required number of bits.

Framing: The output frame is produced by performing the following steps:

1 **Blanking code insertion:** During video blanking intervals, blanking codes are inserted in the output stream. The default blanking code is the 16-bit pattern 0x1080, corresponding to Y = 0x10 and U/V = 0x80 as per *[1]*.

2 **Synchronization pattern detection and correction:** The coder performs detection of various synchronization patterns and applies a correction according to the current output format.

3 **Video Timing Reference Code Insertion:** A 4-byte sequence is inserted at the beginning and the end of each digital video line to delineate lines and frames in the video stream. The sequence is defined in *[1]* as FF 00 00 XY, where the XY byte is defined by:

Table 5: XY bits definition

Bit	Symbol	Definition
7 (msb)	1	Always 1.
6	F	Even / Odd Field. To maintain compatibility with *[1]*, F is alternatively 0 or 1.
5	V	V = 1 during field blanking, 0 otherwise.
4	H	H = 1 during line blanking, 0 otherwise.
3	P3	Protection bit: P3 = V xor H
2	P2	Protection bit: P2 = F xor H
1	P1	Protection bit: P1 = V xor V
0 (lsb)	P0	Protection bit: P0 = F xor V xor H

SAV (Start of Active Video) is defined as the 4-byte sequence where H = 0.

EAV (End of Active Video) is defined as the 4-byte sequence where H = 1.

4.4 Video compression (VC)

Real time video compression permits a frame rate of 30 frame/s in any mode at VGA.

The JPEG compression engine is a standard baseline sequential JPEG encoder *[2]*.

The compression ratio can be modified by applying a multiplication factor on the quantization table. The quantization table can be scaled from a factor of 1/8 to a factor of 8.

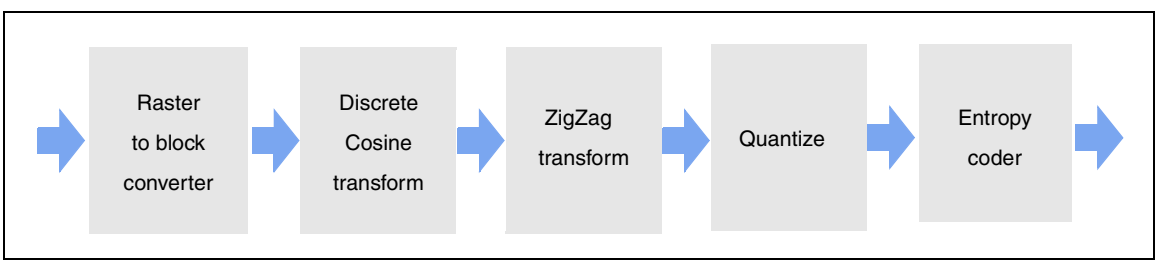
The STV0974 video compression block includes a baseline DCT JPEG encoder compliant with ISO DIS 10918-1.

The JPEG encoder has the following characteristics:

- baseline sequential DCT based encoder
- YUV 422 encoding only
- up to VGA image size
- scalable quantization table
- standard quantization table
- standard Huffman coder

The encoder top level block diagram is presented in *Figure 3*.

Figure 3: Encoder top level block diagram

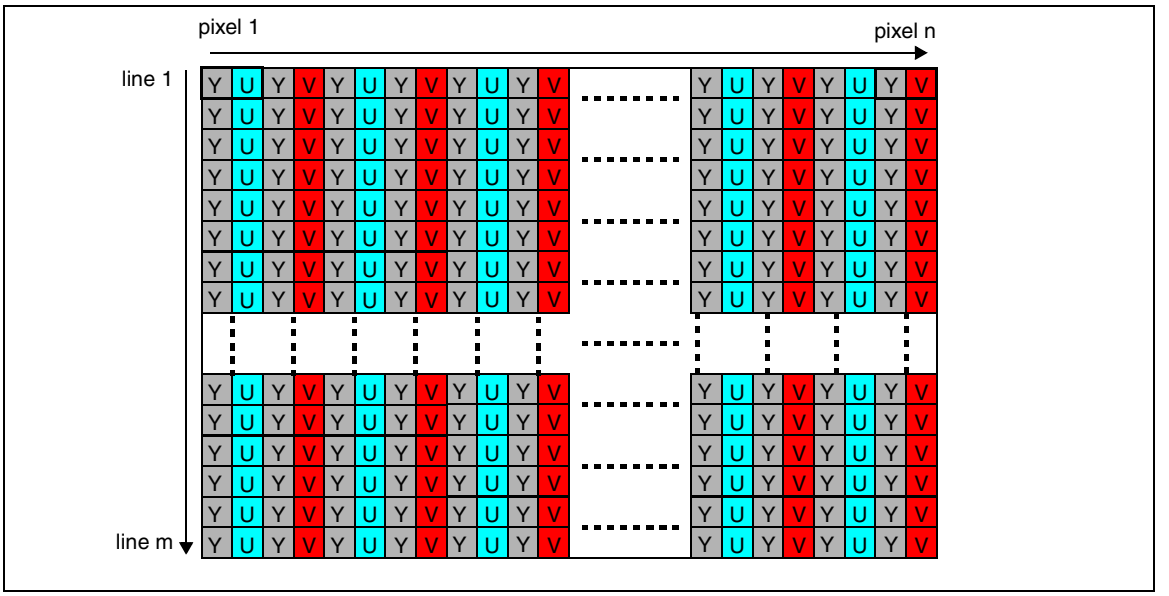


The input data is a YUV 422 8-bit data stream in raster order. The output data is a baseline JPEG data stream.

4.4.1 Raster to block converter

This block transforms the raster scan ordered data into block based ordered data. This data ordering is compliant with ISO DIS 10918-1 Annex A - Section A.2.

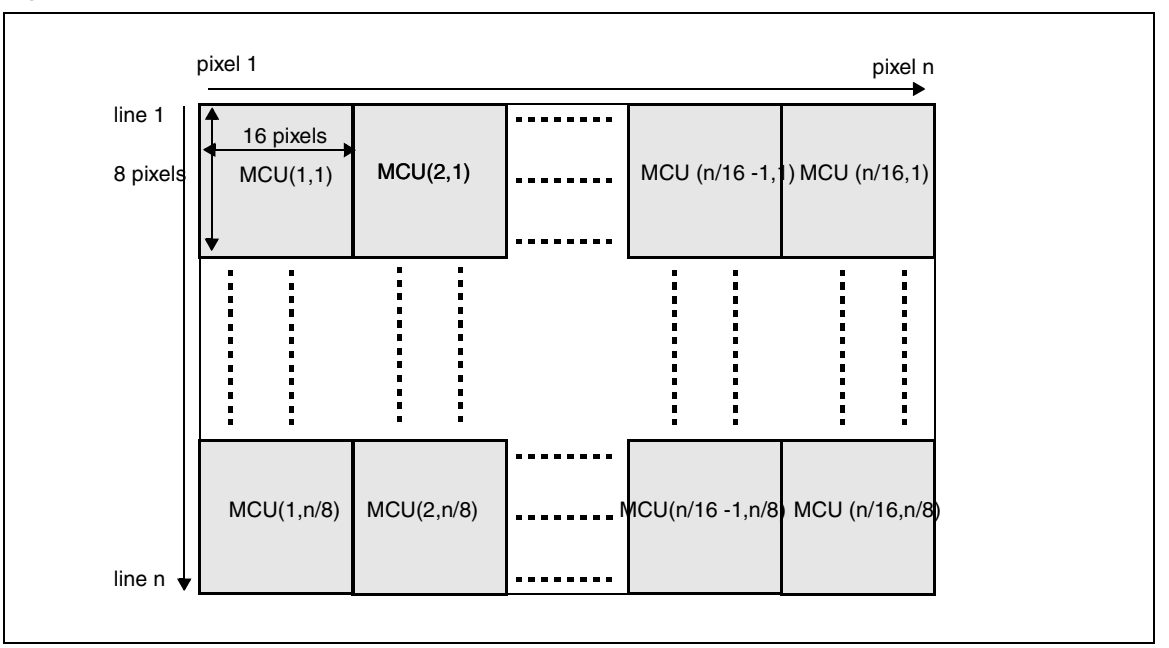
Figure 4: Data sequence at Raster to block input



The sequence of the input data stream is the following: line 1 from left to right up to pixel n, then line 2 from left to right.....up to line m, pixel n.

The output data stream sequence is block based. The image is segmented into MCU (minimum coded units) as illustrated in *Figure 5*.

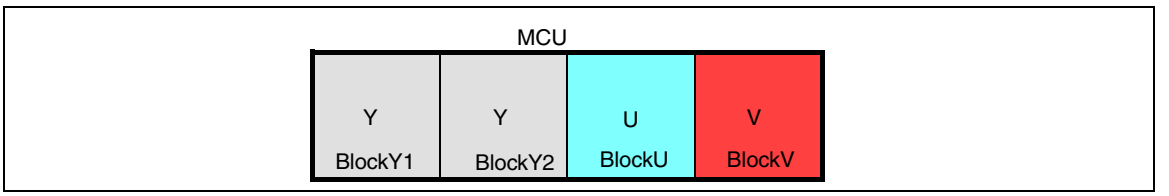
Figure 5: MCU data order



The MCU sequence order is top left to top right and top to bottom.

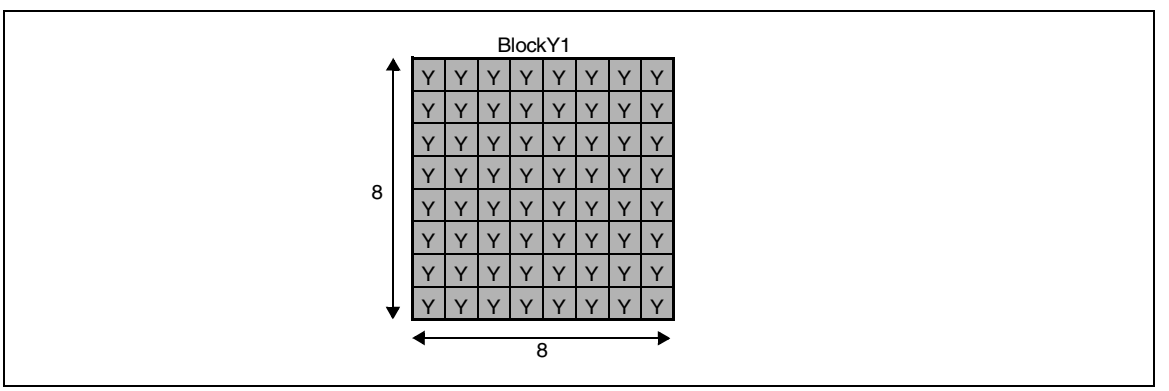
Figure 6 shows the MCU structure made of 4 blocks: 2 blocks of 8x8 Y component, 1 block of 8x8 U component and one block of 8x8 V component. The series of blocks must be processed according to this order.

Figure 6: Structure of each MCU



Each block is composed of 8x8 components. *Figure 7* presents the structure of BlockY1, as an example.

Figure 7: Structure of block Y1



The data sequence inside each block is left to right and top to bottom.

To summarize, at the output of Raster to Block converter, the data order is the following:

Y data of blockY1 of first MCU (64 data from left to right, then top to bottom)

Y data of blockY2 of first MCU (64 data from left to right, then top to bottom)

U data of blockU of first MCU (64 data from left to right, then top to bottom)

V data of blockV of first MCU (64 data from left to right, then top to bottom)

Y data of blockY1 of second MCU (64 data from left to right, then top to bottom)

Y data of blockY2 of second MCU (64 data from left to right, then top to bottom)

U data of blockU of second MCU (64 data from left to right, then top to bottom)

V data of blockV of second MCU (64 data from left to right, then top to bottom)

... up to last image MCU.

4.4.2 Discrete Cosine Transform

This block performs a Discrete Cosine Transform on the incoming data stream. It is compliant with ISO DIS 10918-1 Annex A - Section A.3.

The block processes each 8x8 input block to transform them into 8x8 DCT coefficients. The calculation of the DCT coefficients is done by the formula:

$$F(u, v) = \frac{2}{N} \times \sum_{x=0}^{7} \sum_{y=0}^{7} C(u)C(v)f(x, y)\cos\frac{(2x+1)u\pi}{16}\cos\frac{(2y+1)v\pi}{16}$$

with

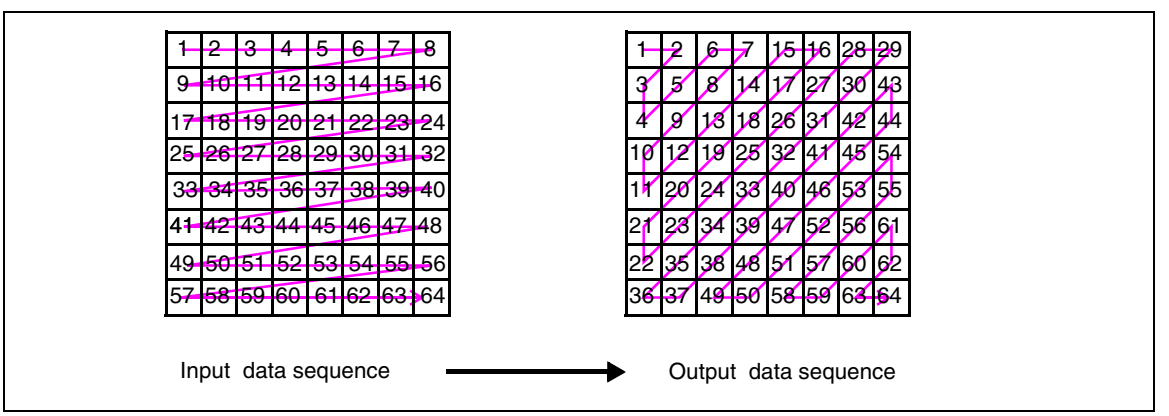
$$C(u),C(v) = \frac{1}{\sqrt{2}} \qquad \forall(u, v) = 0$$

$$C(u),C(v) = 1 \qquad \forall(u, v) \neq 0$$

4.4.3 Zigzag transform

This block is in charge of setting the DCT coefficients in a sequence that corresponds to an increasing spacial frequency of the cosine function. It is compliant with ISO DIS 10918-1 Annex A - Section A.3.6.

Figure 8: ZigZag block sequence re-ordering



4.4.4 Quantization block

This block applies a uniform quantizer on all DCT coefficients, in ZigZag sequence. It is compliant with ISO DIS 10918-1 Annex A - Section A.3.4.

The quantizer step size for each DCT coefficient S_{uv} is the value of the corresponding element Q'_{uv} from the quantization table Q'.

$$Squv = round\left(\frac{Suv}{Q'uv}\right)$$

Where *uv* is the index of the zigzag coefficient.

Table Q' is a scaled quantization table calculated for table Q as follows:

$$Q' = \frac{Squeeze}{32} \times Q$$

where *Squeeze* is a parameter value.

Table Q is represented in *Figure 9*, as described in ISO DIS 10918-1 Annex K.

Figure 9: Luminance and chrominance quantization tables

$Q = \begin{bmatrix} 16 & 11 & 10 & 16 & 24 & 40 & 51 & 61 \\ 12 & 12 & 14 & 19 & 26 & 58 & 60 & 55 \\ 14 & 13 & 16 & 24 & 40 & 57 & 69 & 56 \\ 14 & 17 & 22 & 29 & 51 & 87 & 80 & 62 \\ 18 & 22 & 37 & 56 & 68 & 109 & 103 & 77 \\ 24 & 35 & 55 & 64 & 81 & 104 & 113 & 92 \\ 49 & 64 & 78 & 87 & 103 & 121 & 120 & 101 \\ 72 & 92 & 95 & 98 & 112 & 100 & 103 & 99 \end{bmatrix}$	$Q = \begin{bmatrix} 17 & 18 & 24 & 47 & 99 & 99 & 99 & 99 \\ 18 & 21 & 26 & 66 & 99 & 99 & 99 & 99 \\ 24 & 26 & 56 & 99 & 99 & 99 & 99 & 99 \\ 47 & 66 & 99 & 99 & 99 & 99 & 99 & 99 \\ 99 & 99 & 99 & 99 & 99 & 99 & 99 & 99 \\ 99 & 99 & 99 & 99 & 99 & 99 & 99 & 99 \\ 99 & 99 & 99 & 99 & 99 & 99 & 99 & 99 \\ 99 & 99 & 99 & 99 & 99 & 99 & 99 & 99 \end{bmatrix}$
Quantization table for Y blocks	Quantization table for U and V blocks

Table 6 shows an example of VGA image when different squeeze values are applied by the user.

Table 6: VGA image size - YUV 4: 2: 2 - Example of image size after JPEG compression

Squeeze	a	2	4	8	10	20	30	50	67
Squeeze quantization table factor (Squeeze/8)		0.12	0.25	0.5	0.62	1.25	1.87	3.12	4.19
File size (Kbyte)	614	~80	~51	~32	~27	~21	~12	~9	~9
Bit per pixel		2.13	1.39	0.85	0.72	0.56	0.32	0.24	0.24

a. No compression

4.4.5 Entropy coder

This block performs the following functions:

- insertion of JPEG Markers
- runlength encoding
- Huffman encoding

4.4.5.1 JPEG markers

These markers are compliant with ISO DIS 10918-1 Annex B.

The output JPEG file includes markers defined in *Table 7*, in order of appearance.

Table 7: JPEG markers included in STV0974 output data stream

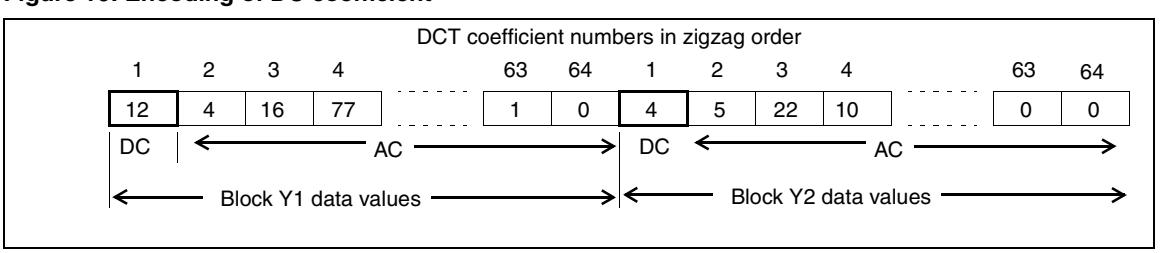
Marker Function	Name	Value
Start of image	SOI	FFD8
Define Quantization Table	DQT	FFDB
Start of frame for baseline DCT	SOF_0	FFC0
Define Huffman Tables	DHT	FFC4
Start of Scan	SOS	FFDA
End of image	End of image	FFD9

4.4.5.2 Runlength and Huffman encoding

Encoding of DC coefficient

The so-called DC coefficient is the first coefficient of each DCT data block. This DC coefficient is coded through its DPCM difference with its previous value, which is huffman encoded. This is described in ISO DIS 10918-1 Annex A - Section F.1.2.1. The DC Huffman tables are described in ISO DIS 10918-1 Annex A - Section K.3.

Figure 10: Encoding of DC coefficient



In the example from *Figure 10*, the DC coefficient in Block Y2 is equal to 4, the previous Luminance DC coefficient is 12 (DC coefficient of Block Y1). The DPCM value is 4-12 = -8 and the encoded value will be Huffman (-8). The code that is generated is Code = DC Huffman (-8).

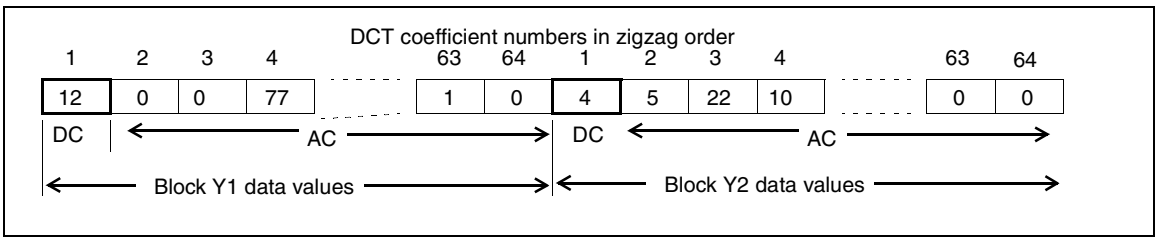
Encoding of AC coefficients

The 63 left coefficients of each DCT block are called AC coefficients. They are encoded using run-length and Huffman encoder. The run-length encoding consists in counting the number of zero values between each non-zero coefficient. When a non zero coefficient is found, the Huffman code of the pair (number of preceding zero, Number value) is Huffman encoded. If a run contains more than 15 zeros, a specific number called ZRL is Huffman encoded.

If all the values up to the end of the block are equal to zero, a specific code called EOB is Huffman encoded.

The Huffman table used are described in ISO DIS 10918-1 Annex A - Section K.3.

Figure 11: Encoding of AC coefficient



In the above example, the first AC coefficient of Block Y1 is 0, as good as the second one. The zeros are not Huffman encoded, but the runlength counts them. When the first non-zero value is reached (Coefficient 4 with value 77), the Huffman code for the pair (number of preceding zeros, value) = (2,77) if Huffman encoded.

The code that is generated is Code = Huffman (2,77).

4.5 Microprocessor interface

4.5.1 Features

- 8-bit microprocessor interface, asynchronous read/write, one address bit
- Indirect access to image sensor and coprocessor control registers
- Direct access to image data (JPEG compressed or uncompressed)
- On-chip 2048 byte image FIFO
- Interrupt request output
- 8/16/32-byte burst DMA support
- 2 Kbyte video FIFO for JPEG data and 10 Kbyte FIFO for non-JPEG data

4.5.2 Description

The STV0974 can be connected to any general purpose 8-bit microprocessor via the microprocessor interface. This interface substitutes functionally to the YUV and I²C interfaces, i.e. both data and control flows are handled through the interface which provides:

- access to the image data FIFO for fast transfers of scaled-down viewfinder images or full-resolution captured and compressed image data. For host systems with DMA support, a DMA request line is provided, as well as programmable FIFO threshold for burst operation. For other systems, an interrupt request output line is provided.The 2048-byte FIFO allows for greater host system latencies; to suit system requirements, the FIFO threshold is programmable.
- access to the camera subsystem configuration and control registers, through an address/data register pair and a status register for data polling. Access requests are posted to the internal controller core that handles the request (as in I²C mode) and finally acknowledges through the microprocessor interface status register.

4.5.3 Direct registers

Access to the microprocessor interface direct registers is controlled by the state of CSN, RDN, WRN and RS (*Table 8*).

Table 8: Microprocessor Interface Direct Registers

CSN	RDN	WRN	RS	Register accessed
0	1	0	0	Address Register (AR)
0	0	1	0	Status Register (SR)
0	1	0	1	Data Write register (DW)
0	0	1	1	Data Read register (DR)
1	X	X	X	No access

The direct registers are used to access all STV0974 indirect registers and external image sensor registers through I²C. To read from a camera register:

1 Write AR with the indirect register address.

2 Poll the status register RDY bit until high.

3 Read the register data from DR.

To write to a camera register:

1 Write AR with the indirect register address.

2 Write DW with the register data.

3 Poll the status register RDY bit until high.

Note: 1 16-bit values are in little-endian representation, i.e. LSB at lower address.

2 No data polling is required to access the microprocessor interface indirect registers.

Address Register (AR)

The Address Register holds the 16-bit address of the camera register to access. AR is written by two consecutive byte writes, least significant byte first.

Note: To avoid LSB/MSB sequence mismatch, any read access (to DR or SR) guarantees that the following write to AR updates the LSB (ADDR bits 7:0).

Table 9: Address Register

Bits	Name	Type	Description
15	ME	WO	0 = Image sensor register (forward command to I²C master). 1 = STV0974 register.
14	RW	WO	0 = Write access 1 = Read access
[13:0]	ADDR	WO	Camera register address.

Status Register (SR)

The status register is an 8-bit read-only direct register holding all pending requests from the camera subsystem.

Table 10: Status Register

Bits	Name	Type	Description
7	IRQ	RO	Interrupt Request: IRQ is set when at least one of the interrupt sources is set, and the corresponding bit mask is set.
6	-	-	Reserved.
5	EOF	-	End Of Frame: EOF is set by the falling edge of VENV (output image vertical envelope). SOF is cleared by writing ICLR bit 5.
4	SOF	RO	Start Of Frame: SOF is set by the rising edge of VENV (output image vertical envelope). SOF is cleared by writing ICLR bit 4.
3	MCI	RO	Micro-Core Interrupt: MCI is set by the micro-core to alert the host of the occurrence of an internal event (status update, error, etc.…). MCI is cleared by writing ICLR bit 3.
2	FERR	RO	FIFO Error: FERR is set by the FIFO controller if a FIFO overflow occurs, or if the FIFO is not empty when cleared at the start of frame. FERR is cleared by writing ICLR bit 2.
1	FRDY	RO	FIFO Ready: This bit indicates that the number of valid bytes in the FIFO is greater than or equal to the FIFO threshold value, i.e: FRDY = (Nbytes ≥ threshold) During the inter-frame period, ‘threshold’ is forced to ‘1’ to flush the FIFO; otherwise, ‘threshold’ is determined by FHTR. FRDY is level sensitive, i.e. it can be cleared only by reading FIFO.
0	RDY	RO	Ready: This bit indicates the state of the access request between the host and the STV0974: 0 = Register access in progress, 1 = AR, DR and DW can be accessed by the host. For a read access, RDY is cleared upon host write to AR (MSB); it is set by the micro-core when DR is updated with the register data. For a write access, RDY is cleared upon host write to DW; it is set by the micro-core when the internal register is updated. Note: RDY is high when AR points to the interface indirect registers.

Data Write Register (DW)

The data write register contains the byte to transfer to a camera register. DW can be written only when SR bit RDY is set.

Table 11: Data write register

Bits	Name	Type	Description
[7:0]	DW	WO	Data Byte to write to camera subsystem.

Data Read Register (DR)

The Data Read Register contains the byte transferred from a camera register. DR is valid only when SR bit RDY is set.

Table 12: Data Read register

Bits	Name	Type	Description
[7:0]	DR	RO	Data Byte read from the camera subsystem.

4.5.4 Indirect registers

The microprocessor interface indirect registers are accessed by the host using an indirect address base of 0x8FF0 / 0xCFF0 (write / read). Register offsets are listed in *Table 13*:

Table 13: Microprocessor interface indirect register map [a] [b]

Offset	Name	Description
0x00	FIFO	FIFO read register.
0x01	MICR	Microprocessor interface control register
0x02	IMASK	Interrupt mask register
0x03	ICLR	Interrupt clear register
0x04 0x05	FTHR	FIFO threshold register.
0x06 0x07	FCNT	FIFO count register.

a. 16-bit values are in little-endian representation, i.e. LSB at lower address.

b. No data polling is required to access the microprocessor interface indirect registers.

FIFO Register (FIFO)

FIFO is a read-only register. When read, FIFO returns the least recent byte from the image data FIFO, decrements the byte count and releases the FIFO interrupt if the count is lower than the threshold. Reading from an empty FIFO returns the last valid byte read.

The image data FIFO is cleared at the beginning of VENV, the image vertical envelope. If the FIFO is not empty, its contents are discarded and the FERR flag is raised in the status register SR. New image data start to fill in the FIFO. If an overflow occurs during VENV, the FERR flag is also raised in SR; FERR can be cleared through ICLR.

Table 14: FIFO register

Bits	Name	Type	Description
[7:0]	FIFO	RO	Image data byte (uncompressed or compressed).

Microprocessor Interface Control Register (MICR)

MICR controls and configures the image data transfer.

Table 15: Microprocessor Interface Control Register

Bits	Name	Type	Description
[7:6]	-	-	Reserved.
5	IRQPOL	RW	IRQ pin polarity: 0 = active high 1 = active low
4	DRQPOL	RW	DRQ pin polarity: 0 = active high 1 = active low
[3:2]	BSIZE	RW	DMA burst size and enable: 00 = DMA operation disabled, DRQ pin is high impedance 01 = 8-byte burst 10 = 16-byte burst 11 = 32-byte burst
1	-	-	Reserved, read as zero, ignored upon write
0	CLR	WO	Clear FIFO (Write Only, read as 0): 0 = No action 1 = Reset FIFO to empty state

Interrupt Mask Register (IMASK)

Table 16: Interrupt Mask Register

Bits	Name	Type	Description
[7:6]	-	-	Reserved
[5:0]	IMASK	RW	Each IMASK bit set to '1' enables the corresponding interrupt source bit in the status register (SR)

Interrupt Clear Register (ICLR)

Table 17: Interrupt Clear Register

Bits	Name	Type	Description
[7:6]	-	-	Reserved
[5:2]	ICLR	WO	Each ICLR bit written with a '1' clears the corresponding interrupt source bit in the status register (SR). Writing a '0' has no effect
[1:0]	-	-	Reserved

FIFO Threshold Register (FTHR)

Table 18: FIFO threshold register

	Description	
FTRH	Holds the FIFO threshold value	
NE = 1	threshold = 1	(TH is ignored)
NE = 0	threshold = TH * 16	(TH valid range is [1, 2...127])

This register is used to program values such as 1 (flush), 16 or 32 (DMA burst) or any greater value up to 2032 for interrupt driven data transfer. Note that for proper DMA operation, 'threshold' must be greater than or equal to the DMA burst size (MICR[BSIZE]).

Table 19: FIFO Threshold Register

Bits	Name	Type	Description
[15:11]	-	-	Reserved
[10:4]	TH	RW	Threshold value in 16-byte increments.
[3:1]	-	-	Reserved
0	NE	RW	Not Empty: 1 = Force threshold to 1 (TH is ignored) 0 = Normal

FIFO Count Register (FCNT)

FCNT is a read-only 16-bit register, returning the current number of bytes available in the FIFO.

Table 20: FIFO Count Register

Bits	Name	Type	Description
[15:0]	FCNT	RO	Number of bytes available in the image data FIFO.

4.5.5 Image transfer operation

Interrupt controlled transfer

The STV0974 generates interrupts by asserting the IRQ signal. The host interrupt handler performs the following operations:

1 Read the status register SR to determine if the STV0974 is the interrupting device (IRQ bit) and detect the active interrupt sources.

2 Acknowledge pending interrupts by writing ICLR.

3 Service the interrupt source(s), i.e. for example:

MCI: read micro-core status and error registers (camera control channel).

SOF: trigger frame synchronous task.

FF: empty the FIFO by reading 16-byte blocks (camera image data channel).

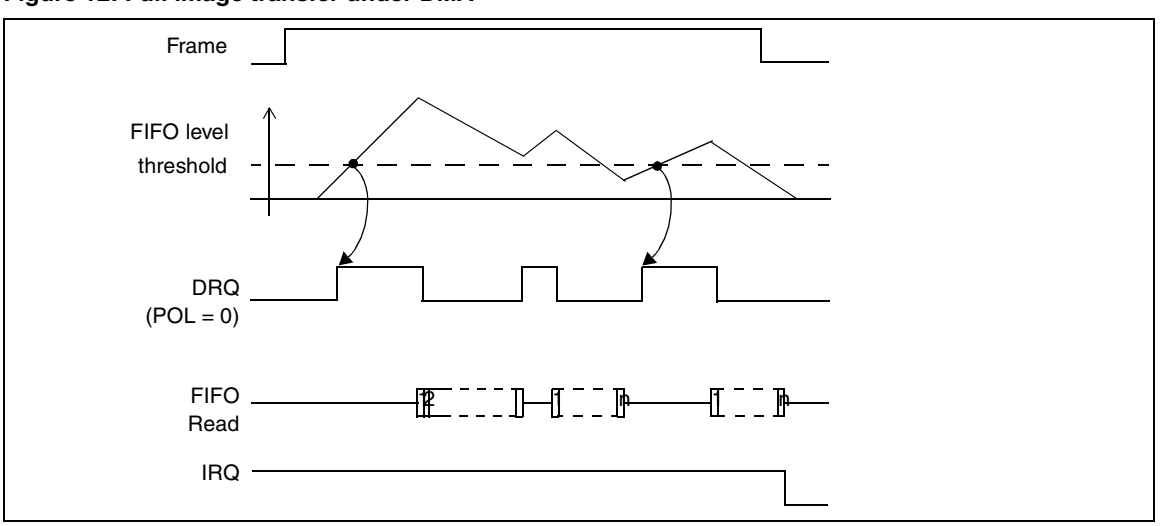
RDY: read DR for a pending read, write next AR (low-level byte transfer).

4 Interrupts can be disabled through IMASK.

DMA controlled transfer

The STV0974 supports DMA operation for image data transfer: the DRQ output signal is used to trigger a DMA burst read transfer from peripheral to memory. A full image transfer under DMA executes as follows:

Figure 12: Full image transfer under DMA



1 The STV0974 is initialized: DMA burst size, FIFO is cleared.

2 DRQ is asserted when the image FIFO threshold is reached or exceeded.

3 The DMA controller starts performing the burst read transfer consisting of 8, 16 or 32 byte reads.

4 DRQ is released after the first byte is read.

5 After the last byte of the burst is read, the transfer terminates on step 6 if the FIFO is empty and the frame end is reached. Otherwise, transfer continues on step 2.

6 IRQ is asserted to signal the end of image transfer; the DMA channel is closed and re-initialized for the next transfer.

This behavior ensures that no request can be missed by the controller, assuming DRQ is an edge-sensitive signal. DRQ polarity can be reversed through MICR[POL] bit.

Note: 1 During DMA transfer, it is assumed that reading DR returns a byte from the FIFO, which means that AR shall be pointing to the FIFO when the DMA channel is active. To access other registers while performing DMA, the DMA controller must be halted and pending transfers properly flushed; then indirect accesses to the camera subsystem can occur. Finally, AR must be restored and the DMA controller released.

2 At the end of the transfer, FIFO underrun can occur if the image size is not an integer multiple of the burst size: dummy bytes are appended at the end of the image buffer. Nevertheless, the JPEG end-of-frame marker (0xffd9) delineates the buffer.

4.6 Video output interface

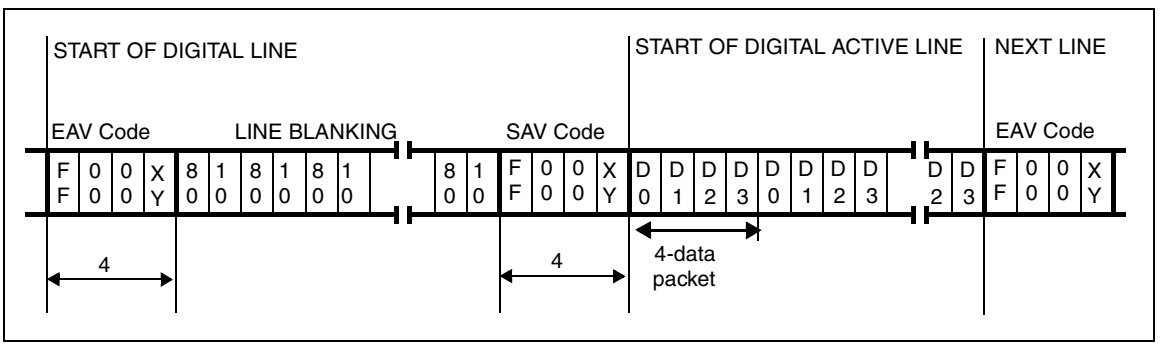
4.6.1 Video synchronization

The STV0974 supports two modes of data stream synchronization. Either the data stream can be synchronized by separate HSYNC and VSYNC signal (see *Section 4.6.3*) or by Synchronization codes in the data stream (see *Section 4.6.2*).

4.6.2 Synchronization codes

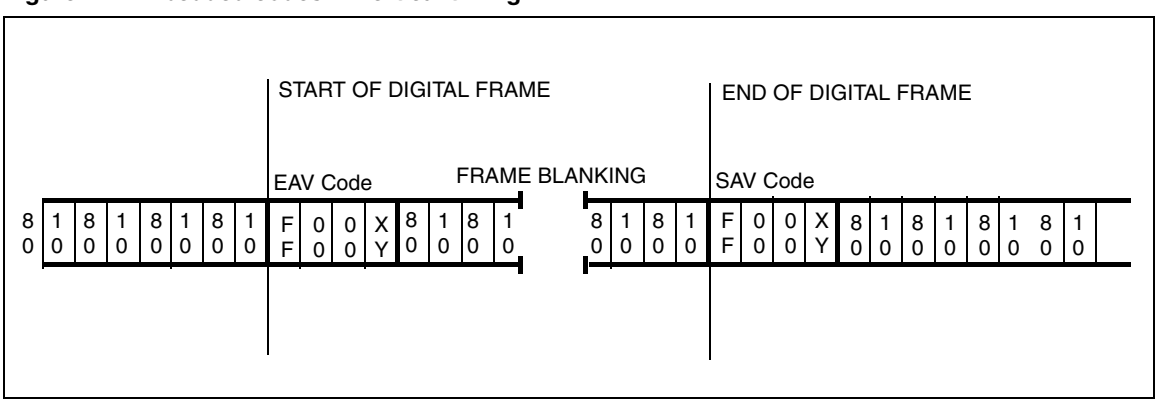
Horizontal synchronization The horizontal synchronization signal can be embedded within the data. *Figure 13* represents the synchronization codes generated in a line.

Figure 13: Embedded code horizontal timing



Vertical synchronization

Figure 14: Embedded codes in vertical timing

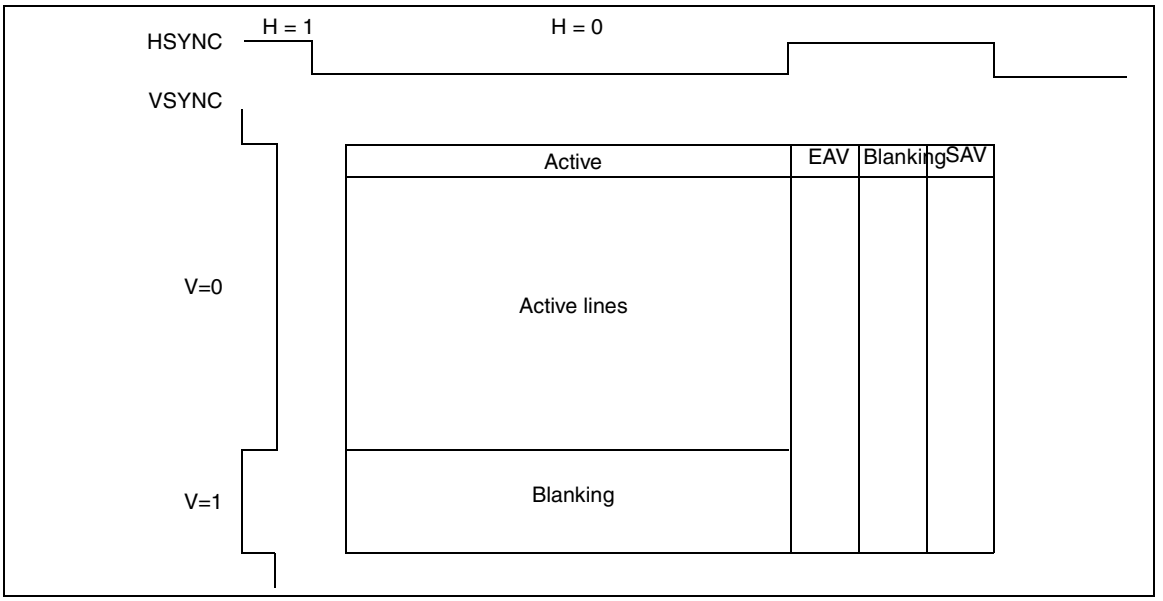


Note: The horizontal synchronization is not sent during vertical blanking.

4.6.3 HSYNC and VSYNC video synchronization

HSYNC and VSYNC synchronization timing is shown in the *Figure 15*.

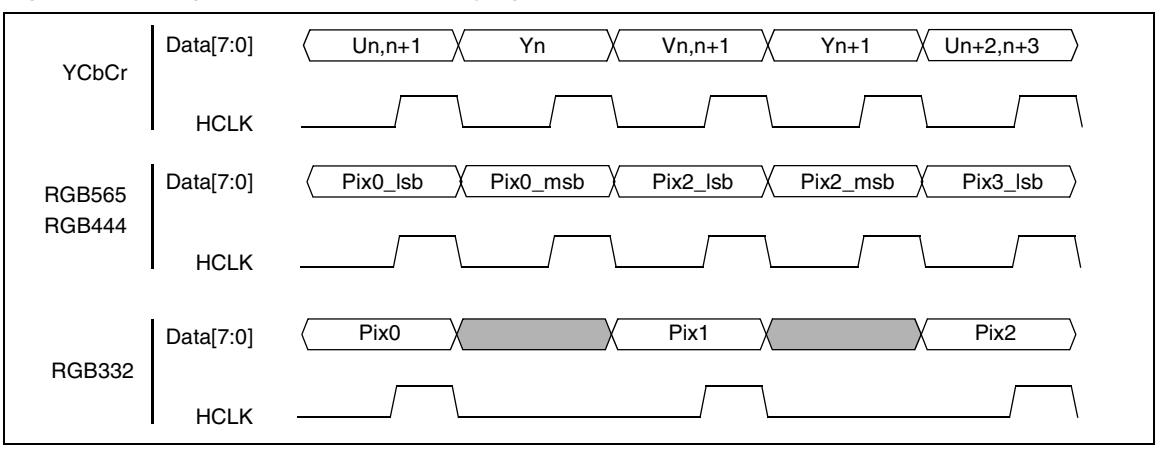
Figure 15: Horizontal and vertical synchronization



4.6.4 Data timing

The YUV timing and the 3 RGB timings are also represented on *Figure 16*, with the associated qualifying HCLK clock.

Figure 16: Timings with associated qualifying clocks

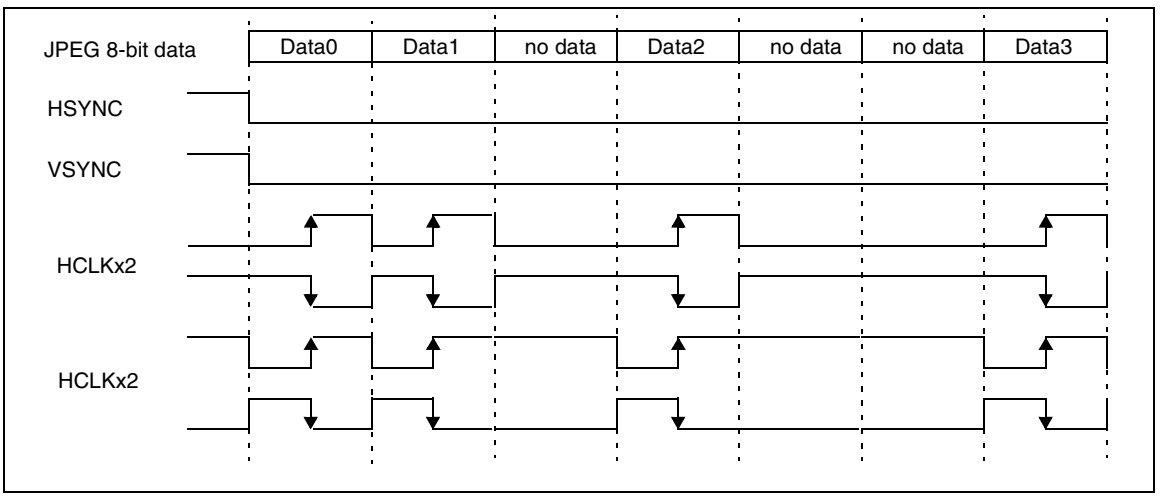


4.6.5 JPEG data on 8-bit parallel with qualification clock

This interface outputs JPEG on parallel 8-bit IOs. Different synchronization can be provided, as described in *Figure 17*.

There are no defined lines in a JPEG data stream. The whole stream is output as a single frame line with VSYNC and HSYNC asserted together.
Polarities of HSYNC, VSYNC and HCLK are programmable.

Figure 17: JPEG data output



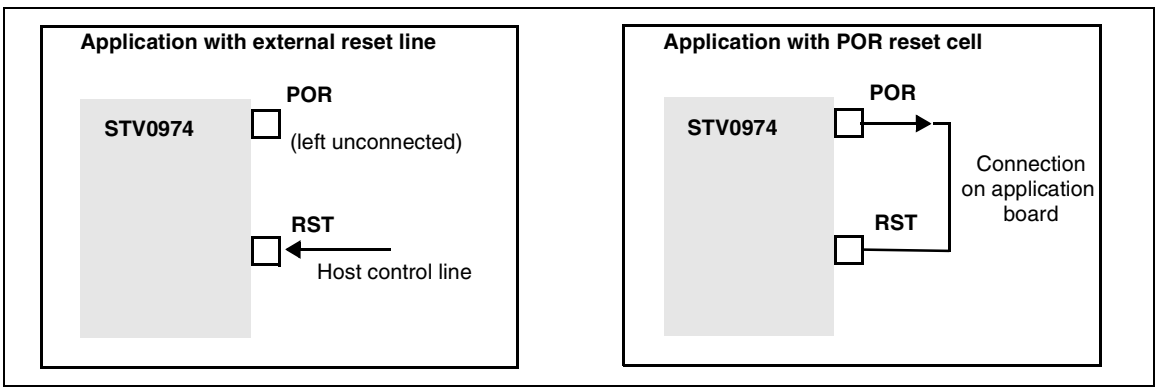
Extra bytes can be added at the end of the image to ease the host DMA task.

4.7 Power management unit

The STV0974 is reset via the internal PowerOnReset cell (POR) or via an external control reset line. The device reset is controlled by the RST pin.

The POR cell generates an output signal on the POR pin every time that the device external supply is switched off or the PDN pin is activated.

Figure 18: Reset of STV0974



The STV0974 enters into power-up phase in two circumstances:

- when the supplies are turned on with PDN pin high.
- when the STV0974 exits from power-down (PDN pin rises with supplies already on).

At power-up, the STV0974 performs its initialization phase and goes into sleep mode.

Figure 19: State machine at power-up

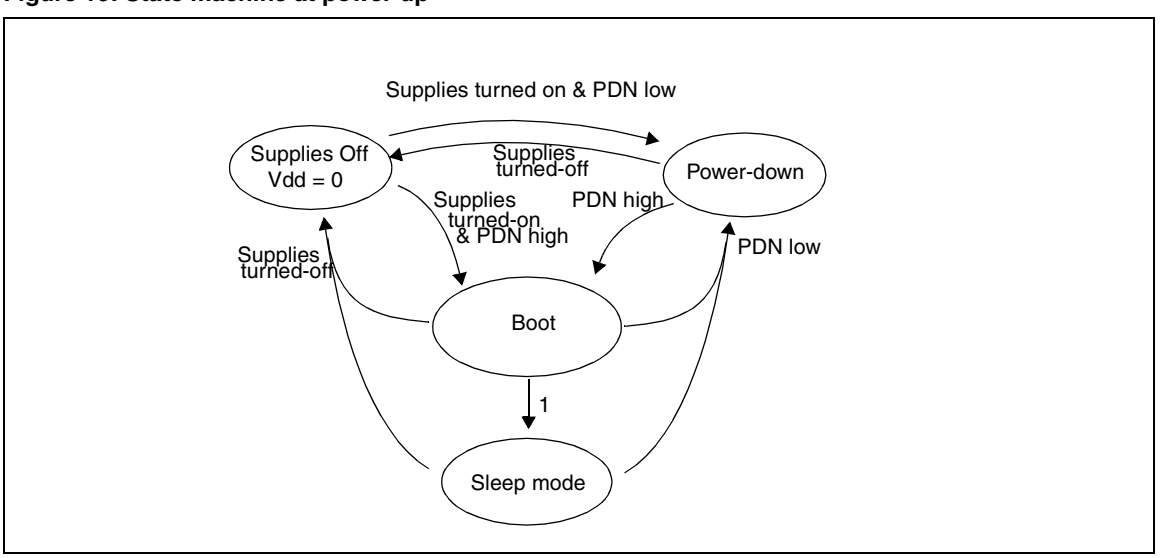
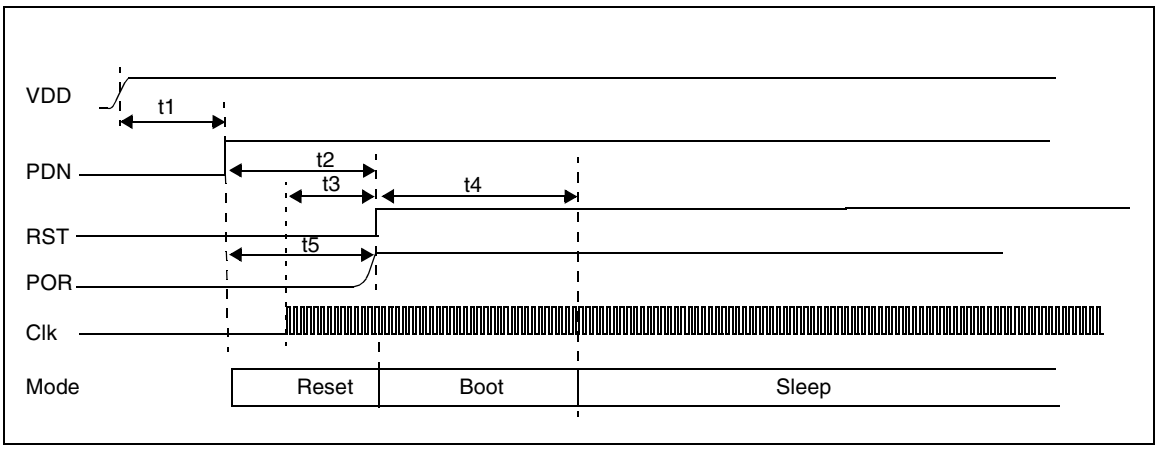


Figure 20: Boot-up phase machine



Timing constraints:

Table 21: Timing constraints

	Min.	Max.	Unit
t1	0		ms
t2	20		µs
t3	20		clk cycles
t4	2		ms
t5	7		µs

Note: To be compatible with external power-on/internal power-down modes (ex: external VDD on and PDN low), all input pads from baseband side as well as SCL and SDA pads on both sensor and baseband sides are "fail-safe".

The "timing constraints" mentioned above correspond to the minimum delay needed between signals, in order to follow a correct power up sequence and insure an adequate initialization phase.

Referring to the application schematics (*Section 8*), STMicroelectronics recommends to connect POR pin (internal supply) to RST pin (Reset).

4.8 Clock input

This block generates all the necessary internal clocks from an input range defined in *Table 22*. The input clock pad accepts up to 26 MHz signals.

Table 22: System input clock frequency range

System clock frequency[a]	
Min. (MHz)	**Max. (MHz)**
6.5	26

a. Standard supported input frequencies (in MHz):
6.5, 8.4, 9, 9.6, 9.72, 12,13, 16.8, 18, 19.2, 19.44, 26

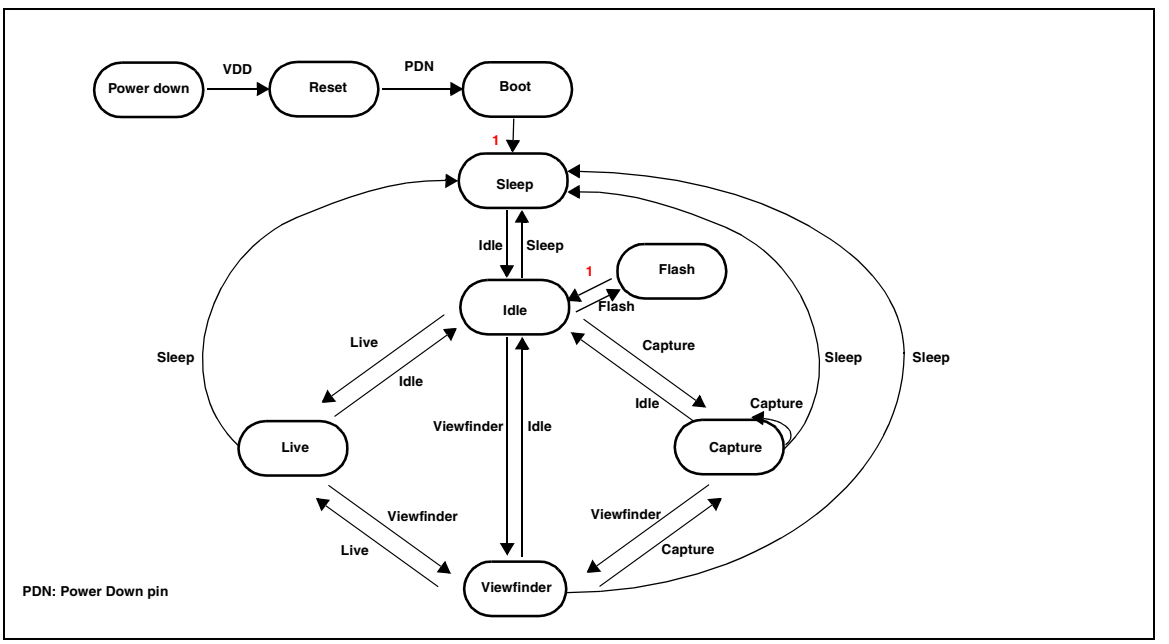
4.9 Camera control unit

4.9.1 Features

- User mode transition
- I^2C register map including high-level registers and low-level registers dedicated to scaler control

4.9.2 Description

Figure 21: State machine user mode transitions



i. the “1” transition is automatic

ii. Flash mode requires a firmware patch. Contact ST support.

iii. Flash mode is not available with the microprocessor interface

Modes

Power down ●Supply is internally cut.

Reset. Transitional state

Boot ●

Sleep mode This mode ensures that the coprocessor consumes the lowest possible power and I^2C control is possible. Patching should occur in sleep mode followed by setting the system clock parameters.

Idle Mode The clock coming from the sensor is active and I^2C control is possible.

Viewfinder Mode The viewfinder mode can be used to display dithered images on low color depth local LCD displays. The programmable gamma allows for a wide range of displays. Different image sizes and data formats can be chosen.

Still Mode This mode is used to take still pictures. Still picture parameters can be set for both image size and data format. the first image output has a guaranteed exposure and color balance. the number of frames output can also be set.

Live Mode Live clips can be generated in all the data and image formats.

Flash Mode Flash mode is used to take a single still picture and synchronously activate a flash gun signal and illuminate the scene during the exposure period of the pixels.

Torch Mode For systems without a flash gun, a torch mode can replace the flash mode. Torch mode is a setting (rather than a mode) which supports illumination of devices by producing a longer illumination pulse with a lower intensity. In torch mode, illumination is switched on before the camera is operated in one of the standard operating modes: ViewFinder, still capture or live.

Mode transitions

Boot to sleep The microcore starts following PDN de-activation. The right configuration is obtained according to the following procedure:

1 Determine the sensor I^2C chip address.

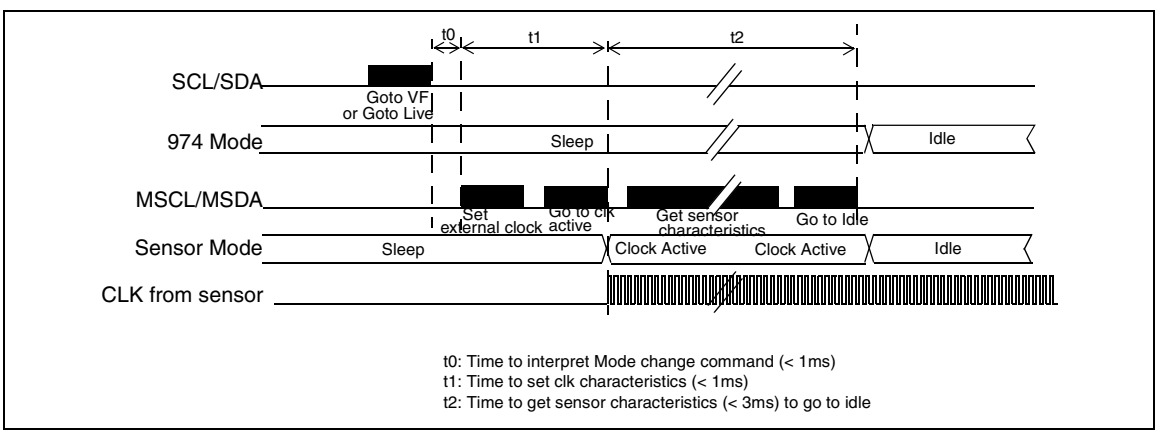
2 Read all sensor registers, either through I^2C reads or status line interpretation.

3 Initialize internal registers.

The device then automatically goes into sleep mode

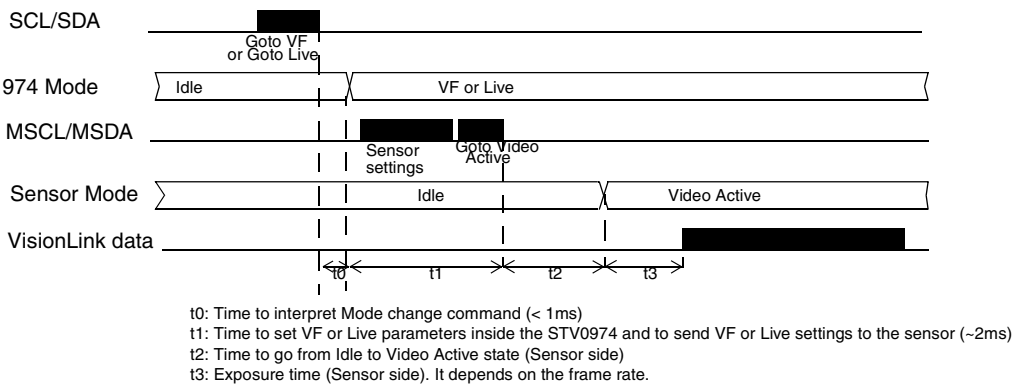
Sleep to idle When exiting sleep mode, the external clock register of the sensor is set, and the sensor goes into Idle mode.

Figure 22: Sleep to idle timing



Idle to viewfinder / live The sensor field and line lengths are set according to user-defined frame rate and data output format. The STV0974 processes all sensor data on the fly. Exposure and white balance controls are computed at the end of each frame.

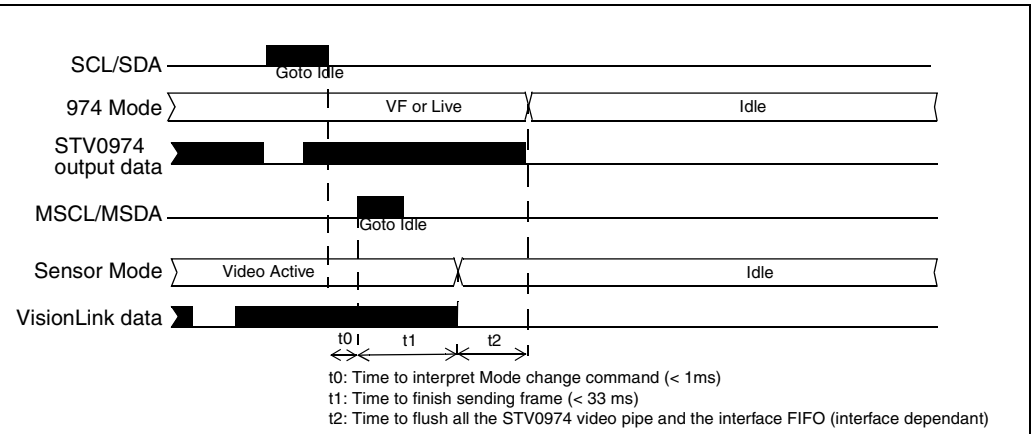
Figure 23: Idle to viewfinder or live



Viewfinder / live to idle

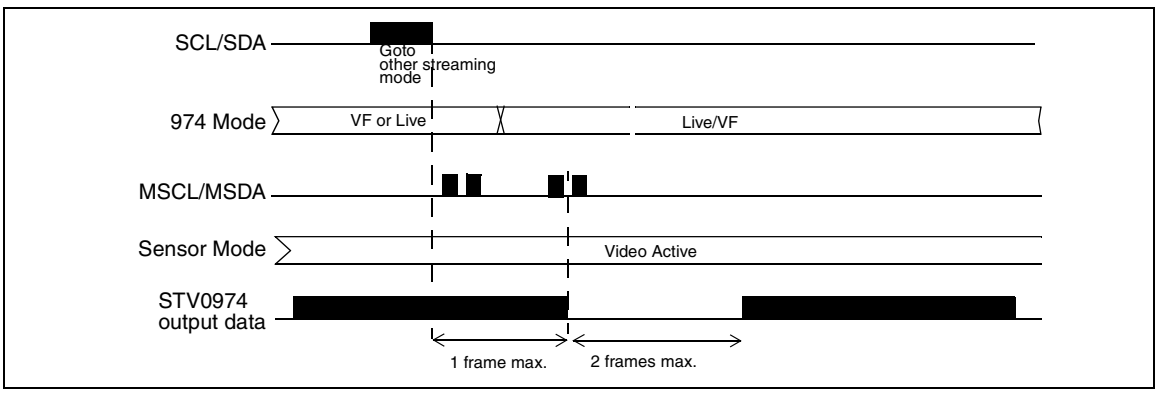
The STV0974 processes all the frame data and switches to idle mode after the last byte. See *Figure 24* below.

Figure 24: Viewfinder or live to idle timing



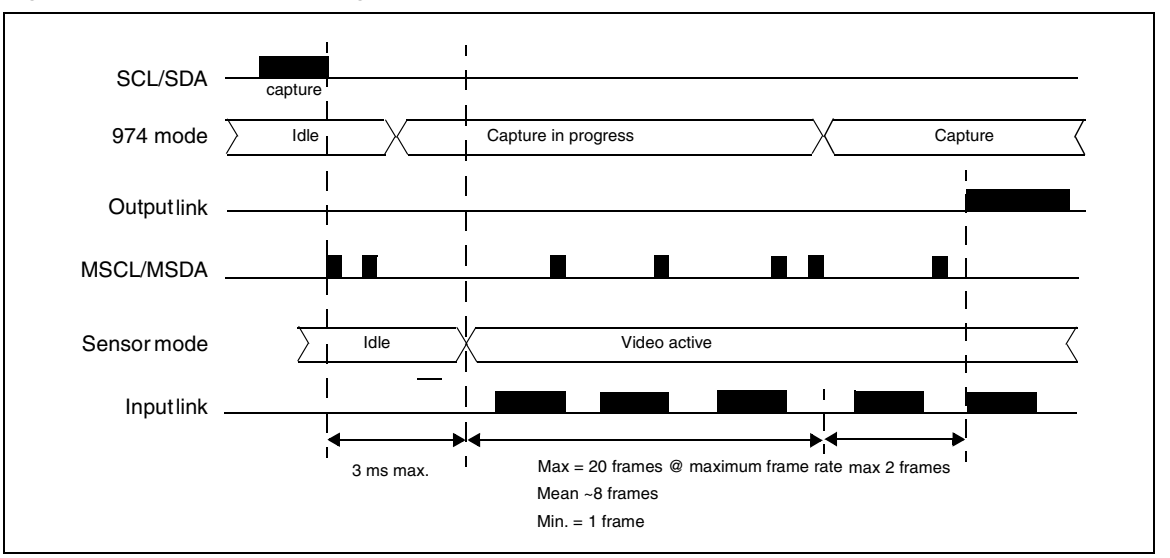
Viewfinder to live/ Live to viewfinder The sensor field and frame lengths are set according to the user defined Live/Capture frame rate and data output format. The latency of this transition is minimal. See *Figure 25* below.

Figure 25: Viewfinder to live or live to viewfinder



Idle to capture Data is grabbed as fast as possible for exposure and white balance convergence. When the system is stable (or timed-out), the user settings are sent to the sensor. See *Figure 26*.

Figure 26: Idle to capture timing



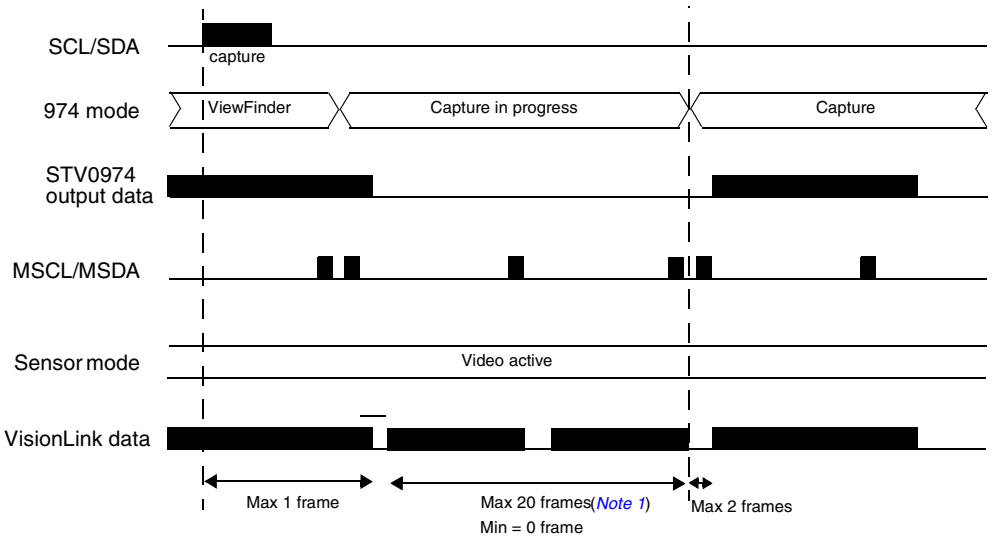
Viewfinder to capture Two cases can occur:

1 The system (exposure, white balance) is already stable in viewfinder mode. The user settings are sent to the sensor. The processed frame is sent after a short latency.

2 The system has not stabilized. STV0974 enters transient mode and, when stable, automatically goes into Capture mode.

Once the image is sent, the STV0974 automatically returns to Idle. See *Figure 27*.

Figure 27: Viewfinder to capture timing

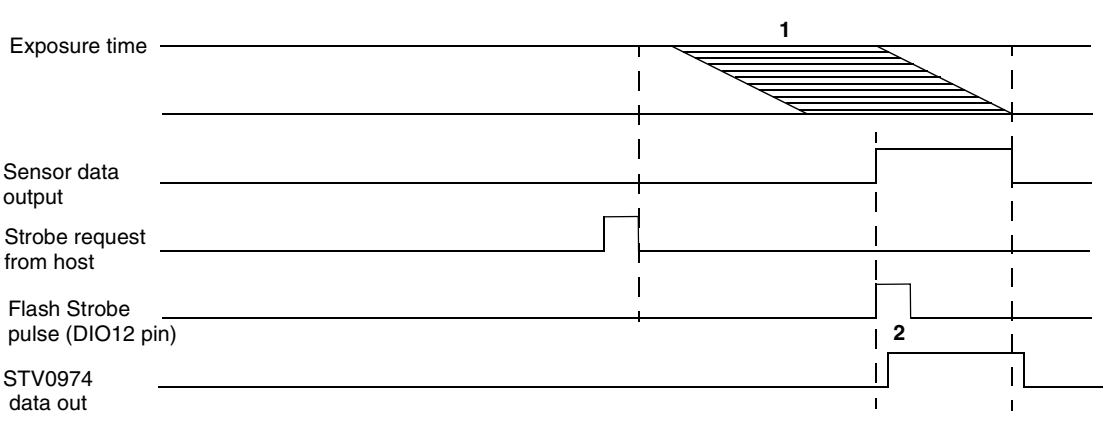


Note: 1 If the system exposure and white balance is already stable, the maximum delay is 1 frame.

Idle to Flash In idle mode, white balance must be set to a fixed setting (automatic white balance setting is not recommended as no convergence is applied) and the “delay transfer mode” must be set to 0 (no frame delay). When changing to flash mode, the maximum frame rate is automatically set with respect to data format. The first frame is captured, processed and transferred by the STV0974. The system automatically goes back to idle mode. *Figure 28* illustrates the timing in flash mode.

When setting the torch mode, the flash mode should not be used. All the standard operating modes like ViewFinder, still capture or live operate normally. As an example, the automatic white balance and exposure control as well as “delay transfer mode” can be active if required.

Figure 28: Flash mode diagram



1 Exposure time of pixels is automatically set to maximum exposure time

2 Strobe pulse width is clipped to a maximum of 8 lines

4.9.3 I²C register map

Register interpreter

The STV0974 I²C address is 0x08.

The addressing space is defined in *Table 23* and *Table 24*.

Table 23: Fields of address map

Index Bit	Description
15	bit15 = 0: reserved for the sensor bit15 = 1: STV0974
14	Pre-fetch read value
13	0: low-level register 1: high-level register
[12-8]	Page group
[7-0]	Register index

The customer accessible register map is divided into groups as listed in *Table 24*.

Table 24: Register groups

Group	Description
Register group [0]	- System read only registers (e.g. sensor ID, firmware revision) - System clock setup - High level operating modes - Output format control
Register group [1]	- Frame rate control - Image sizes - Stills capture setup
Register group [2]	- Image appearance setup - Image manipulation - JPEG control
Register group [3]	- Color saturation - Gamma control
Register group [4]	- Exposure control setup
Register group [5]	- White balance control
Register group [6]	- Flash mode management

There are restrictions related to the states at which registers can be accessed. *Table 25* lists the state coding used in the register description.

Table 25: Register state coding

State code	Description
I	Registers can be accessed safely while the system is in idle state
V	Registers can be accessed safely while the system is in ViewFinder state
C	Registers can be accessed safely while the system is in capture mode state
L	Registers can be accessed safely while the system is in live mode state
S	Registers can be accessed safely while the system is in sleep mode state
A	Registers can be accessed in all stable states

Register contents represent different data types as described in *Table 26*.

Table 26: Type of data

State Code	Description
I	Integer parameter. May be anywhere between 1 bit and 8 bit wide
M	Multiple field registers
B	Bit field register
C	Coded register

Registers listed as reserved or read-only should NOT be written to, as this may cause unpredictable results.

The data format for each register uses the following coding:

- D = Data (1 or 0 as required)
- 0 = Data bit must be set to 0
- 1 = Data bit must be set to 1
- X = Don’t care (either 0 or 1 can be written with no system consequences)
- R = Reserved

4.9.3.1 High-level interface

Register group 0

Table 27: System and status [register group 0]

Name	Index	R/W	State code	Data type	Format *default*	Description
Sensor ID Code MSB	0xA000	R	A	I	DDDD.DDDD *0010.0010*	Bit[15:4]: sensor type Bit [3:0]: Sensor revision
Sensor ID Code LSB	0xA001	R	A	I	DDDD.DDDD *1000.XXXX*	
Firmware Rom Version	0xA002	R	A	I	DDDD.DDDD *0001.0100*	Firmware version identifier
External Clock Frequency MSB[a]	0xA004	R/W	S	MI	RRDD.DDDD *1101.0000*	External clock frequency in MHz coded as fixed point (5:11): Bit [15:11]: Integer part Bit [10:0]: Decimal part (1 unit = 1/2048 MHz) i.e. default value is 26MHz.
External Clock Frequency LSB	0xA005	R/W	S	MI	RRDD.DDDD *0000.0000*	
Sensor Clock Derating	0xA006	R	S	I	RRRR.DDDD *0000.0001*	Sensor clock derating[b] [15-0]: Reserved
Mode Status	0xA007	R	A	I	RRRR.DDDD	[15]: Booting [14-7]: Reserved [6]: Flash [5]: Capture in progress [4]: Live [3]: Capture [2]: Viewfinder [1]: Idle [0]: Sleep
Mode Control	0xA008	R/W	A	I	RRRR.DDDD *0000.0000*	[15-7]: Reserved [6]: Flash [5]: Reserved [4]: Live [3]: Capture [2]: Viewfinder [1]: Idle [0]: Sleep
Status Register	0xA009	R	A	I	DDDD.DDDD *0000.0000*	STV0974 status (*Table 10*)

Table 27: System and status [register group 0]

Name	Index	R/W	State code	Data type	Format *default*	Description
Input / Output Protocol Control	0xA00A	R/W	S	I	RDDD.RDDD *0001.0100*	Bit [7]: Reserved Bit [6:4]: Input 0: Reserved 1: VisionLink 2-3: Reserved 4: Color bars generator Bit [3]: Reserved Bit [2:0]: Output 0: Reserved 1: Reserved 2: I^2C/ITU-R 656 embedded synchro 3: I^2C /ITU-R 656 external synchro I^2C / JPEG parallel output 4: Microprocessor interface controller / microprocessor interface 5: Reserved

a. See *Clock input* section, for standard external clock frequencies supported.

b. The product limitation in derating mode is :
2: Half Speed -> Max I2C clock is 200 kHz
4: Quarter Speed -> Max I2C clock is 100 kHz

Register group 1

Table 28: Image characteristics [Register group 1]

Name	Index	R/W	State code	Data type	Format *default*	Description
Still and Live Sensor Frame Rate[a]	0xA100	R/W	S I V	I	DDDD.DDDD *0011.1100*	Frame rate coded as fixpoint (6:2): Bit [7:2]: Integer part Bit [1:0]: Decimal part (1 unit = 0.25 frame/s) Default is 15 frame/s
Still and Live Output Image Size	0xA101	R/W	A	I	RRRR.RDDD *0000.0000*	[7]: Custom [b] [6]: QQCIF [5]: SubQCIF [4]: QQVGA [3]: QCIF [2]: QVGA [1]: CIF [0]: VGA
Still and Live Output Image Format	0xA102	R/W	S I V	I	RRRR.RDDD *0000.0100*	[4]: JPEG [3]: YUV 4:2:2 [2]: RGB 5:6:5 [1]: RGB 4:4:4 [0]: RGB 3:3:2
Still Multi-frames Transfer Mode	0xA103	R/W	S I V L	B	DDDD.DDDD *0000.0001*	0... 254: 0...254 frame(s) 255: continuous.
Delay transfer Mode	0xA104	R/W	S I	B	DDDD.DDDD *0000.0000*	0... 254: Minimum number of frames (at 30 frame/s) to wait for before sending the requested still one. 255: Reserved
Viewfinder Frame Rate (STV0974 input)[a]	0xA105	R/W	S I L C	I	DDDD.DDDD *0011.1100*	Frame rate coded as fix point (6:2)[a]: bit [7:2]: Integer part bit [1:0]: Decimal part (1 unit = 0.25 frame/s) Default is 15 frame/s
Viewfinder Image Size	0xA106	R/W	A	I	RRRR.RDDD *0000.0101*	[7]: Custom[b] [6]: QQCIF [5]: SubQCIF [4]: QQVGA [3]: QCIF [2]: QVGA [1]: CIF [0]: VGA

Table 28: Image characteristics [Register group 1]

Name	Index	R/W	State code	Data type	Format *default*	Description
Viewfinder Image Format	0xC107	R/W	S I L C	I	RRRR.RDDD *0000.0011*	[4]: JPEG [3]: YUV 4:2:2 [2]: RGB 5:6:5 [1]: RGB 4:4:4 [0]: RGB 3:3:2

a. The corresponding frame rates are considered as targets. If the target cannot be achieved due to derated sensor clock or output format versus output protocol, the closest possible frame rate is achieved, knowing that 30 frame/s is the highest frame rate supported by the device.

b. For custom output sizes, please refer to *Section 4.6*. When continuous mode is selected (255), the grabbed image is output until the mode control register is modified.

Register group 2

Table 29: Image control [register group 2]

Name	Index	R/W	State code	Data type	Format *default*	Description
Antivignetting Correction	0xA200	R/W	A	I	RRRR.DDDD *0000.0110*	Correction in tens of percentage 0: 0% 10: 100%, >10: Frozen
DEFCOR control	0xA201	R/W	A	M	DXXX.XXXX XDXX.XXXX XXDX.XXXX XXXD.DXXX XXXX.XDDD *1010.0111*	Bit[7]: Defect correction matrix (default is square matrix) Bit(6]: Defect correction enable (correction of bad pixels) Bit[5]: Defect scythe enable (Smooth filtering of good pixels) Bit[4:3]: Defect scythe rank (default is 0, maximum value means narrow filter) Bit[2:0]: Defect scythe weight (default is 7, maximum value means minimum weight applied)
NORA control	0xA202	R/W	A	I	RRRR.RDDD *0001.0010*	Nora control register. [0]: Nora disabled [7]: Nora max strength Default is 2
Mirror	0xA203	R/W	S I	B	RRRR.RRXD RRRR.RRDX *0000.0000*	Horizontal mirror Vertical mirror
Sharpness Gain	0xA204	R/W	A	I	00DD.DDDD *0000.1100*	Sharpness gain
Sharpness Enable	0xA205	R/W	A	B	RRRR.RRRD *1111.1101*	Sharpness enable Bit[7:2]: low peak Bit[1:0]: reserved
JPEG Control	0xA206	R/W	A	I	RDDD.DDDD *0011.1110*	Bit [7]: JPEG control 0: Automatic file size computation 1: Manual squeeze control Bit [6:0]: Control settings if bit[7] = 0: Requested size of final JPEG file (in Kbyte) if bit [7] = 1: Manual squeeze control with quantization table scaled by bit [6:0]/8. Applicable range of values for bit [6:0] is [2; 67]

Register group 3

Table 30: Color management [register group 3]

Name	Index	R/W	State code	Data type	Format *default*	Description
Still / live Gamma Standard Gain	0xA300	R/W	A	I	RRRR.DDDD *0000.0011*	Bit[3:0]: gain for standard Gamma curve
Still / live Gamma S-Curve gain	0xA301	R/W	A	M	XXXX.DDDD DDDD.XXXX *0100.0100*	Bit[3:0]: Gain for low S-curve part Bit[7:4]: Gain for high S-curve part
Still / live Gamma Misc.	0xA302	R/W	A	M	XRRR.DDDD DRRR.XXXX *1000.0000*	Bit[3:0]: S-curve pedestal bit [7] = 1 Standard Gamma bit[7] = 0 S-curve Gamma
Viewfinder Gamma Standard Gain	0xA303	R/W	A	M	RRRR.DDDD *0000.0100*	Bit[3-0]: Gain for standard Gamma curve
Viewfinder Gamma S-Curve gain	0xA304	R/W	A	M	XXXX.DDDD DDDD.XXXX *0100.0100*	Bit[3-0]: Gain for low S-Curve part Bit[7-4]: Gain for high S-Curve part
Viewfinder Gamma Misc.	0xA305	R/W	A	M	XRRR.DDDD DRRR.XXXX *1000.0000*	Bit[3:0]: S-curve pedestal bit [7] = 1 Standard Gamma bit [7] = 0 S-curve Gamma
YCbCr Control Y range	0xA306	R/W	A	I	DDDD.DDDD *1000.0000*	Y range value (contrast enhancement)
YCbCr Control Y ceiling	0xA307	R/W	A	M	DDDD.XXXX *0001.0000*	Bit[7:4]: Ceiling value
YCbCr Control Y floor	0xA308	R/W	A	M	DDDD.XXXX *0000.0000*	Bit[3:0]: Floor value (signed value in 2's complement)
YCbCr Control CbCr saturation[a]	0xA309	R/W	A	I	DDDD.DDDD *1000.0000*	CbCr saturation

a. The maximum register value allowed is 144. For higher saturation capabilities, contact ST support.

Note: YCbCr control registers are common for still/live and ViewFinder modes. As a consequence, if different settings are applied in these modes and if for example still capture is requested from ViewFinder mode, it is recommended to set a "transfer mode delay" corresponding to 1 frame minimum, and also to respect a minimum wait of half of a frame prior to changing the YCbCr settings.

Register group 4

Table 31: Exposure management [Register group 4]

Name	Index	R/W	State code	Data type	Format *default*	Description
AC Frequency	0xA400	R/W	S I	B	DDDD.DDDD *0011.0010*	AC Frequency in Hz
Exposure weighting	0xA401	R/W	A	I	RRRR.RRDD *0000.0000*	Zone weight: [3]: Reserved [2]: Backlit [1]: Centered [0]: Flat
Exposure compensation	0xA402	R/W	A	I	DDDD.DDDD *0001.1001*	One unit of compensation is equivalent to 1/3 EV. Default value is equivalent to 0 EV. [Default - 2] is equivalent to -2/3 EV. Valid range is 0 to 36

Register Group 5

Table 32: White balance management [register group 5]

Name	Index	R/W	State code	Data type	Format *default*	Description
White Balance Mode	0xA500	R/W	A	I	RRRR.DDDD *0000.0001*	[15-9]: Reserved [8]: Reserved [7]: Reserved [6]: Reserved [5]: Reserved [4]: User manual (using registers below) [3]: Reserved [2]: Reserved [1]: Automatic [0]: Off
Manual White Balance Red channel	0xA501	R/W	A	C	DDDD.DDDD *0000.0000*	White balance user setting for the red channel gain. Contact ST for support.
Manual White Balance Green channel	0xA502	R/W	A	C	DDDD.DDDD *0000.0000*	White balance user setting for the green channel gain. Contact ST for support.
Manual White Balance Blue channel	0xA503	R/W	A	C	DDDD.DDDD *0000.0000*	White balance user setting for the blue channel gain. Contact ST for support.

Register Group 6

Table 33: Flash mode management [register group 6]

Name	Index	R/W	State code	Data type	Format *default*	Description
Torch polarity	0x8A43	R/W	I	I	RRRR.RDDD *RRR.R000*	Bit[2:0]=0: Torch output (pin DIO12) signal is low Bit[2:0]=7: Torch output (pin DIO12) signal is high
Torch control	0x8A44	R/W	I	I	RDRR.RRRR *R1RR.RRRR*	Bit[6]=0: Torch output (pin DIO12) pad enable. Bit[6]=1: Torch output (pin DIO12) pad in high impedance
Flash pulse polarity	0x8A45	R/W	I	I	RDRR.RRRR *R0RR.RRRR*	Bit[6]=0: Flash pulse active high. Bit[6]=1: Flash pulse active low.
Flash pulse length	0x88D4	R/W	I	I	RRRR.RDDD *0000.0000*	Bit[2:0]: line length - 1 Default is 0, corresponding to 1 video line (maximum pulse allowed is 8 video lines).

Note: Access to the bits mentioned here above is done through a read-modify-write sequence. As an example, when torch mode is set:
- when in idle mode:
set 0x8A44 bit[6] to 0 to enable the torch mode
set 0x8A43 bit[2:0] to 7 to light the torch (if the torch is active high)
- go into required Active mode (still/live or ViewFinder):
set 0x8A43 bit[2:0] to 0 to extinguish the torch

In the case of flash mode:
- when in idle mode:
set 0x8A45 bit[6] to 1 to set the flash pulse active low (default setting is flash pulse active high)
set 0x88D4 bit[2:0] to 7 to set the flash pulse length to 8 video lines
set 0xA104 bit [7:0] to 0 to set 0 transfer frame delay
set 0xA500 bit[3:0] to 5 to set white balance to “daylight” fixed setting
- go into flash mode:
the system automatically goes back to Idle.

4.9.3.2 Low-level interface

Scaler low-level control

These registers are active only if either "*Still and Live Output Image Size*" or "*Viewfinder Image Size*" registers are set to "custom" size.

Table 34: Scaler low-level control

Name	Index	R/W	State code	Data type	Format *default*	Description
Source centre X-position MSB	0x8060	R/W	A	I	RRRR.RRDD *0000.0001*	X-coordinates of the centre of the source image window. Default is 322
Source centre X-position LSB	0x8061	R/W	A	I	DDDD.DDDD *0100.0010*	
Source centre Y-position MSB	0x8062	R	A	I	RRRR.RRDD *0000.0000*	Y-coordinates of centre of the source image window. Default is 242
Source centre Y-position LSB	0x8063	R	A	I	DDDD.DDDD *1111.0000*	
Viewfinder Dest. Image Width MSB	0x8064	R/W	A	I	RRRR.RRDD *0000.0000*	Width of the destination image (after scaling) in viewfinder mode. The value must be a multiple of 8 pixels.
Viewfinder Dest. Image Width LSB	0x8065	R/W	A	I	DDDD.DRRR *1010.0000*	
Viewfinder Dest. image height MSB	0x8066	R/W	A	I	RRRR.RRDD *0000.0000*	Height of the destination image (after scaling) in viewfinder mode. This value must be a multiple of 8 pixels.
Viewfinder Dest. image height LSB	0x8067	R/W	A	I	DDDD.DRRR *0111.1000*	
Viewfinder Scaling factor	0x8068	R/W	A	I	RRRR.RDDD *0000.0100*	Scaling factor in viewfinder mode: [0]: Reserved [1]: x1 [2]: x2 [3]: x3 [4]: x4 (default) [5]: x5 [6]: x6 [7]: x1.5 [8]: x2.5
Still/Live Dest. Image Width MSB	0x8069	R/W	A	I	RRRR.RRDD *0000.0010*	Width of the destination image (after scaling) in still / live mode. This value must be a multiple of: - 2 pixels in YUV output format - 16 pixels in JPEG output format Registers only used for Capture when in idle mode
Still/Live Dest. Image Width LSB	0x806A	R/W	A	I	DDDD.D000 *1000.0000*	
Still/Live Dest. image height MSB	0x806B	R/W	A	I	RRRR.RRDD *0000.0001*	Height of the destination image (after scaling) in still / live mode. This value must be a multiple of 8 pixels. Registers only used for Capture when in idle mode
Still/Live Dest. image height LSB	0x806C	R/W	A	I	DDDD.D000 *1110.0000*	

Table 34: Scaler low-level control

Name	Index	R/W	State code	Data type	Format *default*	Description
Still / Live Scaling factor	0x806D	R/W	A	I	RRRR.RDDD *0000.0001*	Scaling factor in Still/Live: 0: Reserved 1: x1 (Default) 2: x2 3: x3 4: x4 5: x5 6: x6 7: x1.5 8: x2.5

Note: If the scaling factor it too high and the cropped image size is bigger than the full source image, the scaling factor is automatically set to the closest possible high value.

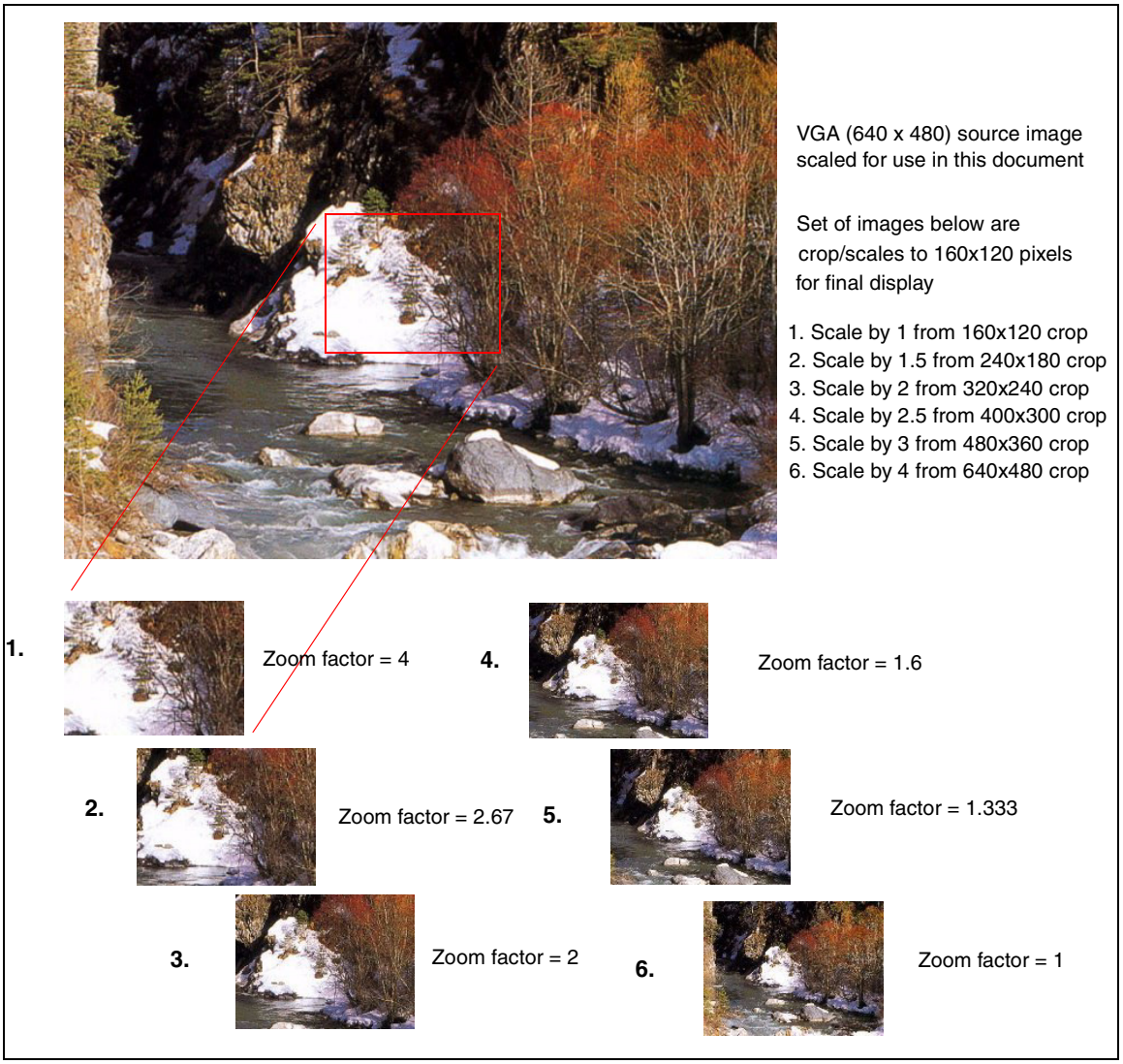
MMS Downscale zoom

This section contains an example of how the low level scalar registers can be used to implement a down scale ‘zoom’ feature suitable for MMS applications. The example assumes that the desired output image size is 160 x 120 pixels. The choice of output image size will limit the number of scaling options available. In this example we are able to select scaling factors 1, 1.5, 2, 2.5, 3 and 4. The source image from which the scaled output images are derived is always the full VGA array, 640 x 480 pixels.

If a smaller output image is chosen, 96 x 80 for example, then clearly the entire scaling factor range would be available.

With reference to the example below (*Figure 29*), a scaling factor of 4 actually yields a ‘zoom’ of 1. This implies that the full scene field of view is preserved within the output image but heavily scaled. To ensure that the smaller scaling factors produce the same output image size it is necessary for the video processor to crop the source VGA image prior to scaling. This has the effect of limiting the scene field of view but yields the ‘zoom’ effect.

Figure 29: MMS crop zoom example



4.9.3.3 Status error codes

A read from the Status Register (0xA009) yields status error codes as described in the table below. The Status Register contents are reset to 0x00 by a write to the Mode Control register.

Table 35: Status error codes

Error code value	Description	Troubleshooting
0x00	No error	
0x21	Sensor communication problem	Sensor not responding. Need to go back to Idle.
0x22	Sensor temporarily not accessible. Retry.	
0x23	Incompatible sensor	Re-grab new image
0x41	JPEG File too big	One of the requested JPEG frames is larger than the target. User to restart capture command
0x51	Time out	

4.9.3.4 Firmware patching

The STV0974 has some firmware patching capabilities addressable through I^2C and microprocessor interfaces through control registers firmware patch code downloads. Up to 15 different patches can be downloaded within a limit of 512 bytes of RAM.

Table 36 : Patch control registers

Name	Index	R/W	Format default	Description
Patch enable	0x84BF	W	RRRR.RRDD	bit [1:0] = 01 patch enabled bit [7:2] = 10 patch disabled
Patch address	0x8480 Ox8481	W	RRRR.RRRR RRRR.RRRR	bit [15:0] = Reserved Patch address delivered by ST
Patch memory offset	0x84A0 0x84A1	W	1DDD.DDDD *DDDD.DDDD*	bit [15] = 1 bit [14:0] = Patch memory offset

The patch space starts from address 0x8600.

Patch structure:
“disable all patches”
“set address to patch”
“set offset of patch in memory”
“write patch in memory (starting from address 0x8600 + patch memory offset)”
“enable all patches”

The state in which to download the patch depends on the nature of the patch, most likely either idle or sleep mode. Please contact ST support for patch delivery and recommendations for ideal use.

4.10 Additional features

There are a number of additional features which are supported by the STV0974, however implementation of these features is not supported by this datasheet. Please contact the ST support team for support of these features if you have a specific requirement.

- The polarity of the HSYNC and VSYNC signal can be programmed. However, these are non-standard settings.
- The transmitted byte order of the RGB and YUV is programmable.
- The viewfinder color matrix can be programmed to match the characteristics of a local LCD display.

5 Electrical characteristics

5.1 Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD} (including VCORE & VDDPOR)	Supply voltage	-0.5 to +2.2	V
	Voltage on any signal pin	-0.5 to (V_{DD} + 0.5)	V
I_{DD}	Supply current	100	mA
	Current on any signal pin	±10	mA
T_{STO}	Storage temperature	-40 to 150	°C
$T_{LEAD, 974E}$	Lead temperature (soldering, 10 s) for lead-free package	+260	°C
$T_{LEAD, 974}$	Lead temperature (soldering, 10 s) for leaded package	+225	°C

Caution: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	+1.7 to +1.9	V
T_A	Ambient temperature	-25 to +70	°C

5.3 Thermal data

Symbol	Parameter	Value	Unit
Rth(j-a)	Junction-ambient thermal resistance - TFBGA56[a]	65	°C/W

a. Typical, measured with the component mounted on an evaluation PC board in free air.

5.4 DC electrical characteristics

Over operating conditions unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Max	Unit
V_{IL}	Input low voltage		-0.3	0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}	V_{DD} + 0.3	V
V_{OL}	Output low voltage	I_{OL} < 2 mA		0.2 V_{DD}	V
V_{OH}	Output high voltage	-I_{OH} < 2 mA	0.8 V_{DD}		V
I_{IL}	Input leakage current Input pins I/O pins	V_{SS} < V_{IN} < V_{DD}		 ±10 ±1	 µA µA
C_{IN}	Input capacitance SCL, MSCL	T_A = 25 °C, freq. = 1 MHz		 6	 pF
$C_{I/O}$	Input / Output capacitance SDA, MSDA	T_A = 25 °C, freq. = 1 MHz		 8	 pF

Table 37: Power supply specifications[a]

Symbol	Parameter	Test Conditions	Typ.	Max	Unit
I_{DDPD}	V_{DD} supply current in power-down mode	V_{DD} = max ; PDN < V_{IL}	5	20	µA
I_{DDIDLE}	V_{DD} supply current in idle mode	V_{DD} = max ; mode = idle.	15	25	mA
$I_{DDACTIVE\_JPEG}$	V_{DD} supply current in active live mode	V_{DD} = max ; mode = live or ViewFinder or capture JPEG at VGA 30 frame/s.	65	75	mA
$I_{DDACTIVE\ NON\_JPEG}$	V_{DD} supply current in active live mode	V_{DD} = max ; mode = live or ViewFinder or capture YUV at VGA 30 frame/s.	55	75	mA

a. Same power consumption for Viewfinder, live and capture modes if same output image size and output data format.

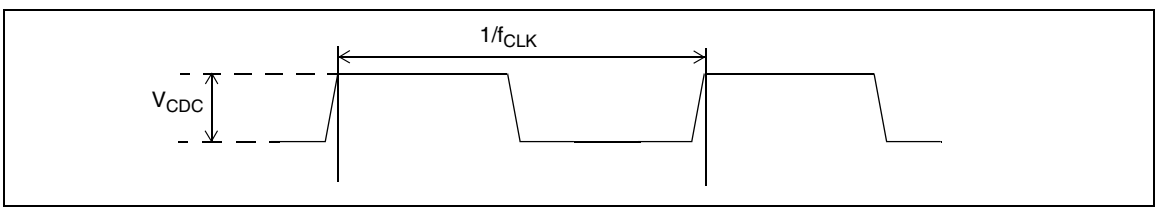
5.5 AC electrical characteristics

5.5.1 CLK

Table 38: CLK electrical characteristics (*Figure 30*)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CDC}	DC coupled square wave voltage	1.7	1.8	1.9	Vp-p
f_{CLK}	Clock frequency input	6.5	13	26	MHz

Figure 30: CLK electrical characteristics



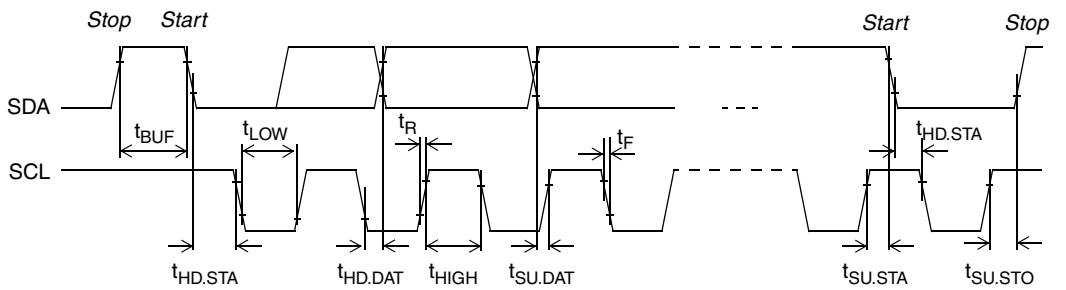
5.5.2 I^2C slave timing

Table 39: I^2C slave timing (*Figure 31*)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency			400	kHz
t_{LOW}	Clock pulse width low	1.3			µs
t_{HIGH}	Clock pulse width high	0.6			µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter			50	ns
t_{BUF}	Bus free time between transmissions	1.3			µs
$t_{HD.STA}$	Start hold time	0.6			µs
$t_{SU.STA}$	Start set-up time	0.6			µs
$t_{HD.DAT}$	Data in hold time	0.15		0.9	µs
$t_{SU.DAT}$	Data in set-up time	100			ns
t_R	SCL / SDA rise time[a]			300	ns
t_F	SCL / SDA fall time[a]			300	ns
$t_{SU.STO}$	Stop set-up time	0.6			µs
t_{DH}	Data out hold-time	0	0.6	0.9	µs

a. Measured from 0.1 to 0.9 or 0.9 to 0.1 VDD and with 4.7 k pull-up resistor and 100pF maximum capacitance on both SDA and SCL.

Figure 31: I²C slave timing



Note: t_{DH} is the same timing as $t_{HD.DAT}$. t_{DH} is a value driven by the STV0974. $t_{HD.DAT}$ is the value when the host is driving.

5.5.3 I²C master timing

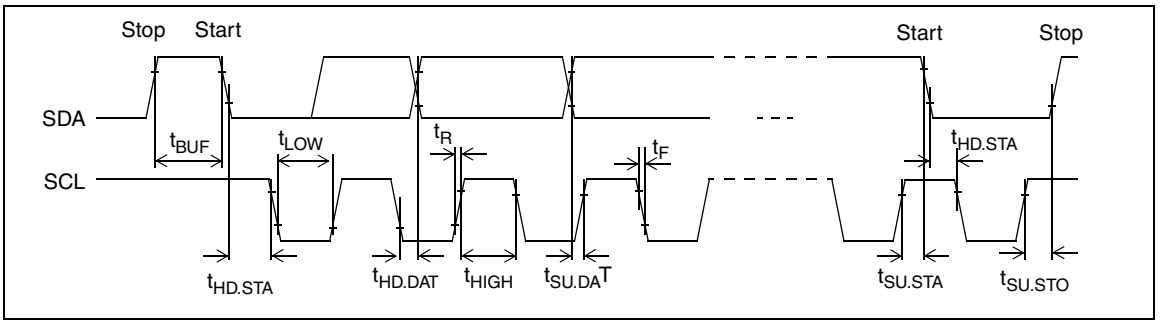
Table 40: I²C master timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	MSCL clock frequency [a]		200	400	kHz
t_{LOW}	Clock pulse width low	1.1			µs
t_{HIGH}	Clock pulse width high	0.6			µs
t_{BUF}	Bus free time between transmissions	1.3			µs
$t_{HD.STA}$	Start hold time	0.6			µs
$t_{SU.STA}$	Start set-up time	0.6			µs
$t_{HD.DAT}$	Data in hold time	0.15		0.9	µs
$t_{SU.DAT}$	Data in set-up time	100			ns
t_R	MSCL / MSDA rise time [b]			300	ns
t_F	MSCL / MSDA fall time [b]			300	ns
$t_{SU.STO}$	Stop set-up time	0.6			µs
t_{DH}	Data out hold-time	0	0.6	0.9	µs

a. 200 kHz recommended through system patch. Please contact ST for details.

b. Measured from 0.1 to 0.9 or 0.9 to 0.1 VDD and with 4.7 k pull-up resistor and 100pF maximum capacitance on both MSDA and MSCL.

Figure 32: I²C master timing



i. t_{DH} is the same timing as $t_{HD.DAT}$. t_{DH} is a value driven by the STV0974. $t_{HD.DAT}$ is the value when the host is driving.

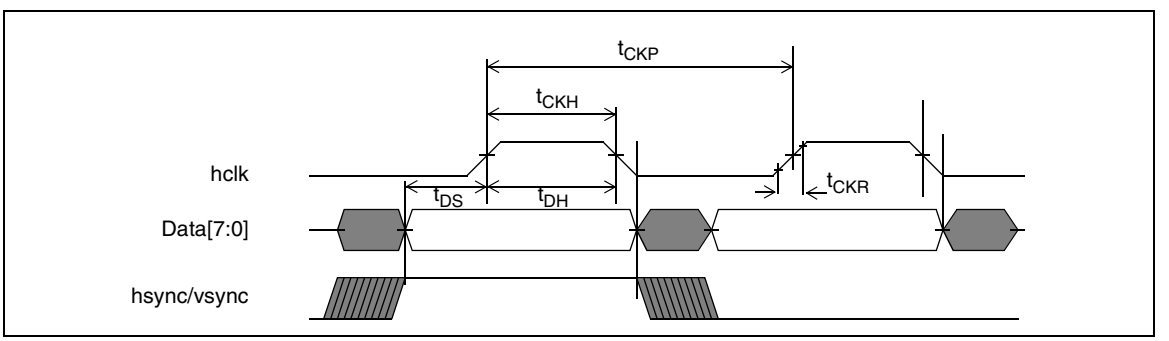
5.5.4 Video output timing

Table 41: Video output timing (*Figure 33*)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{DS}	Data and synchro setup time[a]	10			ns
t_{DH}	Data and synchro hold time [a]	10			ns
t_{CKH}	Clock pulse width high [a]	16			ns
t_{CKP}	Clock period [a]			44	ns
t_{CKR}	Clock rise time[a]			5	ns

a. with a 12 pF capacitance

Figure 33: Video output timing



5.5.5 Microprocessor read/write timing

Table 42: Microprocessor read and write cycle timingv

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{AS}	RS, CSN valid to RDN or WRN low	7			ns
t_{AH}	RS, CSN hold after RDN or WRN high	7			ns
t_{RACC}	Read access time			40	ns
t_{LZ}	RDN high to data high impedance			15	ns
t_{RP}	Read pulse width	40			ns
t_{WP}	Write pulse width	45			ns
t_{WDS}	Data setup to WRN high	35			ns
t_{RREC}	Read recovery time	30			ns
t_{WREC}	Write recovery time	22			ns
t_{ZL}	RDN low to data low impedance	0			ns
t_{RDH}	RDN low to data invalid	0			ns
t_{WDH}	Data hold after WRN high	5			ns

Figure 34: Read cycle timing

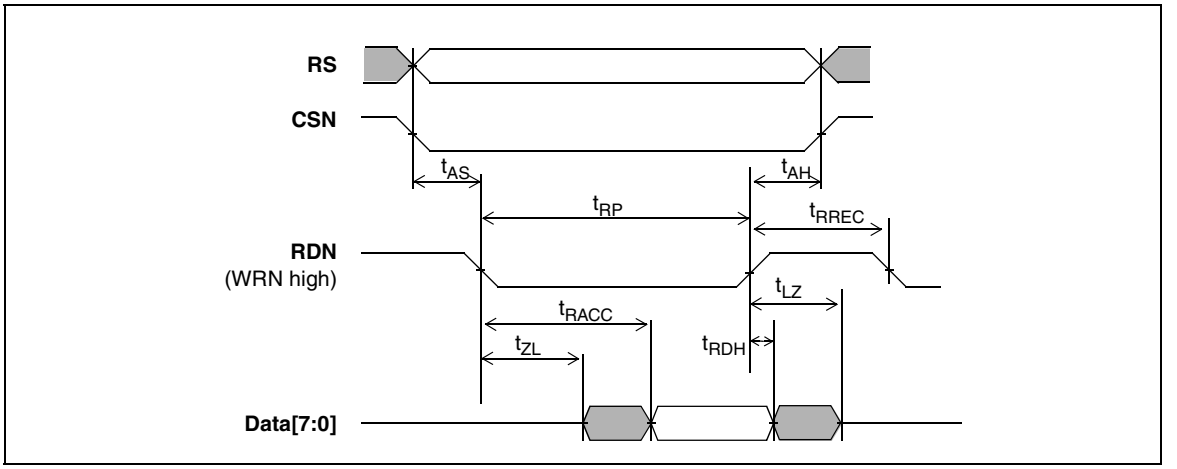
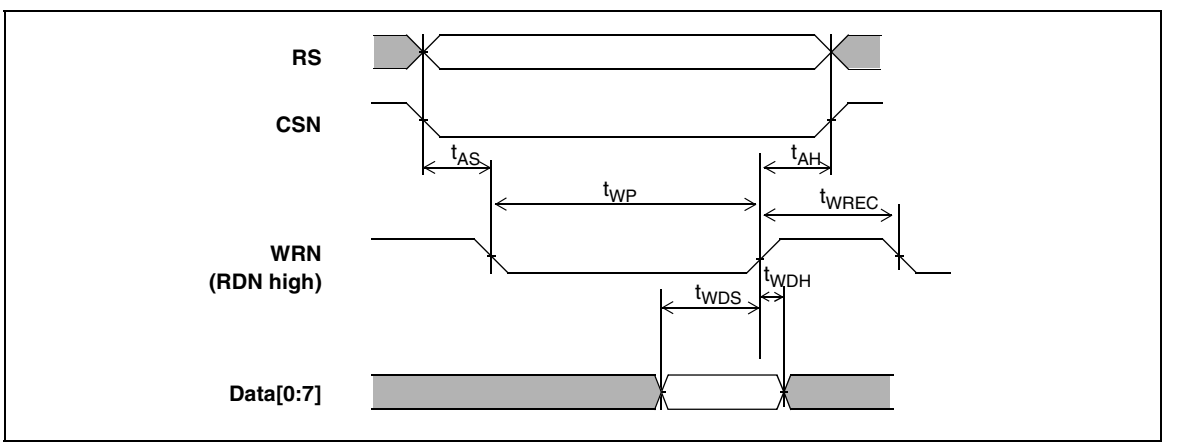


Figure 35: Write cycle timing



5.5.6 VisionLink serial receiver timing

Table 43: VisionLink serial receiver input timing (*Figure 36*)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{DS}	Data setup time	1			ns
t_{DH}	Data hold time	2.7			ns
t_{CKP}	Clock period	8.3			ns

Figure 36: VisionLink basic input timing

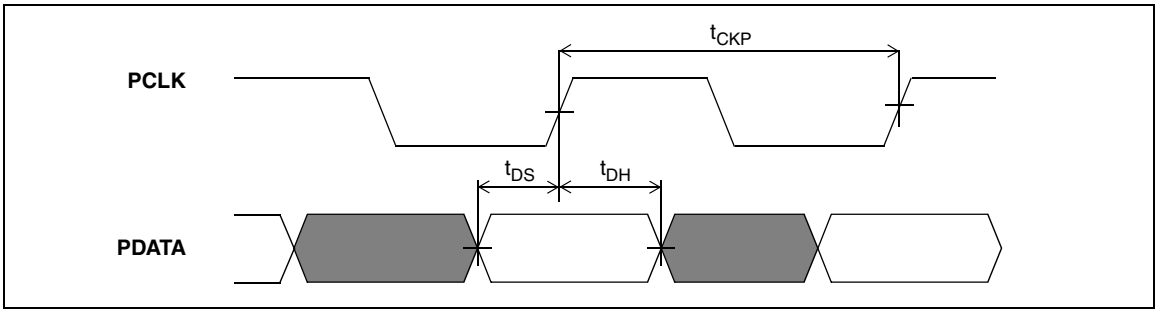


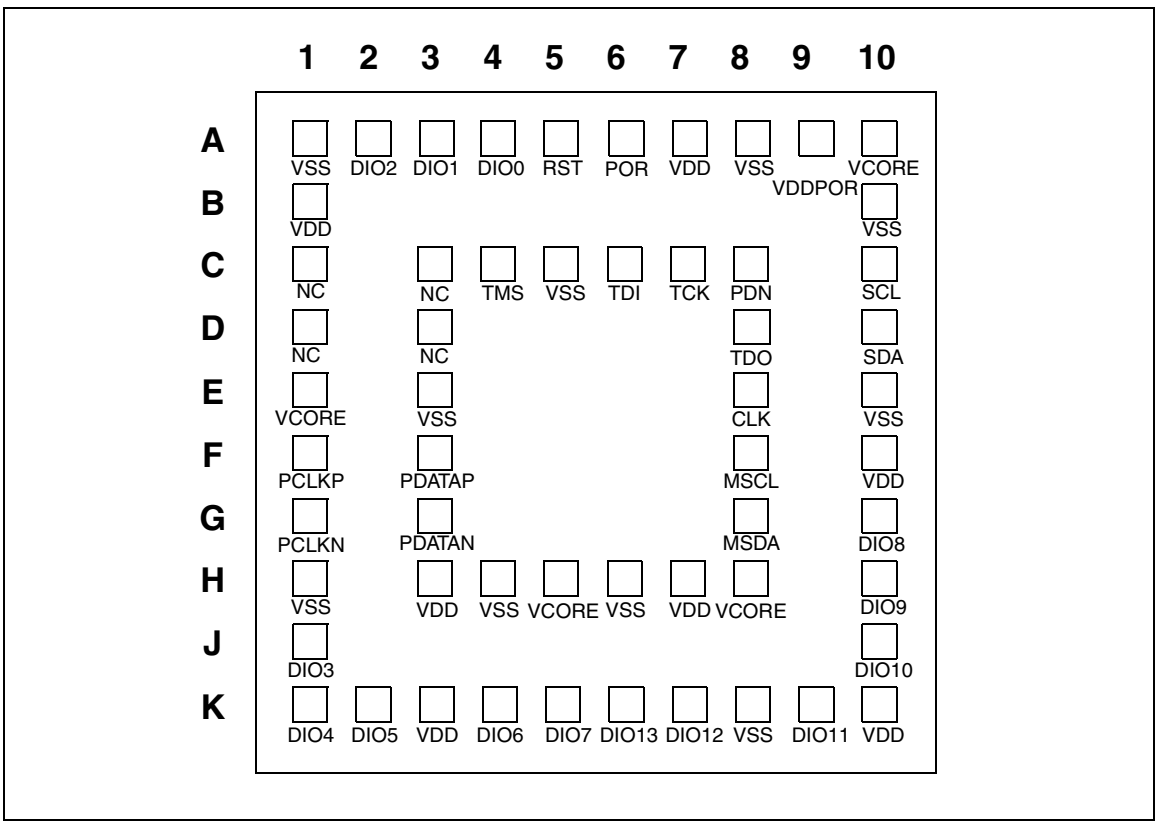
Table 44: Receiver VisionLink / SubLVDS electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_I	Input common mode voltage range	V_{DD} /2 - 0.4	V_{DD}/2	V_{DD}/2 + 0.4	V
V_{IDTH}	Input differential threshold (Va -Vaz)	+/-50		+/-200	mV
$t_{PWRUP/PWRDN}$	Power-up/-down time		2	10	µs

6 Package mechanical data

6.1 Pin assignment

Figure 37: STV0974 pin assignment



6.2 Package dimensions

Table 45: TFBGA 6x6x1.20 56 2R10 0.50 - Package dimensions [a] [b] [c]

Reference	Min.	Typ.	Max.	Unit
A	1.010		1.200	mm
A1	0.150			mm
A2		0.820		mm
b	0.250	0.300	0.350	mm
D	5.850	6.000	6.150	mm
D1		4.500		mm
E	5.850	6.000	6.150	mm
E1		4.500		mm
e		0.500		mm
F	0.600	0.750	0.900	mm
ddd			0.080	mm
.eee [d]			0.15	mm
.fff [e]			0.05	mm

a. Max mounted height is 1.20mm. Based on a 0.27mm ball pad diameter.
Solder paste is 0.15mm thickness and 0.27mm diameter.

b. TFBGA stands for Thin Profile Fine Pitch Ball Grid Array.
Thin profile:
-The total profile height (Dim A) is measured from the seating plane to the top component
- A = (1.01 to 1.20) mm
- Fine pitch: e>1.00mm pitch

c. The terminal A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, indentation or other feature of package body or integral heatslug.
- A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner.

d. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

e. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

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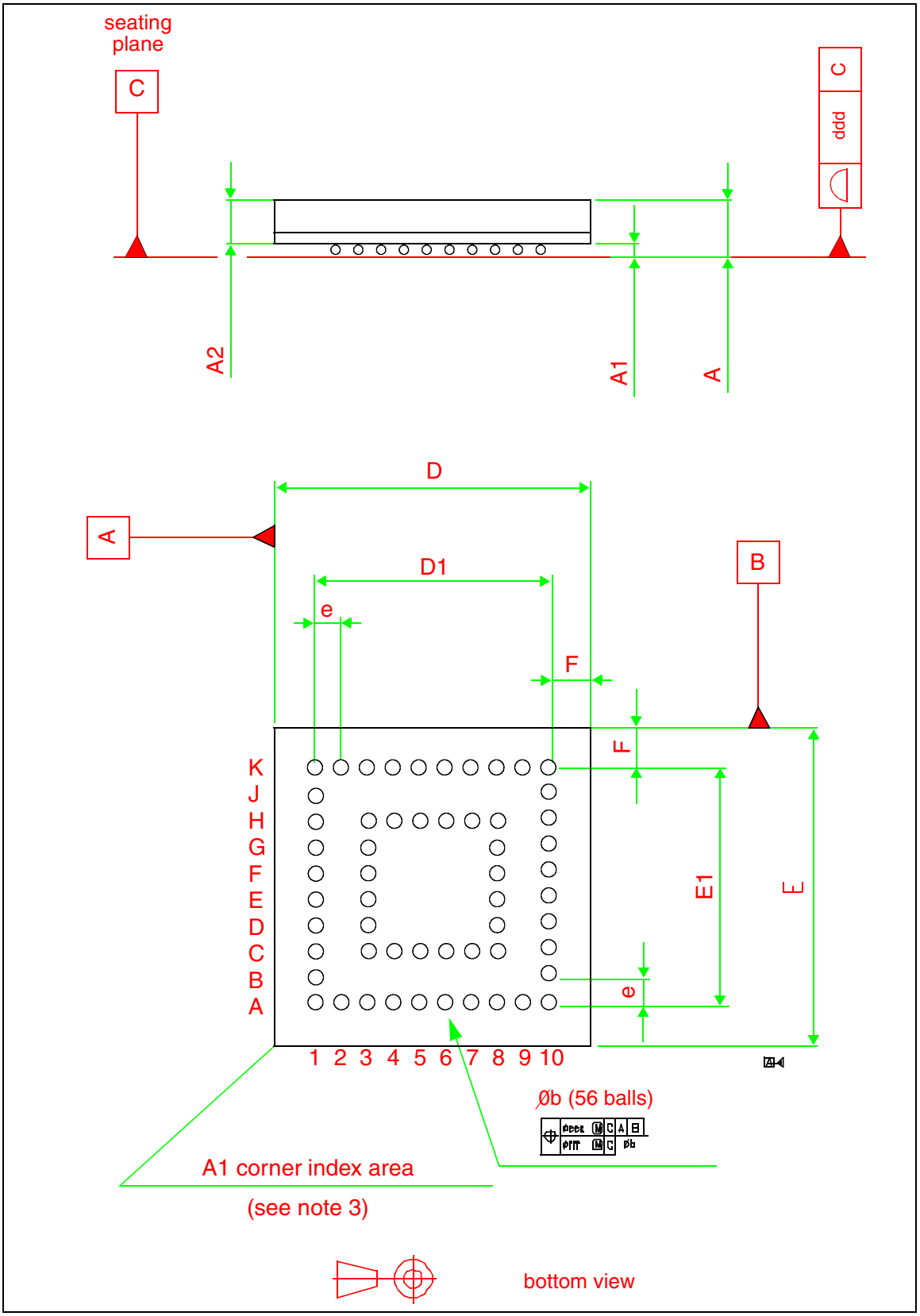
Figure 38: TFBGA 56 6x6x1.2 2R10 0.5



7 PCB layout guide lines for the STV0974 and VS6552

Normal good PCB design practice should be observed for the layout of the STV0974.

Power and ground planes should be used to supply power to STV0974.

The high speed subLVDS signal pairs (PCLKP,PCLKN) and (PDATAP,PDATAN) should be routed as balanced transmissions lines with a characteristic balanced impedance of between 80 to 120 Ω The two traces in the signal pair should be routed together and should be matched in length to within +/-3mm. The pairs of balanced line traces should be matched in length to within +/- 10mm. To save components, 100 Ω termination resistors are embedded in the high speed subLVDS signal pairs (PCLKP/PCLKN) and (PDATAP/PDATAN) of the STV0974.

All passive components for the STV0974 should be placed in close proximity to the device, including the decoupling capacitors. The decoupling capacitors for the VS6552 should be placed close to the sensor.

8 Application schematics

Figure 39: Mobile camera application, 8-bit parallel video interface, $V_{I/O}$ = 2.8V with low level shifter

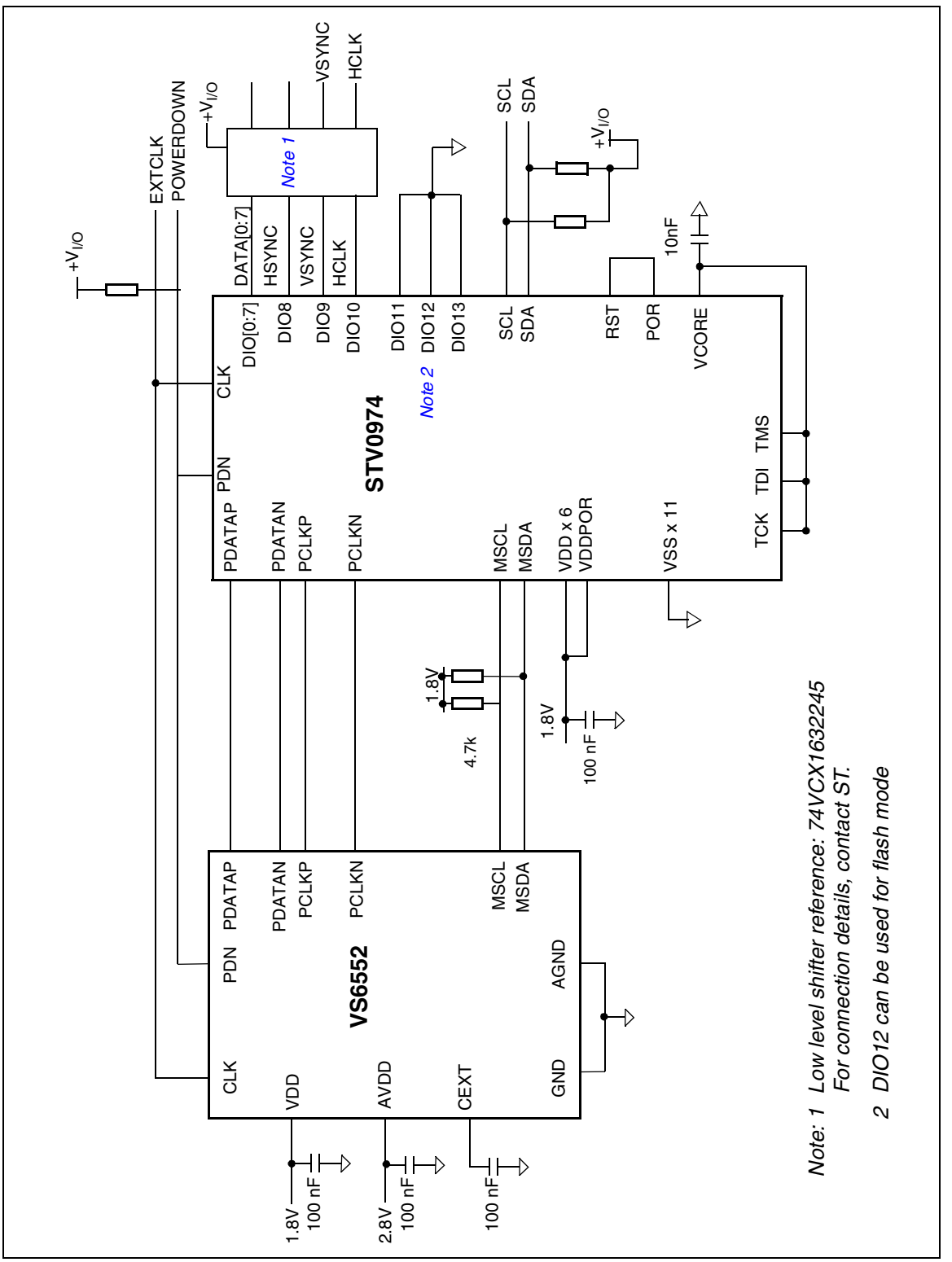
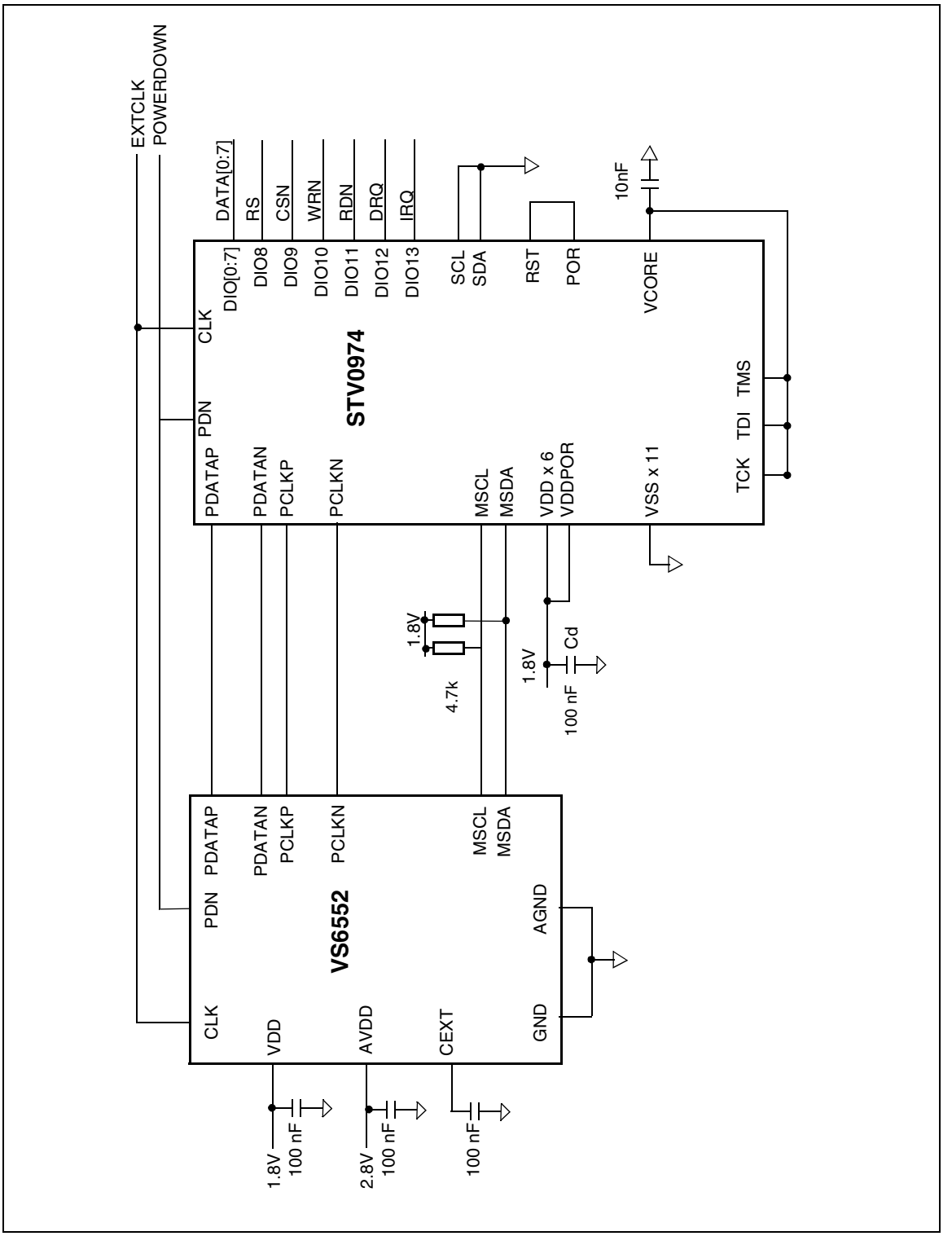


Figure 40: Mobile camera application, microprocessor interface, $V_{I/O}$ = 1.8V, no low level shifter



9 Evaluation kit and demonstration boards

A number of support kits are available. The evaluation kit is recommended for evaluation and system integration as it is an open system and electrical connections can be made from the EVK to the host system. The demonstration boards are small kits that do not allow hard connections to the customers system.

Table 46: Ordering details

Part Number	Description
STV-974-/552S-E01	Evaluation kit including base board, STV0974 plug in, flex attached VS6552 plug-in and socketed VS6552 plug-in
STV-974/552S-R01	Demonstration board with flex attached VS6552
STV-974/552S-R02	Demonstration board with socketed VS6552

Revision history

Revision	Date	Comments
0.1	December 2003	Product preview, draft 10 released in ADCS
0.2	January 2004	Update of application schematics to reflect the changes on some pin name for the VS6552. Update of some register default values.
1	April 2004	Description of video compression block in *Functional description*. Addition of Register Group 6 for flash mode (*I²C register map*.) Review of register default values in *I²C register map*. Review and update of device characteristics in *Electrical characteristics*
1	June 2004	Minor revision. Updated cross reference to Table 35
2	28 Oct 2004	Document status changed to datasheet to reflect the product maturity level. Changes applied: *Table 21: Timing constraints* : t5 value changed to 7 µs minimum (instead of 20µs) *Table 41: Video output timing (Figure 33)* - Note 1 change capacitance value to 12pF(instead of 30 pF) *Section 3: Signal description*: Added precisions about internal resistor for PDATAP/N and PCLKP/N *Electrical characteristics*: Modified I_{DDP} typical value 5 µA (instead of 10). *PCB layout guide lines for the STV0974 and VS6552*: Added one sentence about embedded termination resistors in the STV0974.
3	23 Nov 2004	Minor revision. Format update.

References

[1] ITU-R Rec.BT.656-4. Interfaces for digital component video signals in 525-line and 625-line television system operating at the 4:2:2 level of recommendation ITU-R BT.601 (Part A), 1986-1992-1994-1995-1998

[2] ITU-T Rec. T.81 (1992E) - ISO/IEC 10918-1:1993(E), Information Technology- Digital compression and Coding of Continuous-tone Still Images - Requirements and Guidelines

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