

CMOS 8-Channel Data Selector

High-Voltage Types (20-Volt Rating)

■ CD4512B is an 8-channel data selector featuring a three-state output that can interface directly with, and drive, data lines of bus-oriented systems.

The CD4512B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:

- 3-state output
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Digital multiplexing
- Number-sequence generation
- Signal gating

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

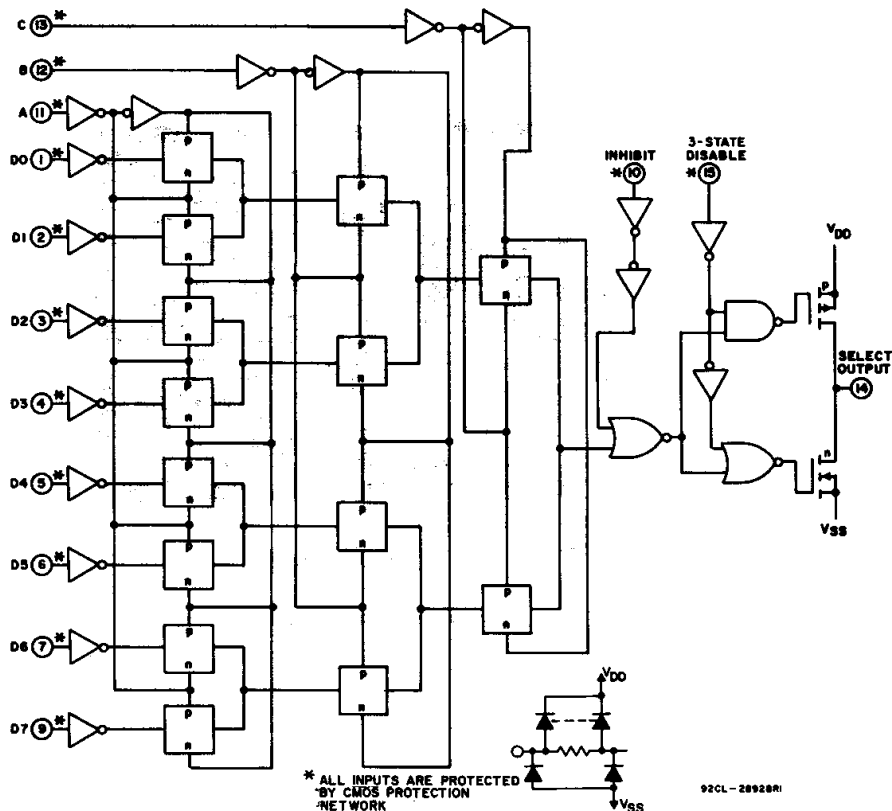
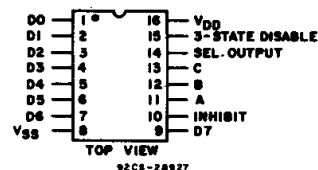
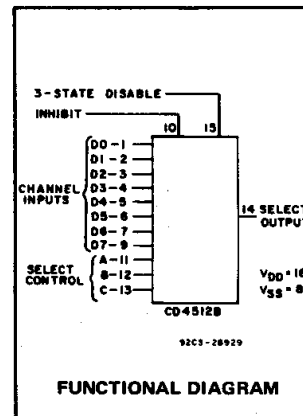


Fig. 1 - Logic diagram.

CD4512B Types



TERMINAL ASSIGNMENT

TRUTH TABLE

SEL. CONT.			INH	3-STATE DISABLE	SEL OUTPUT
A	B	C			
0	0	0	0	0	D0
1	0	0	0	0	D1
0	1	0	0	0	D2
1	1	0	0	0	D3
0	0	1	0	0	D4
1	0	1	0	0	D5
0	1	1	0	0	D6
1	1	1	0	0	D7
X	X	X	1	0	0
X	X	X	X	1	High Z

1 = High Level 0 = Low Level
X = Don't Care

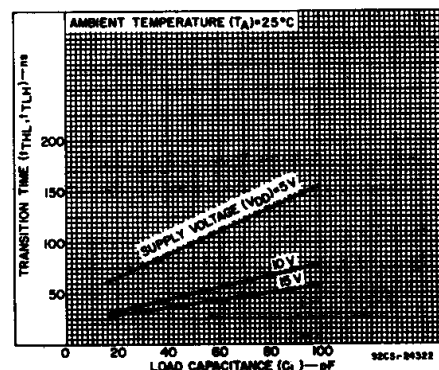


Fig. 2 - Typical transition time as a function of load capacitance.

CD4512B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5V$

DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79\text{mm}$) from case for 10s max $+265^\circ\text{C}$

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage V _{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA
3-State Output Leakage Current I _{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	±10 ⁻⁴	±0.4	μA

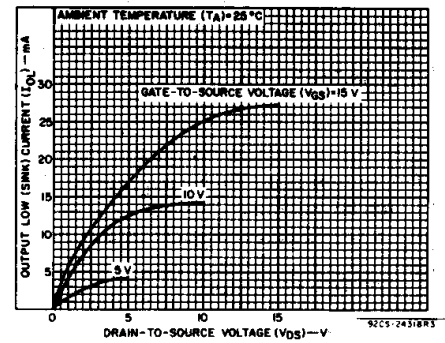


Fig. 3 - Typical output low (sink) current characteristics.

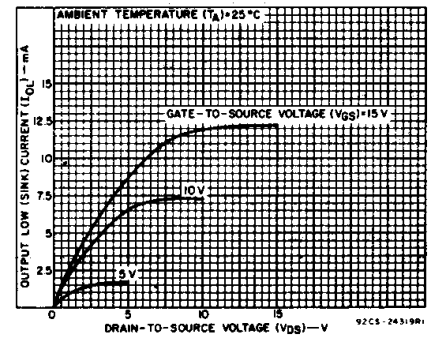


Fig. 4 - Minimum output low (sink) current characteristics.

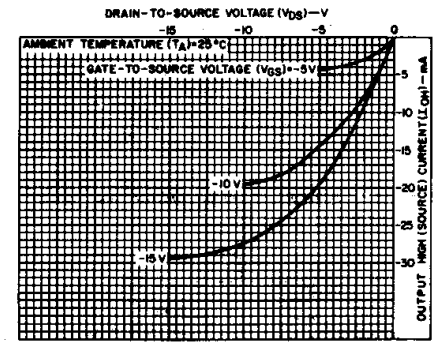


Fig. 5 - Typical output high (source) current characteristics.

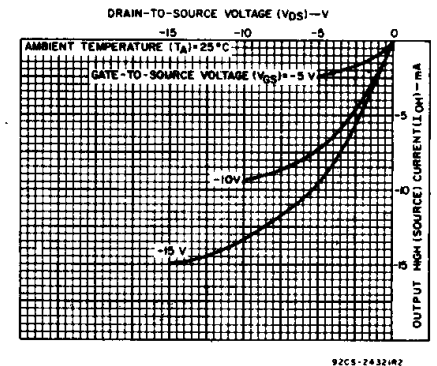


Fig. 6 - Minimum output high (source) current characteristics.

CD4512B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS		UNITS
		Typ.	Max.	
Propagation Delay Time, t_{PHL} , t_{PLH} Inhibit to Output	5	140	280	ns
	10	70	140	
	15	50	100	
"A" Select to Output	5	200	400	ns
	10	85	170	
	15	60	120	
Data to Output	5	180	360	ns
	10	75	150	
	15	55	110	
3-State Disable Delay Time: t_{PZL} , t_{PLZ} , t_{PHZ} , t_{PZH}	5	60	120	ns
	10	30	60	
	15	20	40	
Transition Time, t_{THL} , t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN} (Any Input)		5	7.5	pF

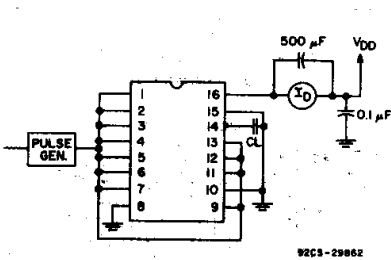


Fig. 9 - Dynamic power dissipation test circuit.

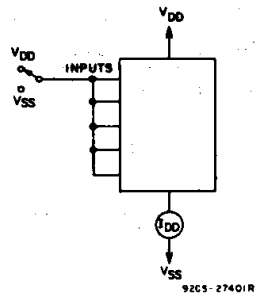


Fig. 10 - Quiescent device current test circuit.

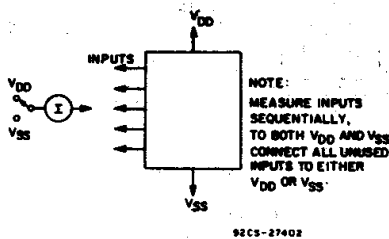


Fig. 11 - Input current test circuit.

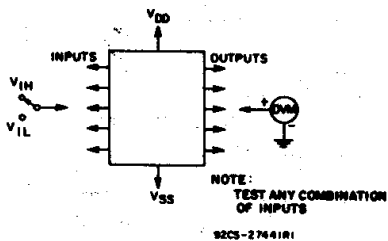


Fig. 12 - Input voltage test circuit.

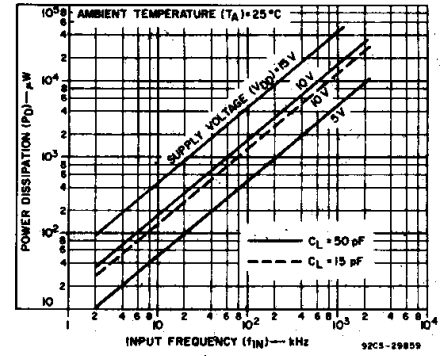


Fig. 7 - Typical dynamic power dissipation as a function of frequency.

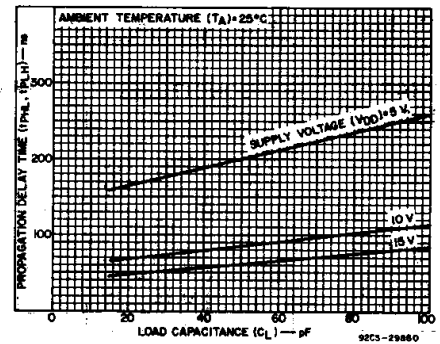
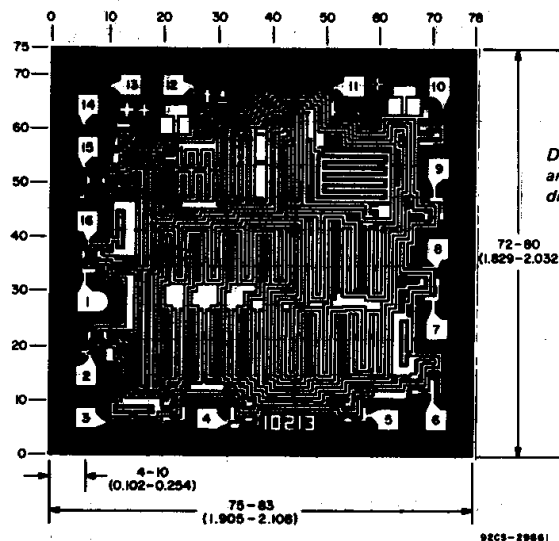


Fig. 8 - Typical propagation delay time as a function of load capacitance ("A" select to output).



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

Dimensions and pad layout for CD4512BH

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