

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

General Description

The MAX2390–MAX2393/MAX2396/MAX2400/MAX2401 (referred to as the “MAX2390 family”) fully integrated direct-conversion receiver ICs are designed for W-CDMA and TD-SCDMA applications.

The MAX2390 family of receiver ICs have over 90dB of dynamic gain control, and typical noise figure of 2.7dB referred to LNA input. Each receiver consists of an ultra-low-current low-noise amplifier (LNA) with on-chip output matching and a two-step gain control. The zero-IF demodulator has a differential circuit topology for minimum LO leakage to receiver's input. The channel selectivity is done completely in the baseband section of the receiver with an on-chip lowpass filter. The AGC section has over 50dB of gain-control range. LO quadrature generation is done on-chip through a divide-by-2 prescaler. The DC offset cancellation in the I/Q baseband channels is done fully on-chip using a DC servo loop. To quickly correct for large DC offset transients in minimal time, very fast settling time is obtained by optimization of the DC-offset-cancellation circuit's time constant.

The MAX2390 family includes a 3-wire serial bus for configuring the different receiver modes. They also include a SHDN pin for full device shutdown. The receivers are fabricated using an advanced high-frequency SiGe BiCMOS process. The ICs operate from a single +2.7V to +3.3V supply and are housed in a small 28-pin leadless QFN-EP and thin QFN-EP packages (5mm x 5mm).

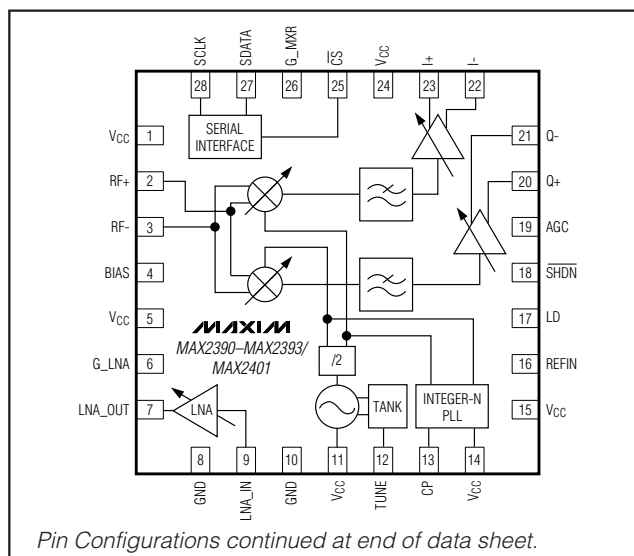
Applications

IMT2000 Handsets	TD-SCDMA Handsets
UMTS Handsets	W-CDMA TDD Handsets
W-CDMA Band II (PCS) Handsets	W-CDMA Band III (DCS) Handsets

Features

- ◆ Fully Monolithic Direct-Conversion Receivers
- ◆ Eliminate External IF SAW + IF AGC + I/Q Demod
- ◆ Meet all 3GPP Receiver's Standard Requirements with at Least 3dB Margin on Eb/No
- ◆ Operate from a +2.7V to +3.3V Single Supply
- ◆ Over 90dB of RF+ Baseband Gain-Control Range
- ◆ Channel Selectivity Over 40dB
- ◆ Receiver Current Consumption $\approx$ 32mA
- ◆ On-Chip DC Offset Cancellation
- ◆ Compatible with Various CMOS Logic Levels

Pin Configurations/ Functional Diagrams



Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	APPLICATION	CHIP RATE (Mcps)	RF BAND (MHz)	SYNTHESIZER
MAX2390ETI	-40°C to +85°C	28 Thin QFN-EP*	W-CDMA Band II	3.84	1930 to 1990	On-Chip
MAX2391ETI	-40°C to +85°C	28 Thin QFN-EP*	IMT2000/UMTS	3.84	2110 to 2170	On-Chip
MAX2391ETI+	-40°C to +85°C	28 Thin QFN-EP*	IMT2000/UMTS	3.84	2110 to 2170	On-Chip
MAX2392ETI	-40°C to +85°C	28 Thin QFN-EP*	TD-SCDMA	1.28	2010 to 2025	On-Chip
MAX2392ETI+	-40°C to +85°C	28 Thin QFN-EP*	TD-SCDMA	1.28	2010 to 2025	On-Chip
MAX2393EGI	-40°C to +85°C	28 QFN-EP*	W-TDD/TD-SCDMA	3.84 or 1.28	1900 to 1920	On-Chip
MAX2396EGI	-40°C to +85°C	28 QFN-EP*	IMT2000/UMTS	3.84	2110 to 2170	External
MAX2400ETI	-40°C to +85°C	28 Thin QFN-EP*	W-CDMA Band II	3.84	1930 to 1990	External
MAX2401ETI	-40°C to +85°C	28 Thin QFN-EP*	W-CDMA Band III	3.84	1805 to 1880	On-Chip
MAX2401ETI+	-40°C to +85°C	28 Thin QFN-EP*	W-CDMA Band III	2.84	1805 to 1880	On-Chip

*EP = Exposed paddle. + Denotes lead-free package.

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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +3.6V
 All Other Pins to GND-0.3V to (V_{CC} + 0.3V)
 LNA_IN+15dBm
 Digital Input Current±10mA
 Digital Output Open-Collector Current 1mA
 Continuous Power Dissipation (T_A = +70°C)
 28-Pin QFN (derate 20.8mW/°C above +70°C) 1666.7mW

Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +160°C
 Lead Temperature (soldering, 10s)+300°C



CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 3.3V, V_{SHDN} = V_{DH} (Note 1), G_{LNA} = G_{MXR} = V_{IH}, HGML mode (see Table 6), no RF input signals, RF input and output ports are terminated into 50Ω, baseband I and Q outputs loaded with 10kΩ || 5pF, V_{AGC} = 2.2V, T_A = -40°C to +85°C. Typical values are for V_{CC} = 2.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V _{CC}			2.7	2.8	3.3	V
Operating Supply Current	I _{CC}	MAX2391, MAX2392, MAX2393, MAX2400	HGML mode		33	39	mA
			HGHL mode		34	40	
			LG mode		29	35	
			IDLE mode		11.5	13	
		MAX2396	HGML mode		31	38	
			LG mode		27	34	
			IDLE mode		10.5	12	
		MAX2390, MAX2401	HGML mode		35	42	
			HGHL mode		36	43	
			LG mode		31	37	
			IDLE mode		12	14	
		All versions	SHDN mode		0.5	15	μA
Gain-Control Input Bias Current	I _{AGC}	0.3V ≤ V _{AGC} ≤ 2.4V		-10		+10	μA
		V _{AGC} ≤ 0.3V; V _{SHDN} = V _{DL}				3	
Common-Mode Output Voltage at I and Q Outputs	V _{CM}	V _{I(CM)} = (V _{I+} + V _{I-}) / 2, V _{Q(CM)} = (V _{Q+} + V _{Q-}) / 2	(V _{CM} = 0 in OPCTRL register)	1.10	1.20	1.30	V
			(V _{CM} = 1 in OPCTRL register)	1.30	1.42	1.55	
Lock Indicator High Leakage Current		PLL locked, V _{LD} = V _{CC} (MAX2390-MAX2393, MAX2401)				0.1	μA
Lock Indicator Low Sink Voltage		Sinking 100μA, PLL unlocked (MAX2390-MAX2393, MAX2401)				0.4	V
SHDN Input-Logic High	V _{DH}	MAX2390-MAX2393, MAX2401		1.5		V _{CC}	V
		MAX2396/MAX2400		V _{CC} - 0.5		V _{CC}	
SHDN Input-Logic Low	V _{DL}			0		0.5	V
SHDN Input Resistance		Resistance to GND		50			kΩ

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 2.7V$ to $3.3V$, $V_{SHDN} = V_{DH}$ (Note 1), $G_{LNA} = G_{MXR} = V_{IH}$, HGML mode (see Table 6), no RF input signals, RF input and output ports are terminated into 50Ω , baseband I and Q outputs loaded with $10k\Omega$ || $5pF$, $V_{AGC} = 2.2V$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are for $V_{CC} = 2.8V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IDLE Input-Logic High	V_{IH}	MAX2396, MAX2400 only	$V_{CC} - 0.5$		V_{CC}	V
IDLE Input-Logic Low	V_{IL}		0		0.5	V
IDLE Input Resistance			Resistance to GND	50		$k\Omega$
Digital Input-Logic High	V_{IH}	$\overline{CS}$, $SDATA$, $SCLK$, G_{MXR} , G_{LNA} (Note 1)	0.7 $\times$ V_{DH} or 1.2V, whichever is greater		V_{CC}	V
Digital Input-Logic Low	V_{IL}		0	0.3 $\times$ V_{DH}		
Input-Logic High Current	I_{IH}				1	μA
Input-Logic Low Current	I_{IL}		-1			μA

AC ELECTRICAL CHARACTERISTICS

(Devices tested on their respective evaluation kits (EV kits); LNA input port is driven with a 50Ω source; LNA output port is terminated with 50Ω load, mixer differential input port is driven through a 1:4 impedance balun with a 50Ω source; baseband I/Q output differential load = $10k\Omega$ || $5pF$; reference oscillator input: 19.2MHz (MAX2390/MAX2391/MAX2392/MAX2393), 26MHz (MAX2401), 15.36MHz (MAX2396/MAX2400); AGC is set to result in a 0.3V_{p-p} differential output-voltage swing at the baseband I/Q output; registers set to power-up defaults (Table 2); $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are for $V_{CC} = 2.8V$ and $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LNA PERFORMANCE						
RF Frequency Range (Note 2)	f_{RF}	MAX2391/MAX2396	2110	2140	2170	MHz
		MAX2392	2010	2017	2025	
		MAX2393	1900	1910	1920	
		MAX2390/MAX2400	1930	1960	1990	
		MAX2401	1805	1842	1880	
Signal Phase Change	$\Delta\phi$	Switching between any of the LNA modes		8		Degrees
LNA HIGH GAIN ("HGLNA", $G_{LNA} = V_{IH}$)						
Power Gain	G_{LNA}	(Note 3)	13	16	18	dB
Noise Figure	NF_{LNA}	(Note 3)		1.5	2.0	dB
Input -1dB Compression Point	IP_{-1dB}	(Note 3)	-20	-16		dBm
3rd-Order Input Intercept Point (Note 4)	$IIP3_{LNA}$	MAX2391/MAX2396	-4.5	-2.5		dBm
		MAX2392/MAX2393	-6	-4		
		MAX2390/MAX2400/MAX2401	-7	-4		
Input Return Loss	dB[S11]	On EV kit, externally matched to 50Ω		-14		dB
Output Return Loss	dB[S22]	On EV kit, internally matched to 50Ω		-14		dB
Reverse Isolation	dB[S12]	On EV kit		-35		dB
LNA LOW GAIN ($G_{LNA} = V_{IL}$)						
Power Gain	G_{LNA}	(Note 3)	-12	-8.0	-5	dB
Noise Figure	NF_{LNA}	(Note 3)		18	22	dB
Input -1dB Compression Point	IP_{-1dB}	(Note 3)	-6	-3		dBm

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

AC ELECTRICAL CHARACTERISTICS (continued)

(Devices tested on their respective evaluation kits (EV kits); LNA input port is driven with a 50Ω source; LNA output port is terminated with 50Ω load, mixer differential input port is driven through a 1:4 impedance balun with a 50Ω source; baseband I/Q output differential load = 10kΩ || 5pF; reference oscillator input: 19.2MHz (MAX2390/MAX2391/MAX2392/MAX2393), 26MHz (MAX2401), 15.36MHz (MAX2396/MAX2400); AGC is set to result in a 0.3V_{P-P} differential output-voltage swing at the baseband I/Q output; registers set to power-up defaults (Table 2); T_A = -40°C to +85°C. Typical values are for V_{CC} = 2.8V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Return Loss	dB[S11]	On EV kit, externally matched to 50Ω			-11		dB
Output Return Loss	dB[S22]	On EV kit, internally matched to 50Ω			-11		dB
Reverse Isolation	dB[S12]	On EV kit			-30		dB
ZERO-IF DEMODULATOR PERFORMANCE (RF+/RF- TO BASEBAND I AND Q OUTPUTS)							
Voltage Gain (Note 5)	AV	HGML mode, VAGC = 2.2V		80	86		dB
		MG or LG mode, VAGC = 2.2V		68	76		
Baseband Gain-Control Range	ΔAV	VAGC = 0.3V to 2.4V (Note 3)		53	60		dB
Baseband Gain-Control Slope	dAV/dV	VAGC = 0.3V to 2.4V (Note 3)		25	29	33	dB/V
DSB Noise Figure (Notes 3, 6)	NF	HGML or HGHL mode, VAGC ≥ 1.8V	MAX2391/MAX2392/ MAX2393/MAX2396	10.5	14		dB
			MAX2390/MAX2400/ MAX2401	9.5	13		
		MG or LG mode, VAGC ≥ 1.8V			18.5	25	
3rd-Order Input Intercept Point	IIP3	HGML mode, VAGC = 2.2V (Note 7)		-5	-1		dBm
		HGHL mode, VAGC = 2.2V (Note 3, 7)		-3.5	0		
		MAX2390/MAX2400/MAX2401 HGML or HGHL mode (Note 8)			-16		
Input -1dB Compression Point	IP-1dB	LG mode, VAGC = 0.5V			-23		dBm
-1dB Output Compression Differential Voltage	OV-1dB	All modes (Note 3)	VAGC ≥ 1.3V	1.0	1.5		VP-P
			VAGC = 0.5V	0.6	1.0		
2nd-Order Input Intercept Point	IIP2	(MAX2391/MAX2396) 190MHz offset; all modes, VAGC ≥ 0.5V (Note 9)			+34		dBm
		(MAX2390/MAX2400) 80MHz offset, all modes, VAGC ≥ 0.5V (Note 9)			+33		
		(MAX2401) 95MHz offset, all modes, VAGC ≥ 0.5V (Note 9)			+33		
		VAGC = 2.2V, HGML mode (Note 10)	(MAX2390/MAX2391/ MAX2393/MAX2396/ MAX2400/MAX2401) 15MHz offset	+25	+33		
			(MAX2392) 4.8MHz offset	+25	+33		
LO Leakage	XLO	At LNA_IN, HGML mode, RX band (Note 3)			-100	-95	dBm
I/Q Gain Imbalance	IΔGI/QI	All modes, VAGC = 0.5V to 2.2V			0.2	1.5	dB

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AC ELECTRICAL CHARACTERISTICS (continued)

(Devices tested on their respective evaluation kits (EV kits); LNA input port is driven with a 50 Ω source; LNA output port is terminated with 50 Ω load, mixer differential input port is driven through a 1:4 impedance balun with a 50 Ω source; baseband I/Q output differential load = 10k Ω || 5pF; reference oscillator input: 19.2MHz (MAX2390/MAX2391/MAX2392/MAX2393), 26MHz (MAX2401), 15.36MHz (MAX2396/MAX2400); AGC is set to result in a 0.3V_{p-p} differential output-voltage swing at the baseband I/Q output; registers set to power-up defaults (Table 2); T_A = -40°C to +85°C. Typical values are for V_{CC} = 2.8V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/Q Quadrature Phase Imbalance	$ \Delta\Phi_{I/Q} $	All modes, V _{AGC} = 0.5V to 2.2V			4	Degrees
Error Vector Magnitude (Note 11)	EVM	MAX2391/MAX2392/MAX2393/MAX2396		15		%
		MAX2390/MAX2400/MAX2401		17		
Differential DC Offset at I/Q Baseband Output	ΔDC	Including DC servo loop; V _{AGC} = 2.2V			±25	mV
BASEBAND CHANNEL RESPONSE (W-CDMA); MAX2391/MAX2393/MAX2396						
-3dB Lowpass Corner Frequency	f _{-3dB}			2.4		MHz
Filter Attenuation Relative to 180kHz	A _{dB}	At 5MHz offset	51	58		dB
		At 10MHz offset	59	67		
		At 15MHz offset	64	75		
Passband Gain Flatness	ΔA_{dB}	100kHz to 1.92MHz (Note 3)		1.2	1.7	dB
BASEBAND CHANNEL RESPONSE (W-CDMA); MAX2390/MAX2400/MAX2401						
-3dB Lowpass Corner Frequency	f _{-3dB}	MAX2390/MAX2400		2.1		MHz
		MAX2401		2.2		
Filter Attenuation Relative to 180kHz	A _{dB}	At 2.7MHz offset, MAX2390/MAX2400	36	56		dB
		At 2.8MHz offset, MAX2401				
		At 3.5MHz offset, MAX2390/MAX2400	50	56		
		At 3.6MHz offset, MAX2401				
		At 5MHz offset	57	65		
		At 15MHz offset	65	75		
Passband Gain Flatness	ΔA_{dB}	100kHz to 1.92MHz (Note 3)		1.9	2.5	dB
BASEBAND CHANNEL RESPONSE (TD-SCDMA); MAX2392/MAX2393						
-3dB Lowpass Corner Frequency	f _{-3dB}			0.75		MHz
Filter Attenuation Relative to 180kHz	A _{dB}	At 1.6MHz offset	51	57		dB
		At 3.2MHz offset	56	65		
		At 6.4MHz offset	64	76		
Passband Gain Flatness	ΔA_{dB}	50kHz to 0.64MHz (Note 3)		1.2	1.7	dB

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AC ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ON-CHIP VCO							
VCO Frequency (VCO Range is 2x the LO Range)	f _{OSC}	MAX2391/MAX2396		4220		4340	MHz
		MAX2392		4020		4050	
		MAX2393		3800		3840	
		MAX2390/MAX2400		3860		3980	
		MAX2401		3610		3760	
Phase Noise	Φ _N	At 10MHz offset; locked (Note 3)			-139	-133	dBc/Hz
Pulling		From IDLE mode to ON mode (Note 3)			0.5	1	MHz _{p-p}
Pushing		V _{CC} stepped 3.3V to 2.7V (Note 3)				13	MHz/V
VCO INTERFACE TO EXTERNAL SYNTHESIZER (MAX2396/MAX2400)							
VCO Tuning Gain	K _{VCO}	Referred to the VCO frequency (2x RFLO)	MAX2396	130		300	MHz/V
			MAX2400	100		270	
VCO Output Frequency		Output to synthesizer is f _{VCO} / 3 = 2f _{RFLO} / 3	MAX2396	1406.67	1426.67	1446.67	MHz
			MAX2400	1286.67	1306.67	1326.67	
VCO Output Differential Voltage		(Note 12)		180			mV _{p-p}
VCO Tuning Voltage Range	V _{TUNE}			0.4		2.3	V
INTEGER-N RF SYNTHESIZER (MAX2390–MAX2393, MAX2401)							
Main PLL Integer Division Ratio		15-bit register (64/65 dual-modulus prescaler), f _{COMP} = 200kHz		4032	10700	32767	
Reference Frequency Range	f _{REF}			10	19.2	40	MHz
REFDIV Reference-Divider Ratio		9-bit register		16	96	511	
Charge-Pump Output Current (Sink or Source)	I _{CP}	CONFIG:CP1 = 1, CONFIG:CP0 = 1, V _{CPOUT} = V _{CC} / 2		2.0	2.5	3.0	mA
Charge-Pump Leakage Current	I _{L_CP}					10	nA
SYSTEM TIMING							
Turn-On Time Including DC Offset Cancellation	t _{ON}	From IDLE mode to ON mode VGA set to maximum gain with -40dBm signal at demodulator input (Note 3)			30	60	μs
3-WIRE SERIAL INTERFACE TIMING							
Data to Clock Setup	t _{CS}	Per timing diagram		20			ns
Data to Clock Hold Time	t _{CH}	Per timing diagram		10			ns
Clock Pulse-Width High	t _{CWH}	Per timing diagram		20			ns
Clock Pulse-Width Low	t _{CWL}	Per timing diagram		20			ns
Clock to Load Enable/Setup Time	t _{ES}	Per timing diagram		20			ns
Clock Frequency						20	MHz

Note 1: Logic thresholds track V_{SHDN}. This allows the digital interface to operate with logic levels from 1.2V to V_{CC}.

Note 2: All min and max specifications are measured over this frequency range.

Note 3: Guaranteed by design and characterization.

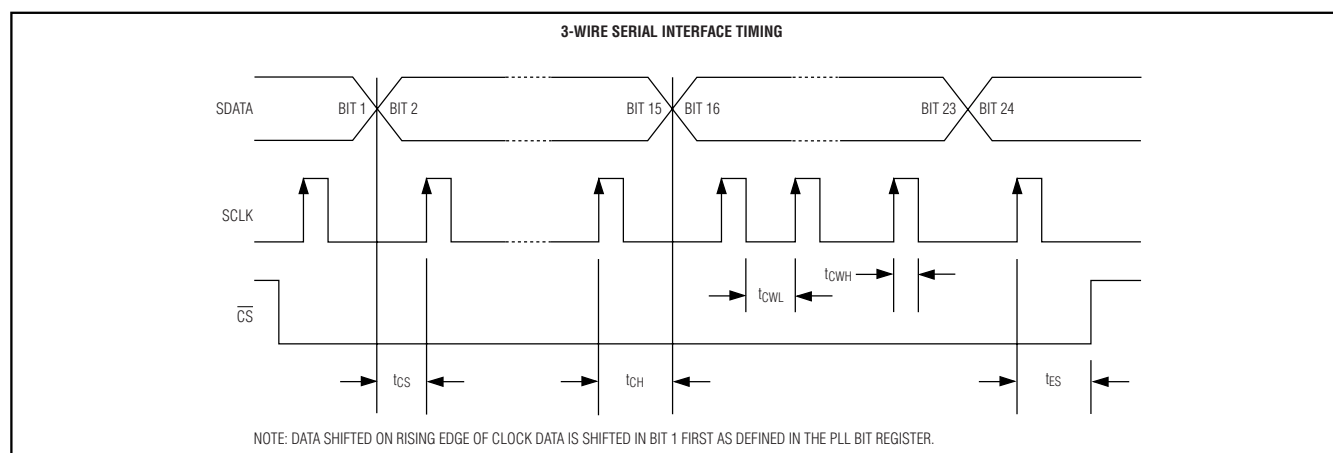
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AC ELECTRICAL CHARACTERISTICS (continued)

(Devices tested on their respective evaluation kits (EV kits); LNA input port is driven with a 50 Ω source; LNA output port is terminated with 50 Ω load, mixer differential input port is driven through a 1:4 impedance balun with a 50 Ω source; baseband I/Q output differential load = 10k Ω || 5pF; reference oscillator input: 19.2MHz (MAX2390/MAX2391/MAX2392/MAX2393), 26MHz (MAX2401), 15.36MHz (MAX2396/MAX2400); AGC is set to result in a 0.3V_{p-p} differential output-voltage swing at the baseband I/Q output; registers set to power-up defaults (Table 2); T_A = -40°C to +85°C. Typical values are for V_{CC} = 2.8V and T_A = +25°C, unless otherwise noted.)

- Note 4:** MAX2391/MAX2396: tones at 2025.0MHz and 1930.0MHz (-28dBm/toner); receiver tuned for input RF of 2120.0MHz.
MAX2392: tones at 2020.6MHz and 2023.8MHz (-35dBm/toner); receiver tuned for input RF of 2017.4MHz.
MAX2393: tones at 1910.0MHz and 1920.0MHz (-35dBm/toner); receiver tuned for input RF of 1900.0MHz.
MAX2390/MAX2400: tones at 1963.5MHz and 1965.9MHz (-35dBm/toner); receiver tuned for input RF of 1960.0MHz.
MAX2401: tones at 1846MHz and 1848.4MHz (-35dBm/toner); receiver tuned for input RF of 1842.4MHz.
- Note 5:** Voltage gain defined as the differential baseband RMS I or Q output voltage, measured across the 10k Ω load, divided by the RMS differential input voltage at RF+/RF-.
- Note 6:** NF is constant or flattens out for AGC voltage $\geq 1.75V$.
- Note 7:** MAX2391/MAX2396: tones at 2150.0MHz and 2160.18MHz (-35dBm/toner); receiver tuned for input RF of 2140MHz.
MAX2392: tones at 2020.6MHz and 2023.98MHz (-35dBm/toner); receiver tuned for input RF of 2017.4MHz.
MAX2393: tones at 1910.0MHz and 1919.82MHz (-35dBm/toner); receiver tuned for input RF of 1900.0MHz.
MAX2390/MAX2400: tones at 1970.0MHz and 1980.18MHz (-35dBm/toner); receiver tuned for input RF of 1960.0MHz.
MAX2401: tones at 1852.4MHz and 1862.58MHz (-35dBm/toner); receiver tuned for input RF of 1842.4MHz.
Measure IM3 product at 180kHz.
- Note 8:** MAX2390/MAX2400: tones at 1963.5MHz and 1965.9MHz (-35dBm/toner); receiver tuned for input RF of 1960.0MHz, IM3 at 1.1MHz baseband.
MAX2401: tones at 1846MHz and 1848.4MHz (-35dBm/toner); receiver tuned for input RF of 1842.4MHz. IM3 at 1.2 MHz baseband.
- Note 9:** MAX2391/MAX2396: tones at 1950.0MHz and 1950.18MHz (-35dBm/toner); receiver tuned for input RF of 2140MHz.
MAX2390/MAX2400: tones at 1880.0MHz and 1880.18MHz (-35dBm/toner); receiver tuned for input RF of 1960.0MHz.
MAX2401: tones at 1747.4MHz and 1747.58MHz (-35dBm/toner); receiver tuned for input RF of 1842.4MHz.
Measure IM2 product at 180kHz.
- Note 10:** MAX2391/MAX2396: tones at 2155.0MHz and 2155.18MHz (-35dBm/toner); receiver tuned for input RF of 2140MHz.
MAX2392: tones at 2022.2MHz and 2022.38MHz (-35dBm/toner); receiver tuned for input RF of 2017.4MHz.
MAX2393: tones at 1915.0MHz and 1915.18MHz (-35dBm/toner); receiver tuned for input RF of 1900.0MHz.
MAX2390/MAX2400: tones at 1975.0MHz and 1975.18MHz (-35dBm/toner); receiver tuned for input RF of 1960.0MHz.
MAX2401: tones at 1857.4MHz and 1857.58MHz (-35dBm/toner); receiver tuned for input RF of 1842.4MHz.
Measure IM2 product at 180kHz.
- Note 11:** The receiver is tested using the DL reference measurement channel (12.2kbps) as specified in subclause C.3.1 in the 3GPP 25.101 standard document.
- Note 12:** I/Q differential output load impedance is 5k Ω minimum (10k Ω typical) in parallel with 5pF.

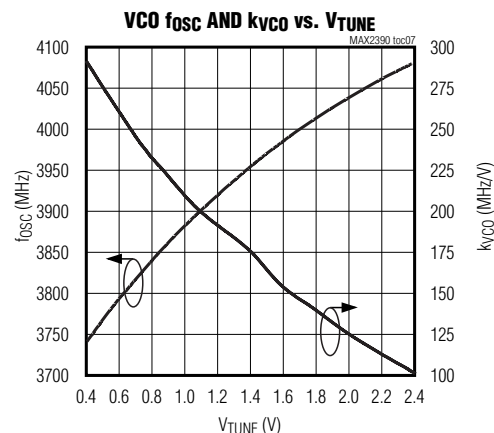
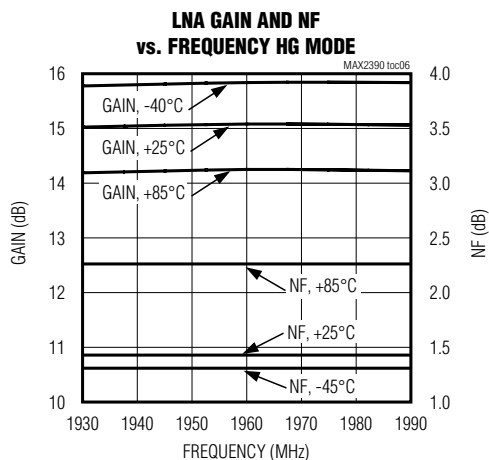
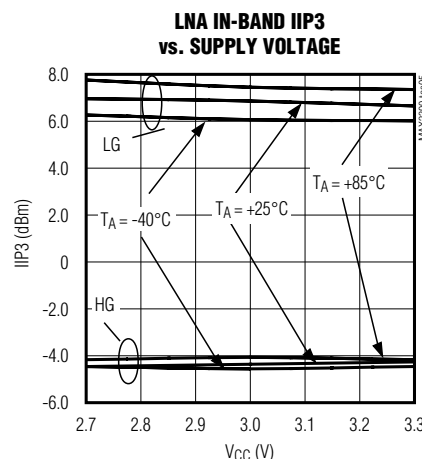
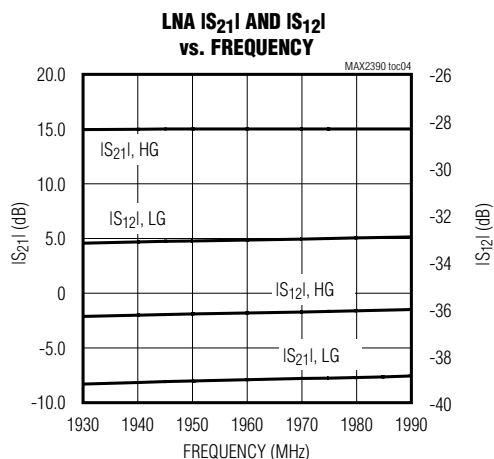
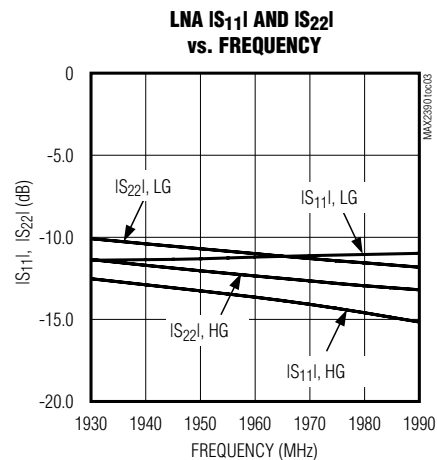
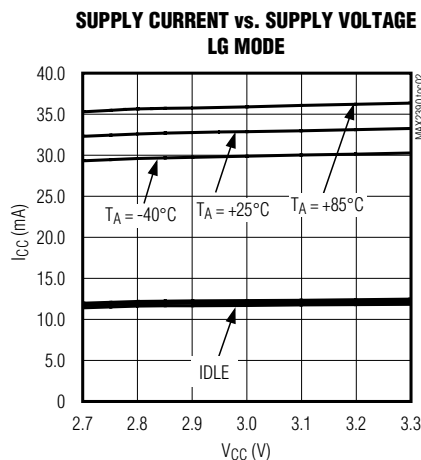
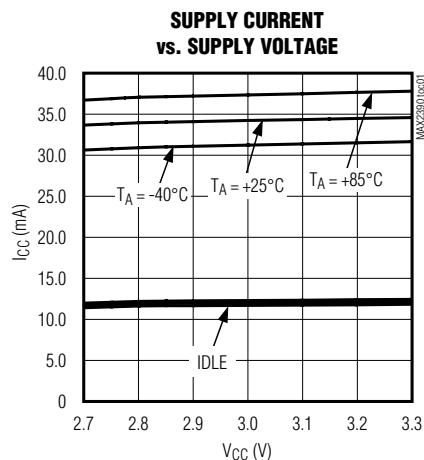
Timing Diagram



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2390 Typical Operating Characteristics

(MAX2390 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1960MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

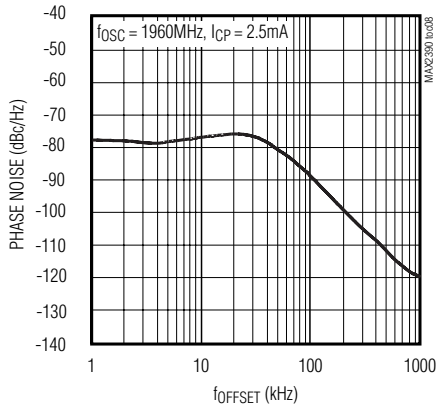


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

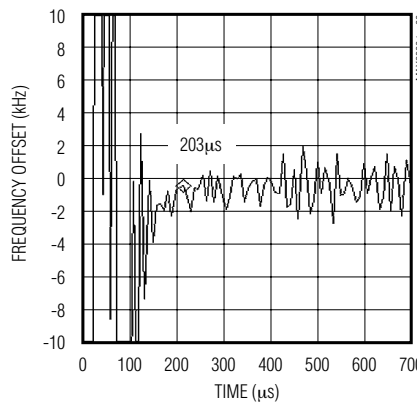
MAX2390 Typical Operating Characteristics (continued)

(MAX2390 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1960MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

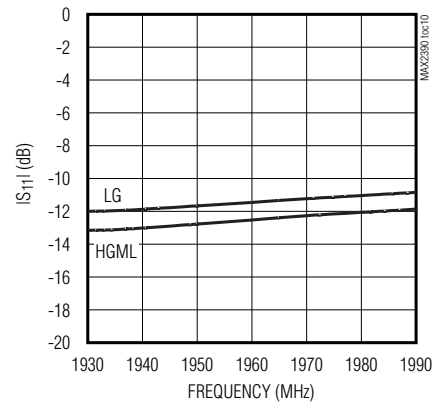
**SYNTHESIZER CLOSED-LOOP
PHASE NOISE**



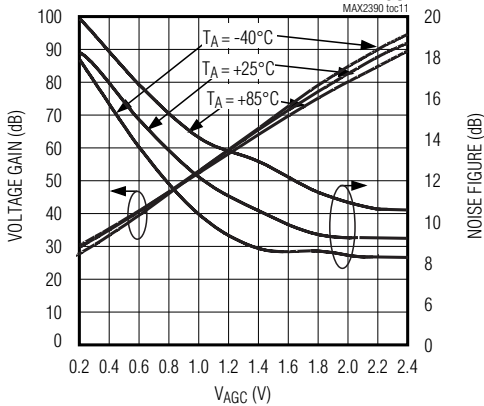
PLL SETTLING TIME 60MHz STEP



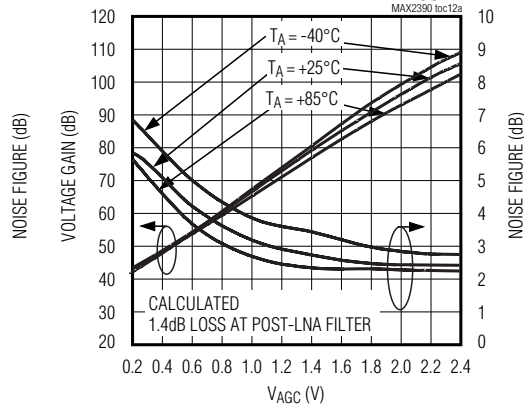
DEMODULATOR IS_{11} vs. FREQUENCY



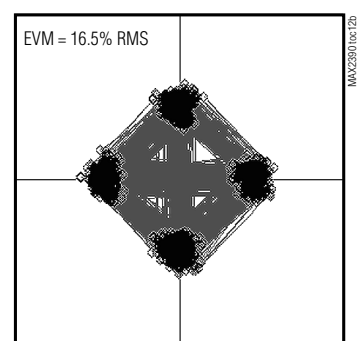
DEMODULATOR GAIN AND NF vs. V_{AGC}



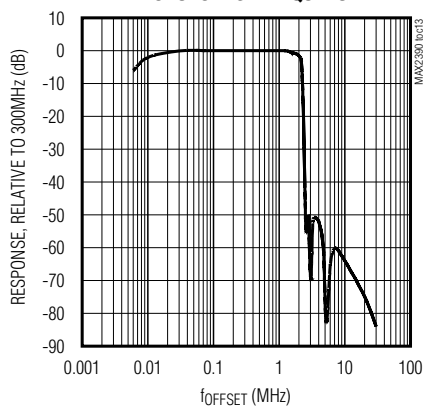
CASCADED GAIN AND NF vs. V_{AGC}



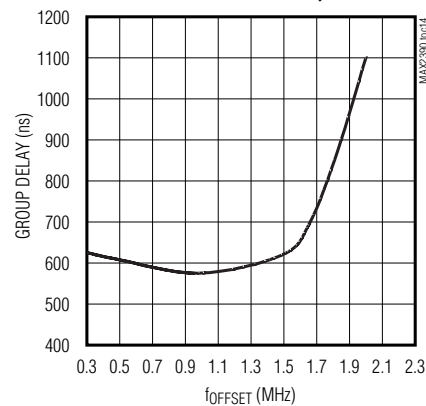
**COMPOSITE EVM
W-CDMA: PCCPCH + SCH**



**BASEBAND CHANNEL
RESPONSE vs. FREQUENCY**



**BASEBAND CHANNEL
GROUP DELAY vs. FREQUENCY**

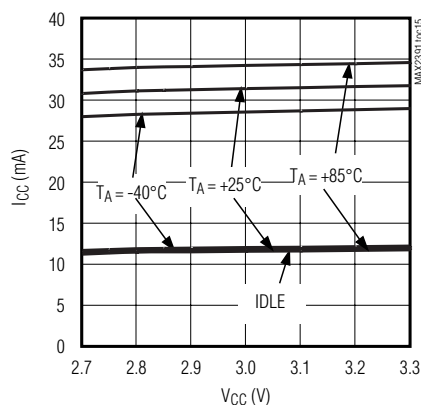


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

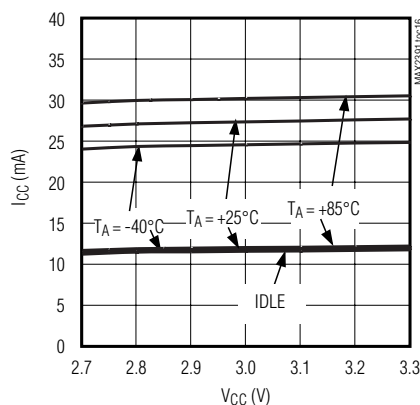
MAX2391 Typical Operating Characteristics

(MAX2391 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2140MHz$, $T_A = +25^{\circ}C$, unless otherwise noted.)

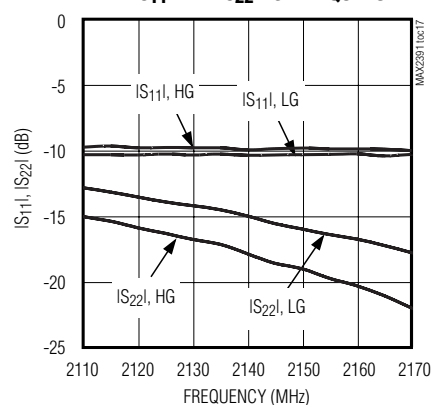
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGML MODE**



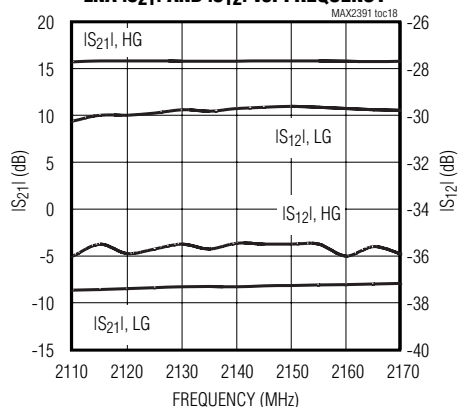
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



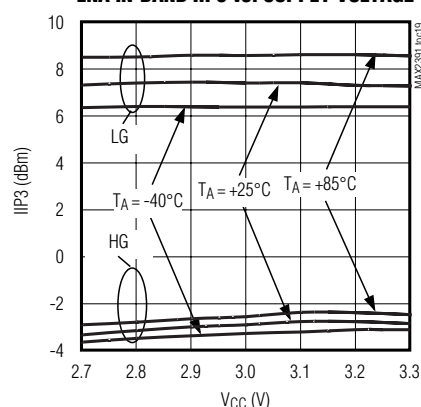
LNA $|S_{11}|$ AND $|S_{22}|$ vs. FREQUENCY



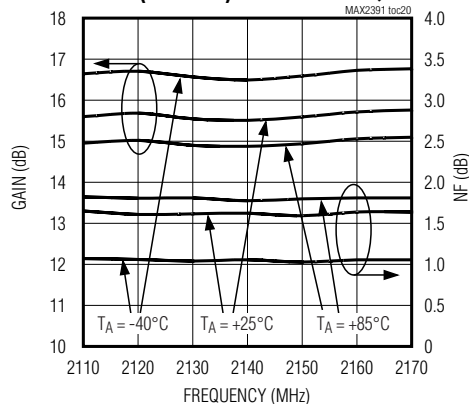
LNA $|S_{21}|$ AND $|S_{12}|$ vs. FREQUENCY



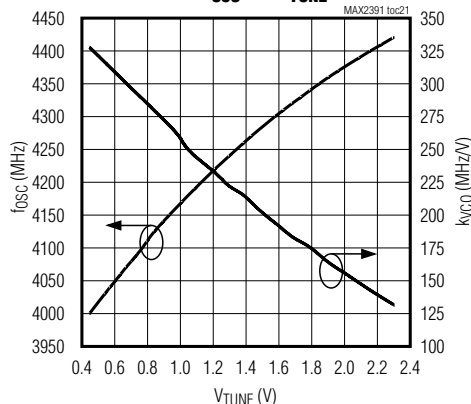
LNA IN-BAND IIP3 vs. SUPPLY VOLTAGE



LNA GAIN (HG MODE) AND NF vs. FREQUENCY



VCO f_{osc} vs. V_{TUNE}

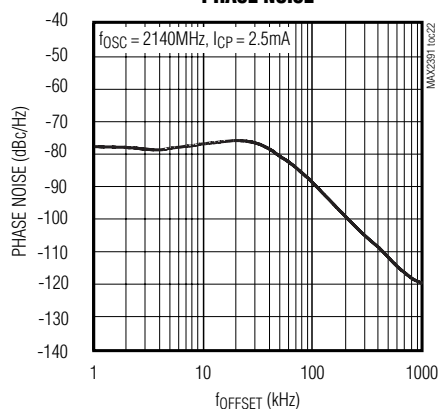


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

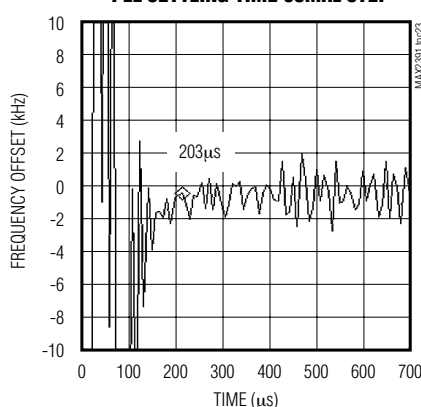
MAX2391 Typical Operating Characteristics (continued)

(MAX2391 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2140MHz$, $T_A = +25^{\circ}C$, unless otherwise noted.)

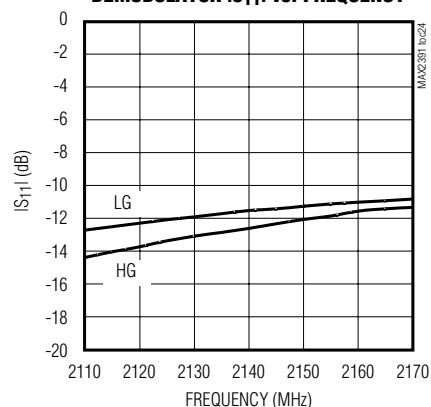
**SYNTHESIZER CLOSED-LOOP
PHASE NOISE**



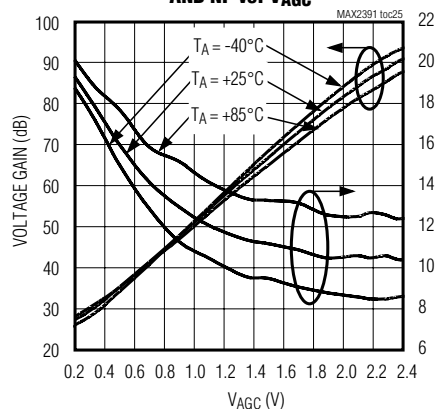
PLL SETTLING TIME 60MHz STEP



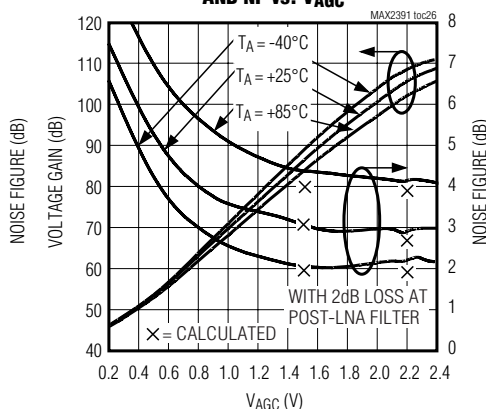
DEMODULATOR IS_{11} vs. FREQUENCY



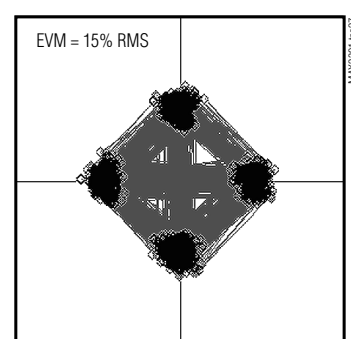
**DEMODULATOR GAIN (HGML MODE)
AND NF vs. V_{AGC}**



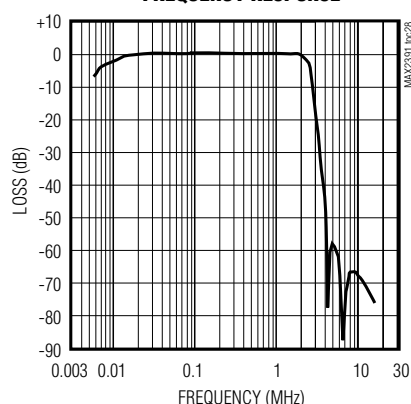
**CASCADED GAIN (HGML MODE)
AND NF vs. V_{AGC}**



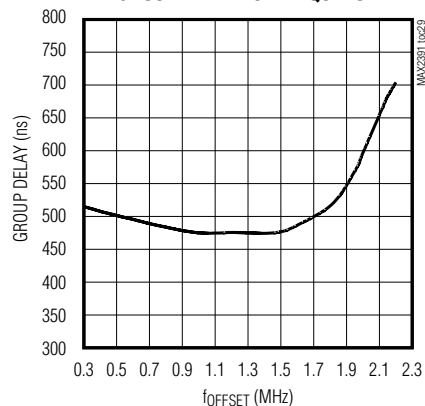
**COMPOSITE EVM
W-CDMA: PCCPCH + SCH**



**BASEBAND CHANNEL
FREQUENCY RESPONSE**



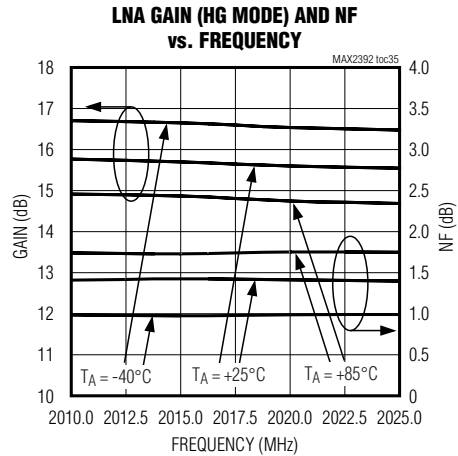
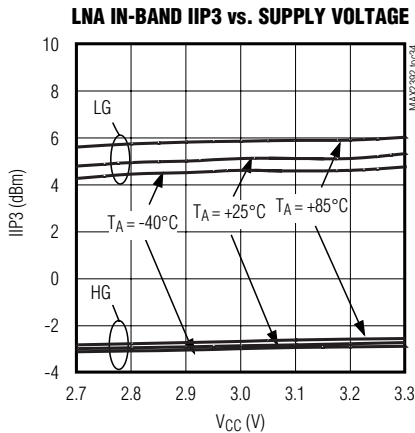
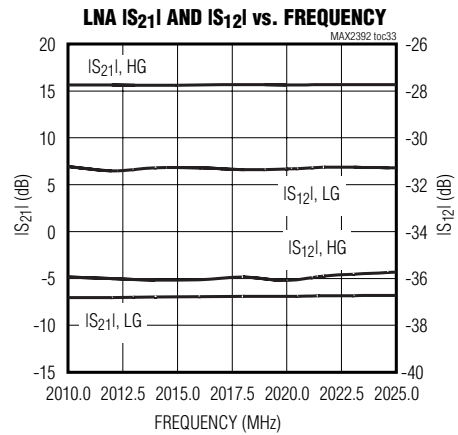
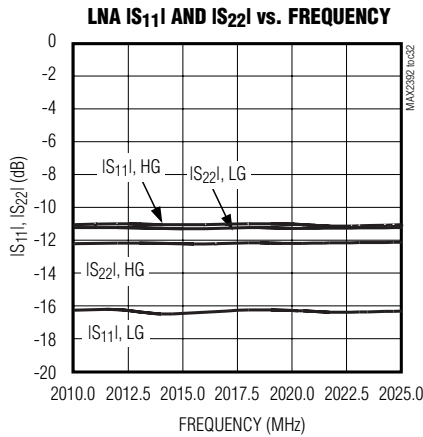
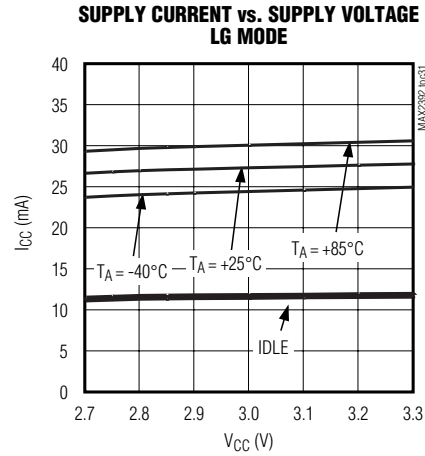
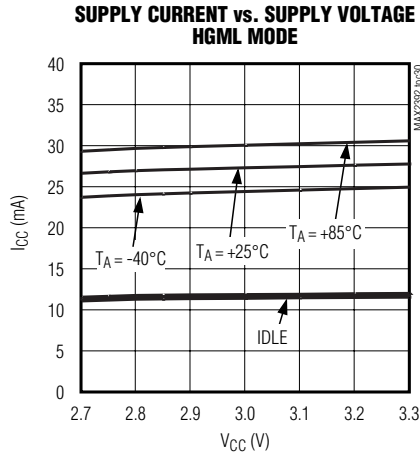
**BASEBAND CHANNEL
GROUP DELAY vs. FREQUENCY**



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2392 Typical Operating Characteristics

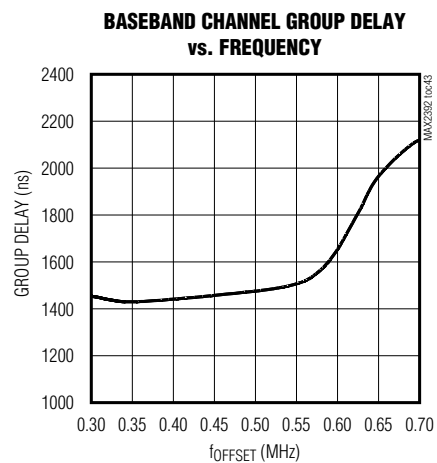
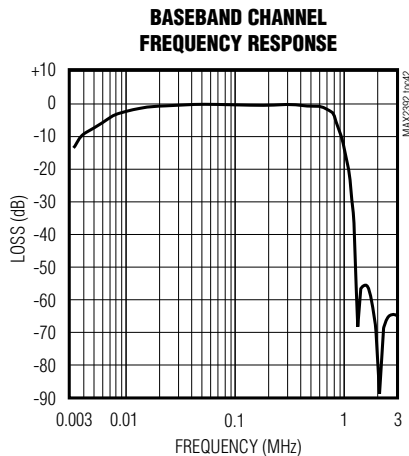
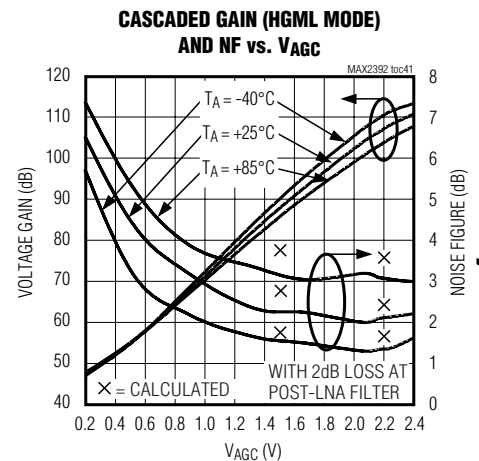
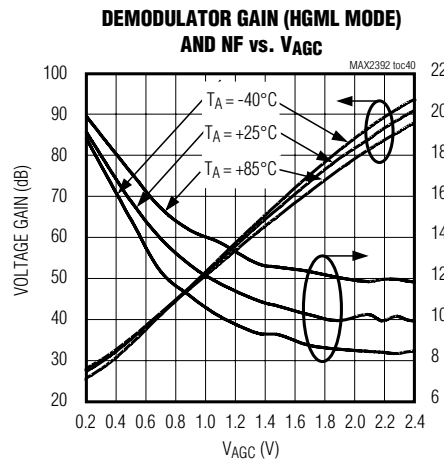
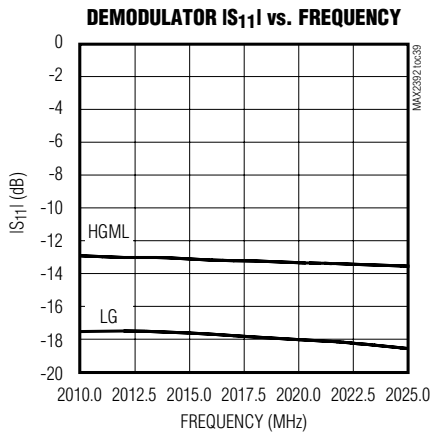
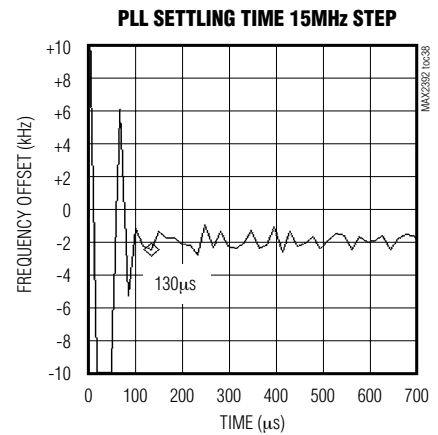
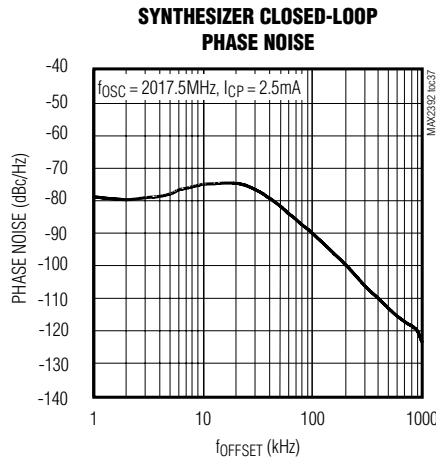
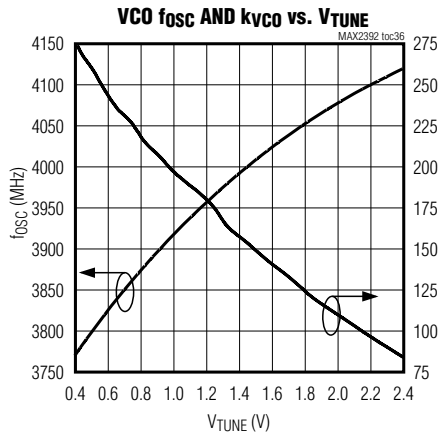
(MAX2392 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2017MHz$, $T_A = +25^{\circ}C$, unless otherwise noted.)



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2392 Typical Operating Characteristics (continued)

(MAX2392 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2017MHz$, $T_A = +25^{\circ}C$, unless otherwise noted.)

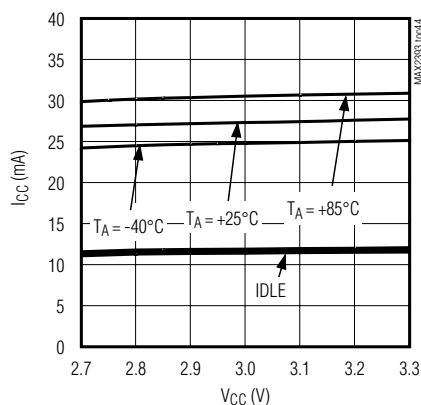


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

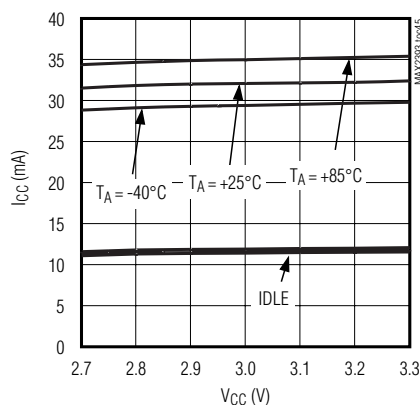
MAX2393 Typical Operating Characteristics

(MAX2393 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1910MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

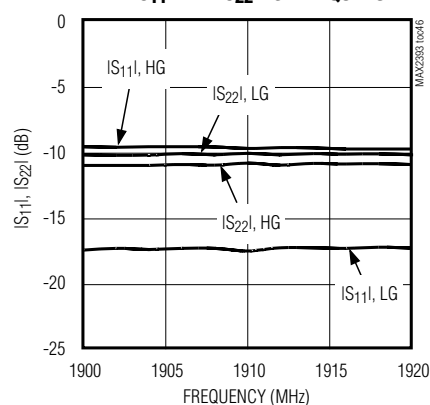
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



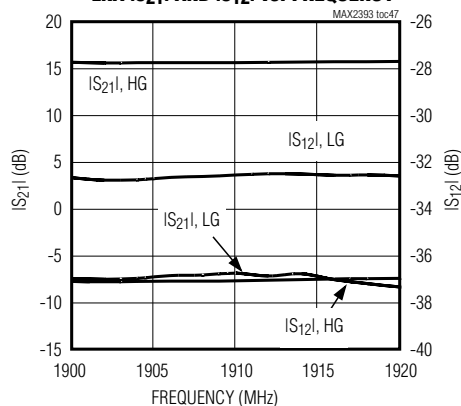
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGML MODE**



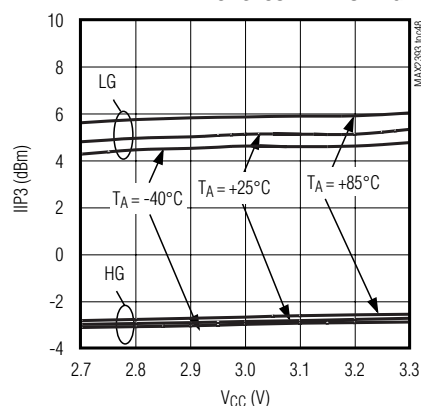
LNA IS_{11} AND IS_{22} vs. FREQUENCY



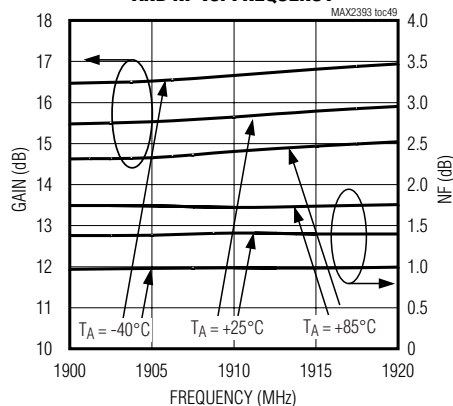
LNA IS_{21} AND IS_{12} vs. FREQUENCY



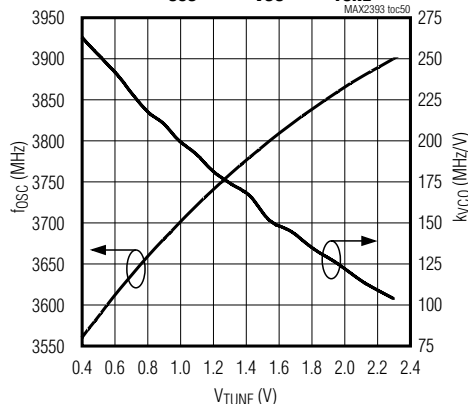
LNA IN-BAND IIP3 vs. SUPPLY VOLTAGE



**LNA GAIN (HG MODE)
AND NF vs. FREQUENCY**



VCO f_{osc} AND k_{VCO} vs. V_{TUNE}

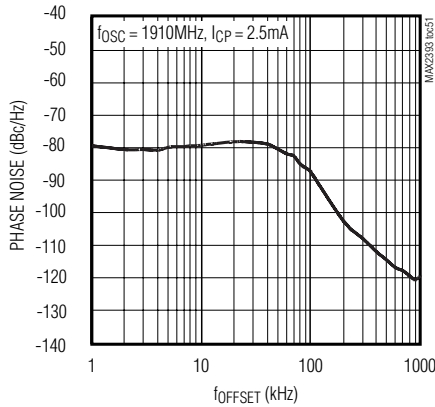


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

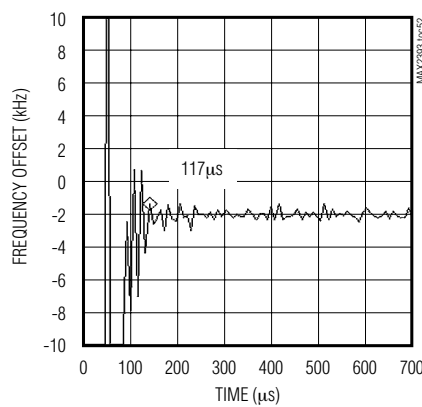
MAX2393 Typical Operating Characteristics (continued)

(MAX2393 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1910MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

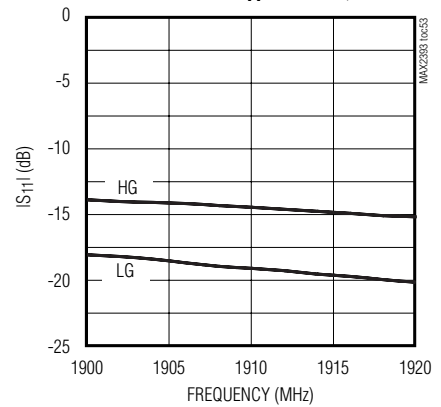
**SYNTHESIZER CLOSED-LOOP
PHASE NOISE**



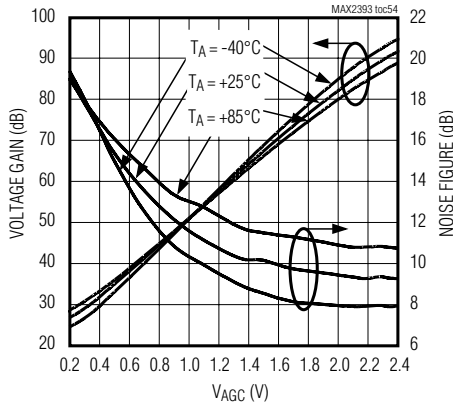
PLL SETTLING TIME 20MHz STEP



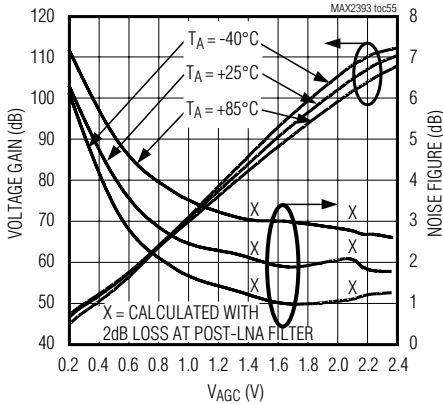
DEMODULATOR IS_{11} vs. FREQUENCY



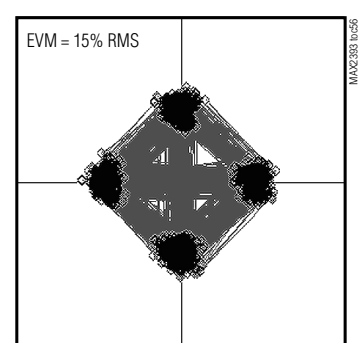
**DEMODULATOR GAIN (HGML MODE)
AND NF vs. V_{AGC}**



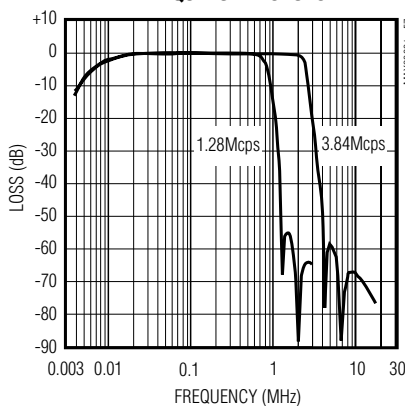
**CASCADED GAIN (HGML MODE)
AND NF vs. V_{AGC}**



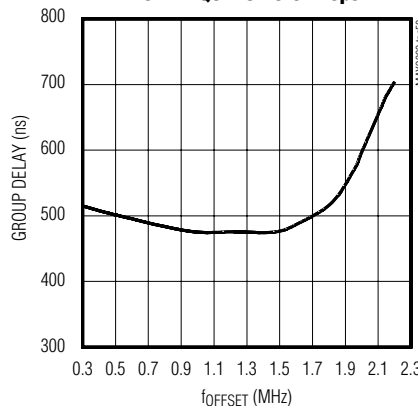
**COMPOSITE EVM
W-CDMA: PCCPCH + SCH**



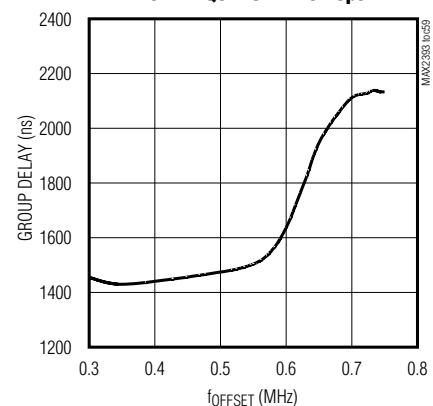
**BASEBAND CHANNEL
FREQUENCY RESPONSE**



**BASEBAND CHANNEL GROUP DELAY
vs. FREQUENCY 3.84Mcps**



**BASEBAND CHANNEL GROUP DELAY
vs. FREQUENCY 1.28Mcps**

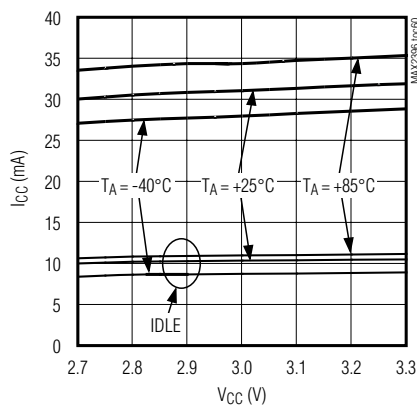


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

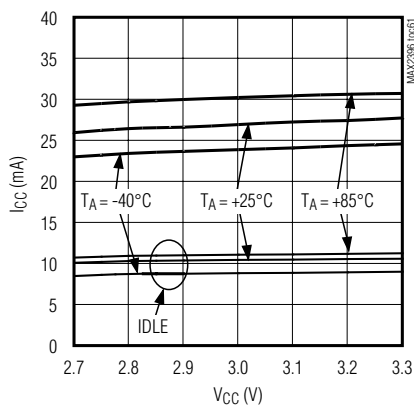
MAX2396 Typical Operating Characteristics

(MAX2396 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2140MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

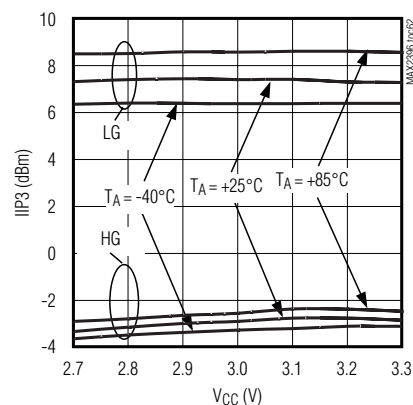
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGHL MODE**



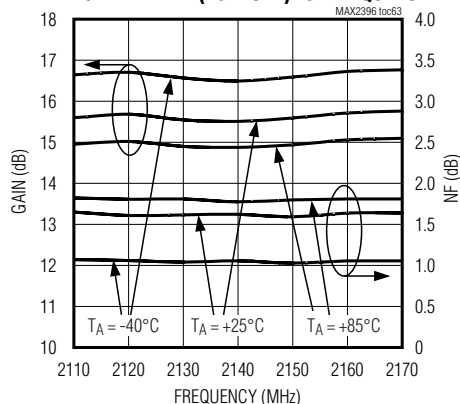
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



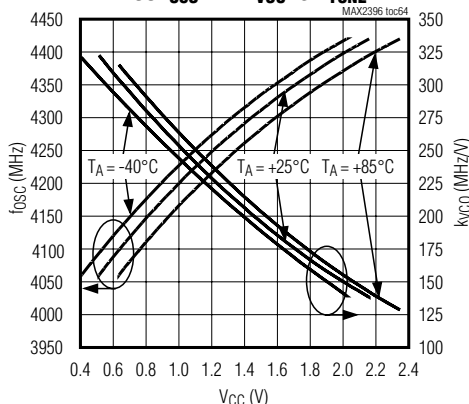
LNA IN-BAND IIP3 vs. SUPPLY VOLTAGE



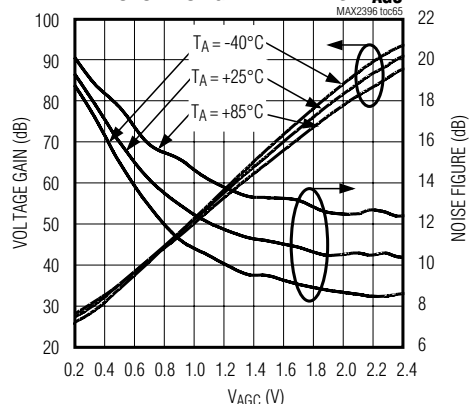
LNA GAIN AND NF (HG MODE) vs. FREQUENCY



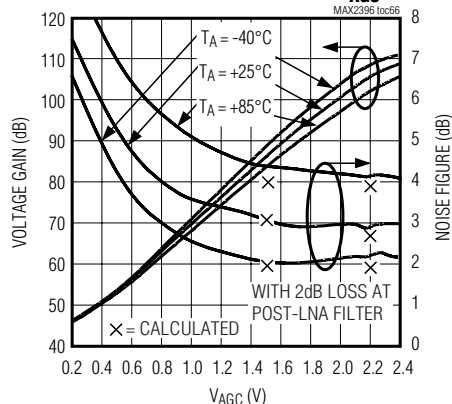
VCO f_{OSC} AND k_{VCO} vs. V_{TUNE}



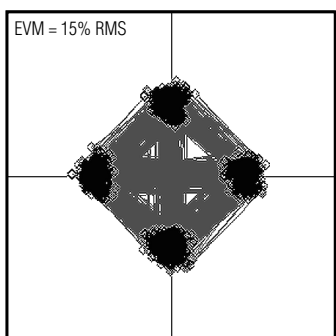
DEMODULATOR GAIN AND NF vs. V_{AGC}



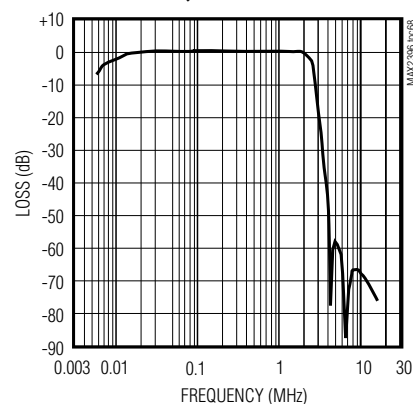
CASCADED GAIN AND NF vs. V_{AGC}



**COMPOSITE EVM
W-CDMA: PCCPCH + SCH**



FREQUENCY RESPONSE

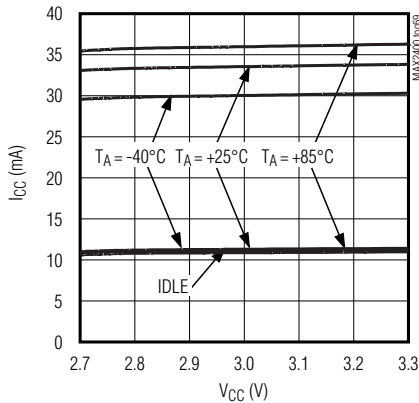


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

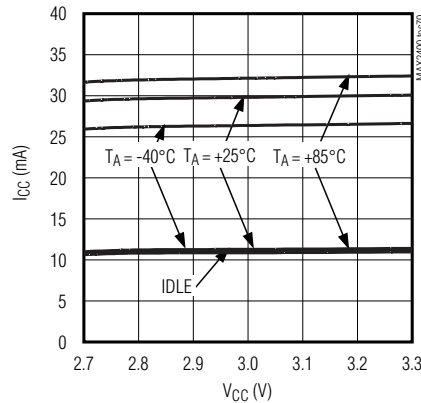
MAX2400 Typical Operating Characteristics

(MAX2400 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1960MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

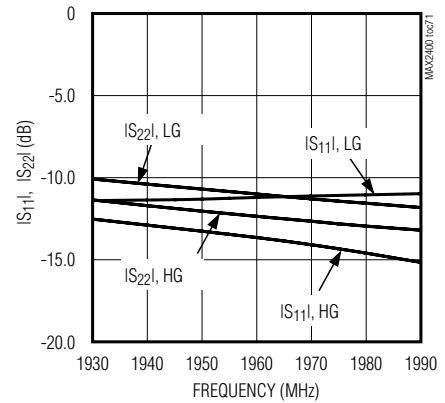
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGML MODE**



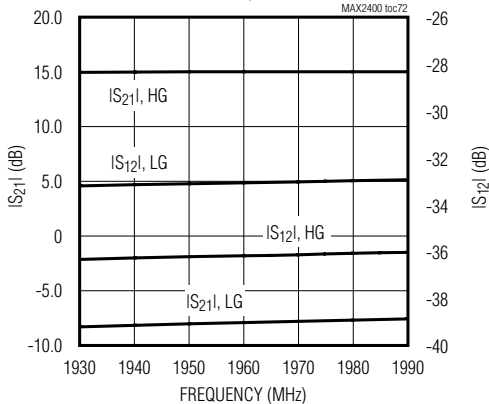
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



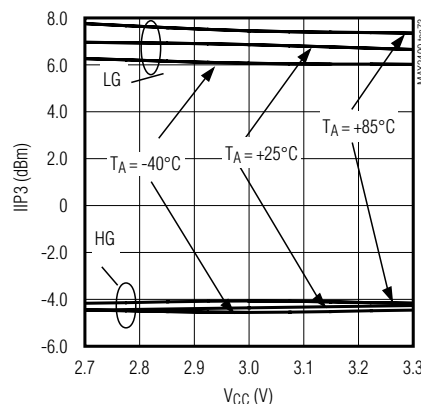
**LNA IS_{11} AND IS_{22}
vs. FREQUENCY**



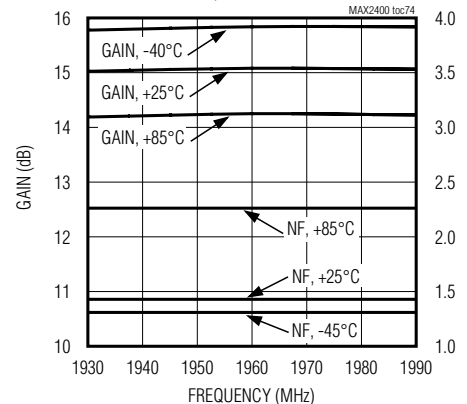
**LNA IS_{21} AND IS_{12}
vs. FREQUENCY**



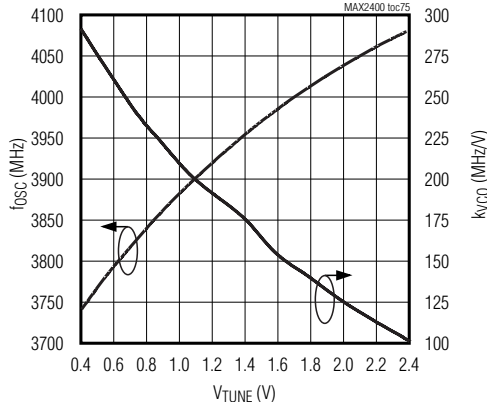
**LNA IN-BAND IIP3
vs. SUPPLY VOLTAGE**



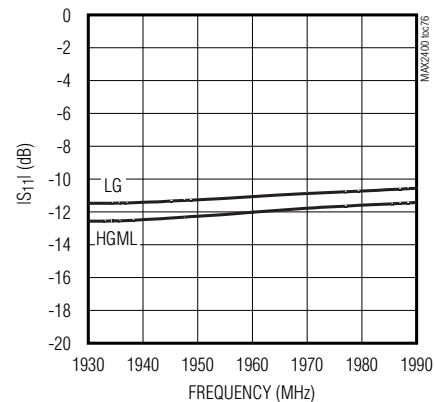
**LNA GAIN AND NF
vs. FREQUENCY HG MODE**



VCO f_{osc} AND k_{VCO} vs. V_{TUNE}



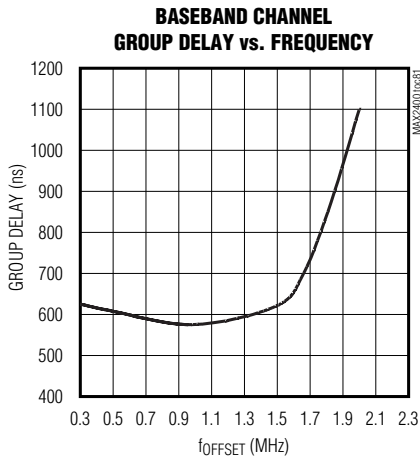
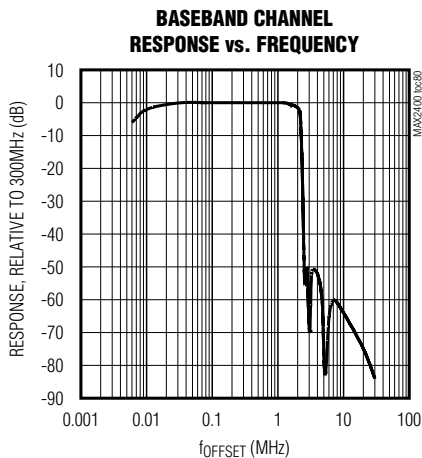
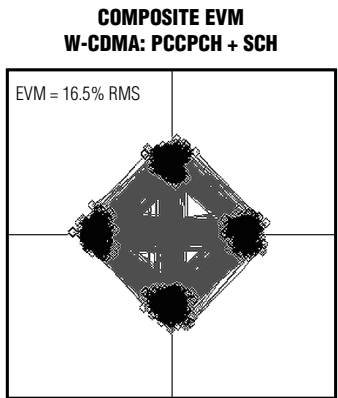
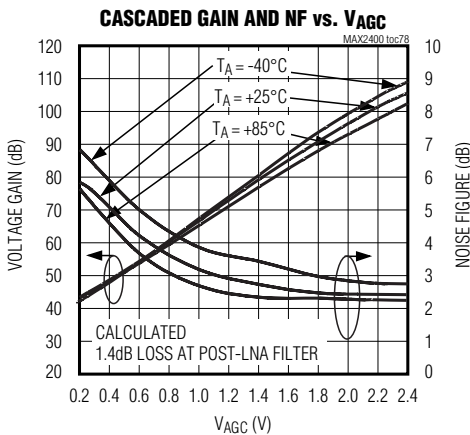
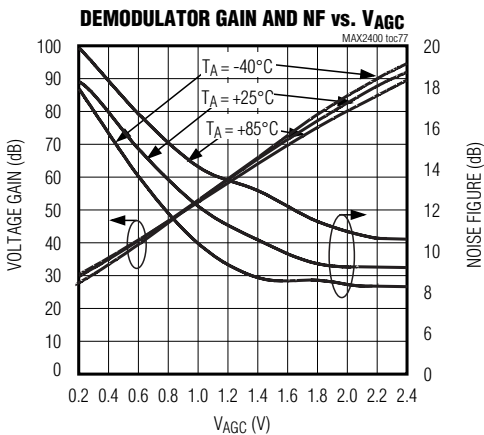
DEMODULATOR IS_{11} vs. FREQUENCY



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2400 Typical Operating Characteristics (continued)

(MAX2400 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1960MHz$, $T_A = +25^{\circ}C$, unless otherwise noted.)

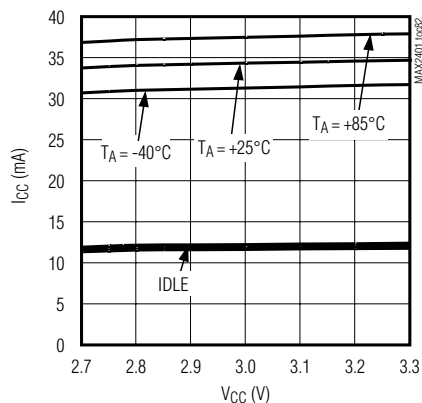


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

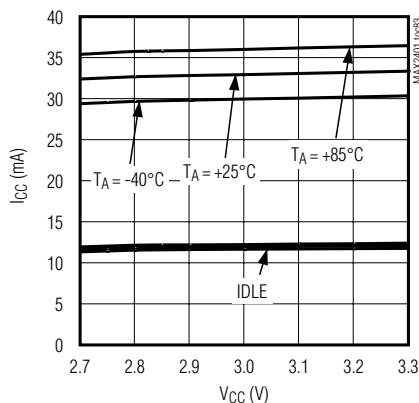
MAX2401 Typical Operating Characteristics

(MAX2401 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1842.4MHz$, $T_A = +25^{\circ}C$, unless otherwise noted.)

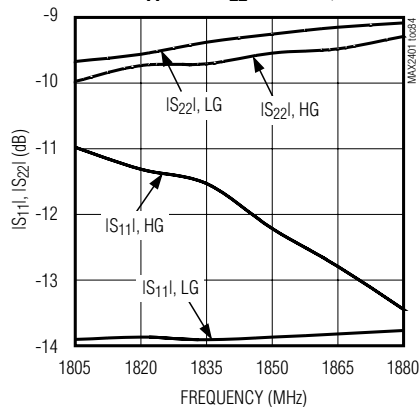
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGML MODE**



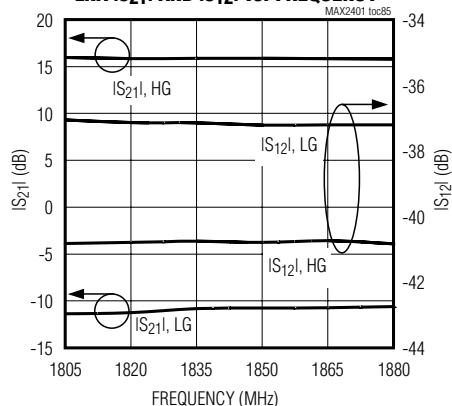
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



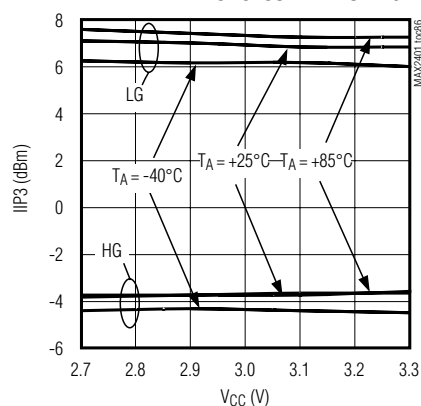
LNA $|S_{11}|$ AND $|S_{22}|$ vs. FREQUENCY



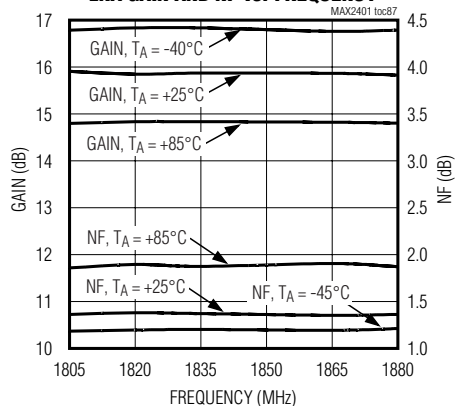
LNA $|S_{21}|$ AND $|S_{12}|$ vs. FREQUENCY



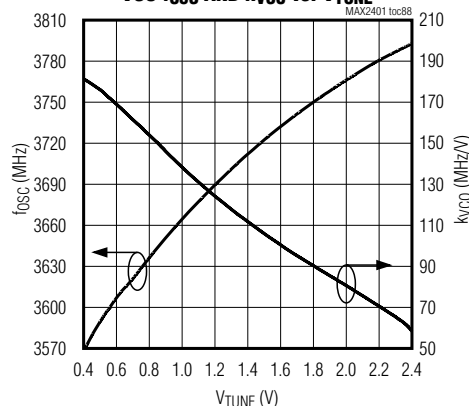
LNA IN-BAND IIP3 vs. SUPPLY VOLTAGE



LNA GAIN AND NF vs. FREQUENCY



VCO f_{osc} AND k_{VCO} vs. V_{TUNE}

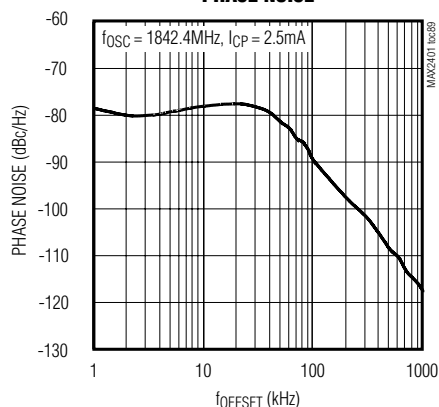


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

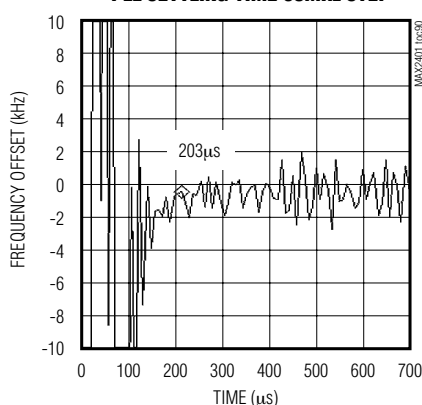
MAX2401 Typical Operating Characteristics (continued)

(MAX2401 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1842.4MHz$, $T_A = +25^{\circ}C$, unless otherwise noted.)

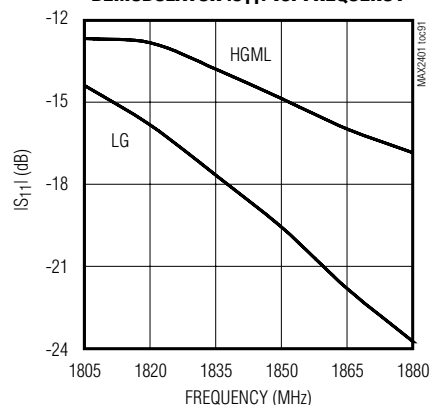
**SYNTHESIZER CLOSED-LOOP
PHASE NOISE**



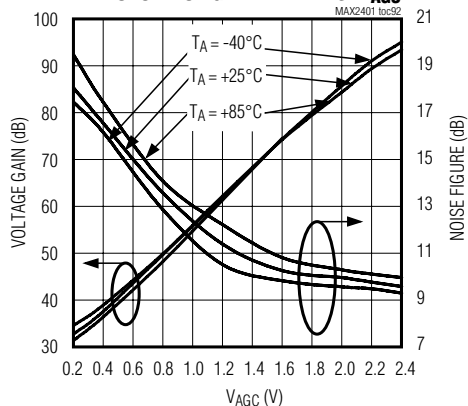
PLL SETTLING TIME 60MHz STEP



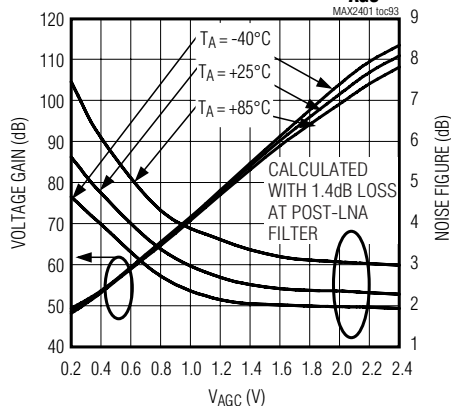
DEMODULATOR IS_{11} vs. FREQUENCY



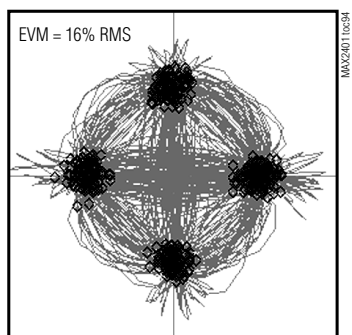
DEMODULATOR GAIN AND NF vs. V_{AGC}



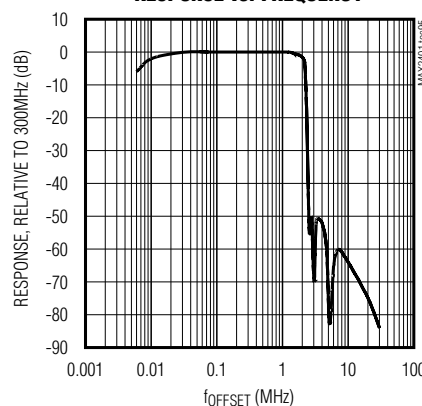
CASCADED GAIN AND NF vs. V_{AGC}



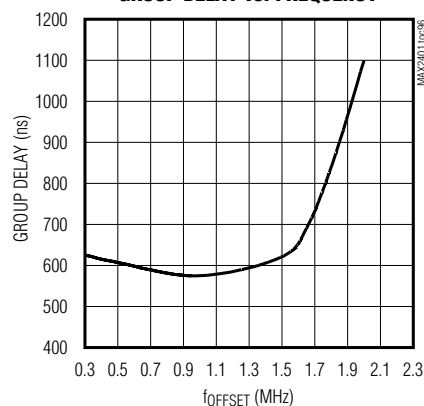
**COMPOSITE EVM
W-CDMA: PCCPCH + SCH**



**BASEBAND CHANNEL
RESPONSE vs. FREQUENCY**



**BASEBAND CHANNEL
GROUP DELAY vs. FREQUENCY**



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

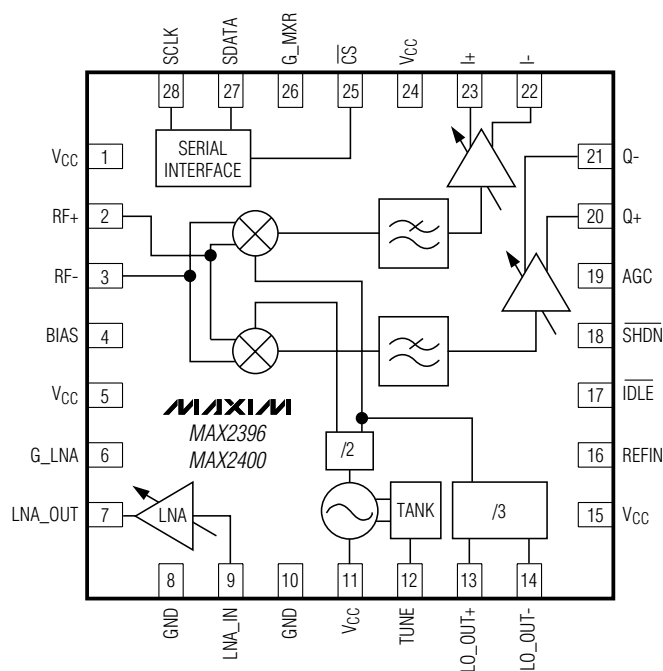
Pin Description

PIN	NAME	FUNCTION
1	VCC	Supply Pin for I/Q Mixers. This pin must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch. Use 100pF for RF bypassing to GND.
2	RF+	Noninverting RF Input to Zero-IF Demodulator (200Ω Differential Nominal Impedance Between RF+ and RF-)
3	RF-	Inverting RF Input to Zero-IF Demodulator (200Ω Differential Nominal Impedance Between RF+ and RF-)
4	BIAS	External Bias Resistor Connection
5	VCC	Supply Pin for LNA. This pin must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch. Use 100pF for RF bypassing to GND.
6	G_LNA	LNA Gain Mode Logic-Control Pin
7	LNA_OUT	LNA Output. Internally matched to 50Ω.
8	GND	RF Ground Return for LNA. Provide multiple vias to the system ground plane as close to the pin as possible.
9	LNA_IN	LNA Input. Externally matched to 50Ω. See the <i>Applications Information</i> section for more information.
10	GND	RF VCO Varactor Ground Return. Provide multiple vias to the system ground plane as close to the pin as possible.
11	VCC	Supply Pin for VCO. This pin must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch. Use 100pF for RF bypassing to GND.
12	TUNE	RF VCO Varactor TUNE Input. Connect PLL loop filter between CP and TUNE.
13	CP	(MAX2390–MAX2393, MAX2401) High-Impedance Output of the RF Charge Pump. The RF PLL's loop filter is connected between this pin and TUNE.
	LO_OUT+	(MAX2396/MAX2400) VCO Divide-by-3 Noninverting Output to Synthesizer
14	VCC	(MAX2390–MAX2393, MAX2401) Supply Pin for Synthesizer Charge Pump. Use 100nF for bypassing to GND.
	LO_OUT-	(MAX2396/MAX2400) VCO Divide-by-3 Inverting Output to Synthesizer
15	VCC	Supply Pin for On-Chip Digital Circuitry. Use 100nF for bypassing to GND.
16	REFIN	Synthesizer Reference Frequency Input. AC-couple to the reference source through 1nF.
17	LD	(MAX2390–MAX2393, MAX2401) Open-Drain Output Indicating LOCK Status of the RF PLL. It is open drain to wire-OR with LD from TX chip.
	IDLE	(MAX2396/MAX2400) Idle Mode Enable. Drive IDLE low to disable all blocks except serial bus, VCO, and divide-by-3 prescaler to PLL.
18	SHDN	Shutdown Logic Pin for Entire Receiver (Active Low)
19	AGC	Analog Input Pin Controlling the Baseband VGA Gain
20	Q+	Noninverting Baseband Output for Q Channel
21	Q-	Inverting Baseband Output for Q Channel
22	I-	Inverting Baseband Output for I Channel
23	I+	Noninverting Baseband Output for I Channel
24	VCC	Supply Pin for Baseband Circuitry. Use 100nF for bypassing to GND.
25	CS	3-Wire Serial Bus Enable Input (Active Low)
26	G_MXR	Mixer Gain Mode Logic-Control Pin
27	SDATA	3-Wire Serial Bus Data Input
28	SCLK	3-Wire Serial Bus Clock Input

MAX2390–MAX2393/MAX2396/MAX2400/MAX2401

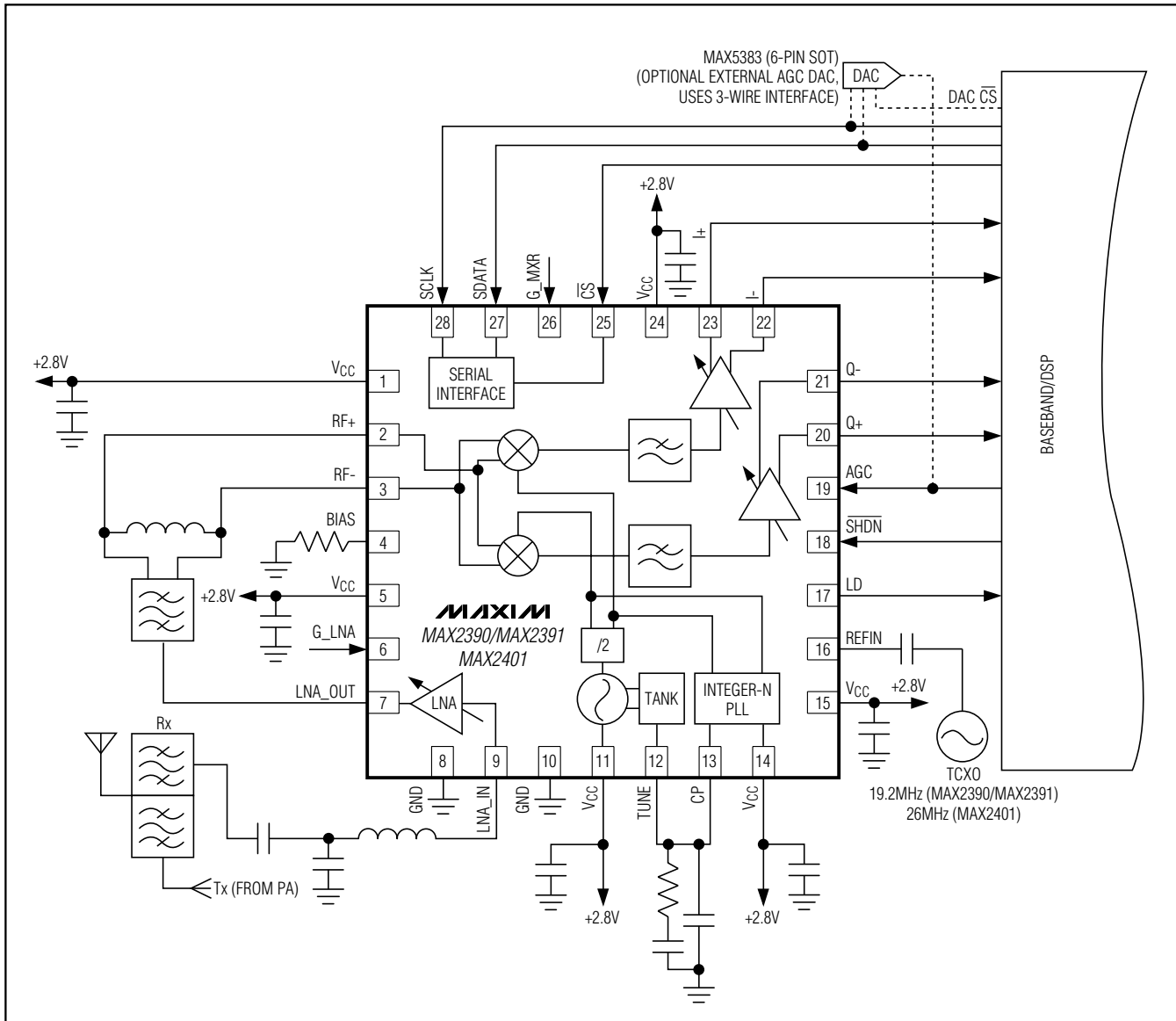
W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

Pin Configuration/Functional Diagram for MAX2396/MAX2400



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

W-CDMA FDD Receiver Operating Circuit (MAX2390/MAX2391/MAX2401)



MAX2390-MAX2393/MAX2396/MAX2400/MAX2401

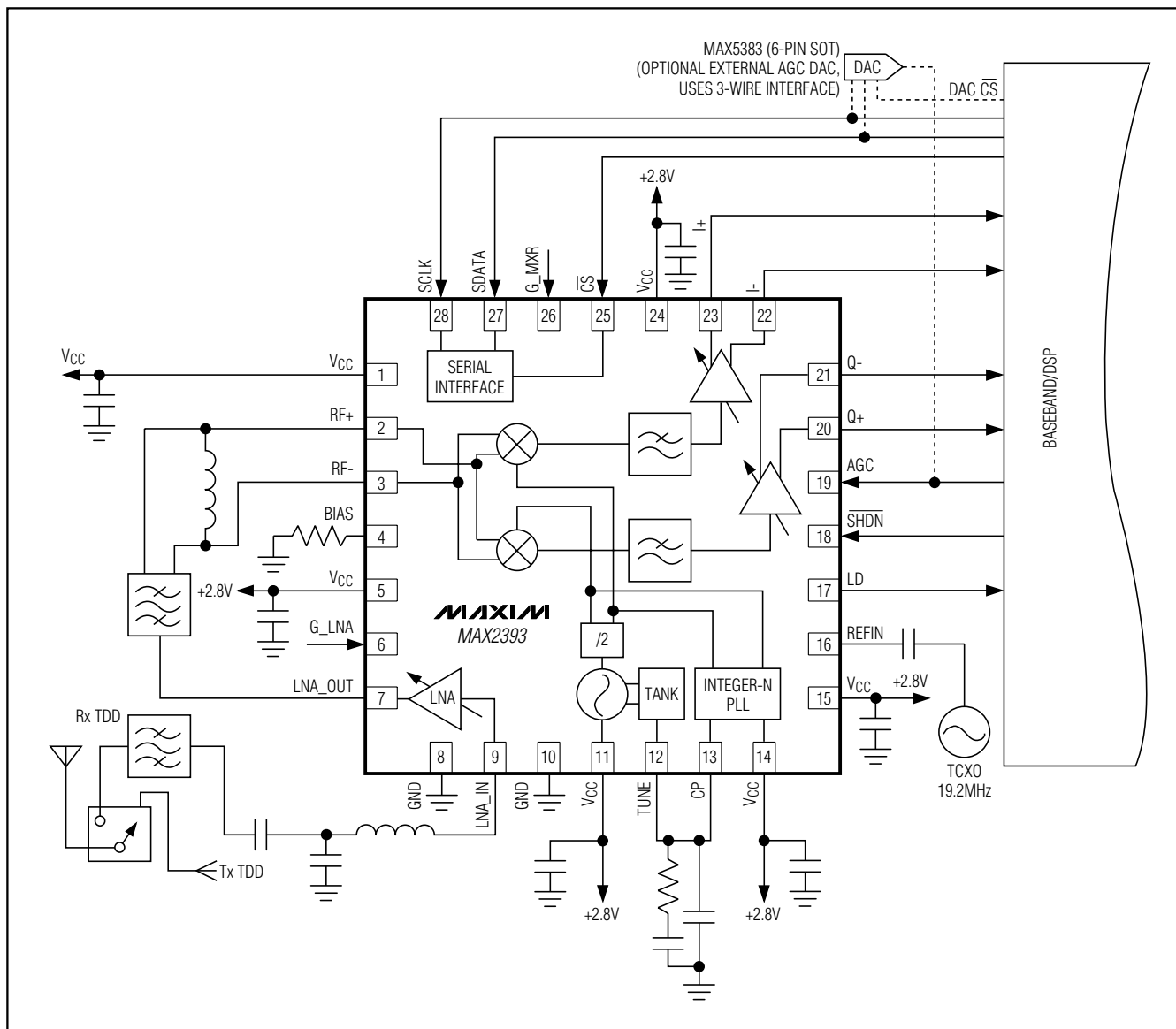
MAX2390-MAX2393/MAX2396/MAX2400/MAX2401

MAX2390-MAX2393/MAX2396/MAX2400/MAX2401



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

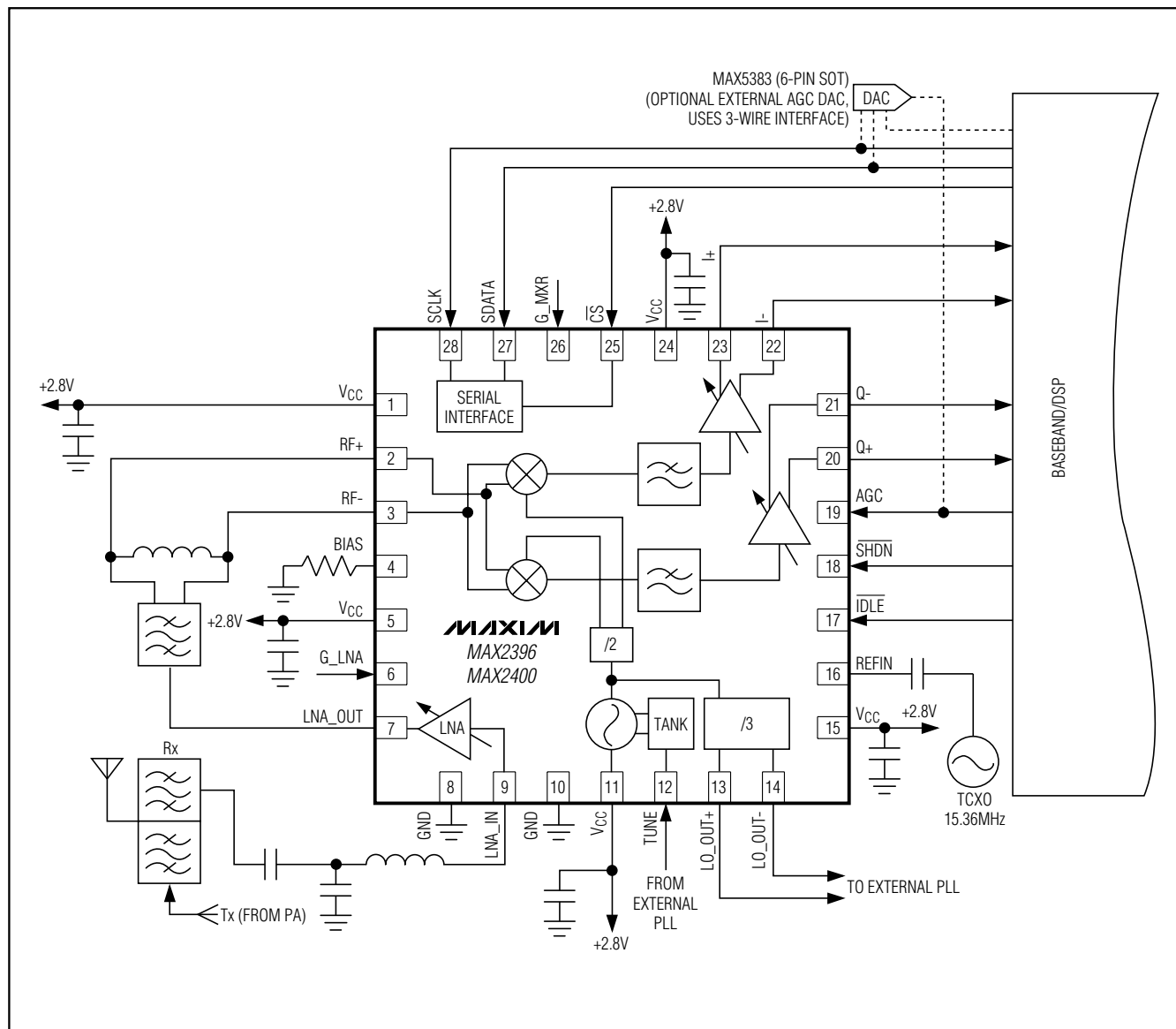
W-TDD Receiver Operating Circuit (MAX2393)



MAX2390-MAX2393/MAX2396/MAX2400/MAX2401

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

W-CDMA FDD Receiver Operating Circuit (External Synthesizer) (MAX2396/MAX2400)



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

Detailed Description

With the exception of the analog-input AGC, all functionality of these direct-conversion receivers can be controlled through the 3-wire serial interface (SPI™/QSPI™/MICROWIRE™ compatible).

Register Definition

All devices in this family have two programmable 20-bit registers: the configuration register (CONFIG) and the control register (OPCNTRL). The MAX2391/MAX2392/MAX2393/MAX2401 have two additional programmable 20-bit registers: the main PLL divide register (RFM) and the reference PLL divide register (RFR). The 4 least significant bits of the data sent are the register's address. The 16 most significant bits are used for register data. All registers contain a few don't care bits. These can be either 0 or 1 and do not affect operation. Tables 1a and 1b provide a register summary. Data is shifted in MSB first. When $\overline{CS}$ is low, data is shifted with the rising edge of the clock. When $\overline{CS}$ transitions to high, the shift register is latched into the register selected by the contents of the address bits. Power-up defaults for the four registers are shown in Table 2.

The RFM register sets the main-frequency divide ratio for the RF PLL. The RFR register sets the reference-frequency divide ratio. The RF LO frequency can be determined by the following:

$$\text{RF LO frequency} = f_{\text{REFIN}} \times (\text{RFM} / \text{RFR})$$

where f_{REFIN} is the external input reference frequency

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SPI and QSPI are trademarks of Motorola, Inc.

for the MAX2390–MAX2393, MAX2401.

The operation control register (OPCNTRL) and the configuration register (CONFIG) are used to program the receiver for the appropriate mode of operation. See Tables 3 and 4 for the function of each bit.

The test register is used to set the receiver in factory testing mode. It should only be programmed at receiver turn-on with the word 0370 (hex) for MAX2390–MAX2393, MAX2401 and 2370 (hex) for MAX2396/MAX2400.

Power Management

Bias control is distributed among several functional sections and can be controlled to accommodate different power-down modes as shown in Table 5.

The IC has three bias states: SHUTDOWN, IDLE, and ON. SHUTDOWN can be asserted by either a hardware control line ($\overline{SHDN}$) or by bit 5 of the operation control register (OPCNTRL.SHDN). When the serial interface is used to shut down the part, an internal linear regulator, with $I_Q \approx 90\mu\text{A}$, stays functional to keep the serial interface operational. Use the $\overline{SHDN}$ logic-control pin to bring quiescent current below $10\mu\text{A}$. Register bit settings maintain their values after a hard shutdown, provided $\overline{CS}$ remains high. IDLE mode disables the LNA, I/Q mixers, and baseband circuitry, but keeps the serial interface and synthesizer operational, dropping quiescent current to 11.5mA . The entire receiver is ON when $\overline{SHDN}$ is high and OPCNTRL.SHDN and OPCNTRL.IDLE bits (MAX2390–MAX2393, MAX2401) or the IDLE pin (MAX2396/MAX2400) are set to 1; the typical supply current is 32mA .

Table 1a. Register Definition (MAX2390–MAX2393, MAX2401)

REGISTER NAME	20-BIT REGISTER																LSB			
	DATA 16 BITS																ADDRESS 4 BITS			
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	A3	A2	A1	A0
RFM	×	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	0	0	1	1
RFR	×	×	×	×	×	×	×	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	1	1	1
OPCNTRL	×	×	×	×	(RESERVED)	(RESERVED)	(RESERVED)	(RESERVED)	RC1	RC0	$\overline{SHDN}$	$\overline{IDLE}$	GLNA	LMXR	GMXR	VCM	1	0	1	1
CONFIG	×	×	×	×	(RESERVED)	(RESERVED)	(RESERVED)	(RESERVED)	(RESERVED)	BW_SEL	DC_CANCEL_EN	RF_PLL_EN	VCO_EN	CP1	CP0	LNA_EN	1	1	1	1

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

Table 1b. Register Defintion (MAX2396/MAX2400)

REGISTER NAME	20-BIT REGISTER																LSB			
	DATA 16 BITS																ADDRESS 4 BITS			
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	A3	A2	A1	A0
OPCNTRL	X	X	X	X	(RESERVED)	(RESERVED)	(RESERVED)	(RESERVED)	RC1	RC0	SHDN	(RESERVED)	GLNA	LMXR	GMXR	VCN	1	0	1	1
CONFIG	X	X	X	X	(RESERVED)	(RESERVED)	(RESERVED)	(RESERVED)	(RESERVED)	(RESERVED)	DC_CANCEL_EN	LO_GEN_EN	VCO_EN	(RESERVED)	(RESERVED)	LNA_EN	1	1	1	1

Data shifted in MSB first.
 X represents a "don't care."
 Set all (RESERVED) bits to 0.

Table 2. Power-Up Default Register Settings

REGISTER	ADDRESS	DEFAULT	FUNCTION		
RFM	0011 _b	0x29CC (10780 _{DEC})*	MAX2391	RF Main-Divider Count	
		0x2768 (10088 _{DEC})*	MAX2392		
		0x254E (9550 _{DEC})*	MAX2393		
		0x2648 (9800 _{DEC})*	MAX2390, MAX2401		
RFR	0111 _b	0x0060 (0096 _{DEC})*	MAX2390/MAX2391/MAX2393/MAX2401		RF Reference-Divider Count
		0x0041 (0065 _{DEC})*	MAX2392		
OPCTRL	1011 _b	03B hex	Operation control settings		
CONFIG	1111 _b	07F hex	Configuration control settings		
TEST	0001 _b	0370 hex**	MAX2390–MAX2393, MAX2401		Disables Test Mode
		2370 hex**	MAX2396/MAX2400		

Data shifted in MSB first.
 X represents a "don't care."
 Set all (RESERVED) bits to 0.
 *200kHz comparison frequency.
 **Needs to be programmed at receiver turn-on.

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

Table 3. Operation Control Register (OPCNTRL, Address 1011)

BIT (B0 = LSB)	POWER-UP STATE	BIT NAME	FUNCTION
B11, B10, B9, B8	0 0 0 0	(RESERVED)	Set to zero for normal operation.
B7, B6	0 0	RC1, RC0	Sets the -3dB corner of the highpass filter used for DC offset removal at baseband (only possible when the automatic DC-offset-cancellation bit (CONFIG.B5) is disabled): 0 0 = 8.6kHz highpass corner 0 1 = 17.2kHz highpass corner 1 0 = 100kHz highpass corner 1 1 = 1MHz highpass corner
B5	1	$\overline{\text{SHDN}}$	Zero shuts down everything except serial interface and registers, retaining their values.
B4	1	$\overline{\text{IDLE}}$	For MAX2390–MAX2393/MAX2401: Zero shuts down everything except RF PLL, RF VCO, serial interface, and registers, retaining their values.
		(RESERVED)	For MAX2396/MAX2400: Set to 1 for normal operation.
B3	1	GLNA	Sets LNA operating mode according to the following: 1 = high gain 0 = low gain
B2	0	LMXR	Sets mixer linearity in high-gain mode: 0 = medium linearity 1 = high linearity
B1	1	GMXR	Sets MIXER operating mode according to the following: 1 = high gain 0 = low gain
B0	1	VCM	Sets output common-mode voltage for baseband I/Q outputs: 0 = 1.2V 1 = 1.42V

MAX2390–MAX2393/MAX2396/MAX2400/MAX2401

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

Table 4. Configuration Register (CONFIG, Address 1111)

BIT	POWER-UP STATE	BIT NAME	FUNCTION
B11, B10, B9, B8, B7	0 0 0 0 0	(RESERVED)	Set to 0 for normal operation.
B6	1	BW_SEL	For MAX2393 only: 1 = selects the 3G W-CDMA mode for baseband filters. 0 = selects the TD-SCDMA mode for baseband filters.
		(RESERVED)	Set to 1 for normal operation.
B5	1	DC_CANCEL_EN	0 = disables the automatic DC-offset-cancellation circuit.
B4	1	RF_PLL_EN	For MAX2390–MAX2393/MAX2401: 0 = disables the RF PLL + LO generation circuit.
		LO_GEN_EN	For MAX2396/MAX2400: 0 = disables the LO generation circuit.
B3	1	VCO_EN	0 = disables the VCO.
B2, B1	1 1	CP1, CP0	For MAX2390–MAX2393/MAX2401: A 2-bit word sets the RF charge-pump current as follows: 0 0 = 1000µA 0 1 = 1500µA 1 0 = 2000µA 1 1 = 2500µA
		(RESERVED)	For MAX2396/MAX2400: Set to 11 for normal operation.
B0	1	LNA_EN	0 = disables on-chip LNA. Set to zero for external LNA.

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

Table 5. Power-Down Modes

POWER-DOWN MODES	COMMENTS	LOGIC			SERIAL INTERFACE	LNA + I/Q MIXERS + BB CIRCUITRY	RF VCO + RF PLL + LO GENERATION
		SHDN PIN	SHDN BIT	IDLE BIT			
SHUTDOWN	SHDN pin is HIGH, SHDN bit is ZERO. All blocks are OFF except serial bus and registers, which retain their values; a LOW on SHDN pin overrides SHDN bit.	1	0	X	ON	OFF	OFF
	SHDN pin is LOW. All blocks are OFF; registers retain their preshutdown values.	0	X		OFF		
IDLE	IDLE bit (OPCTRL.B4) is ZERO. All blocks are OFF except RF PLL, RF VCO, serial bus, and registers, which retain their values.	1	1	0	ON	OFF	ON

Table 6. Operational Modes

MODE*	EXTERNAL CONTROL PINS/ OPCTRL REGISTER BITS					CORRESPONDING LNA MODE	CORRESPONDING MIXER MODE
	MIXER			LNA			
	LMXR (BIT)	GMXR		GLNA			
		(PIN)	(BIT)	(PIN)	(BIT)		
HGML	0	1	1	1	1	High gain	High gain, medium linearity
HGHL	1	1	1	1	1	High gain	High gain, high linearity
MG	X	1	0	1	1	High gain	Low gain
		0	X				
LG	X	1	0	1	0	Low gain	Low gain
		0	X	0	X		

*Definitions:

HGML: high gain, medium linearity

HGHL: high gain, high linearity

MG: medium gain

LG: low gain

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

Applications Information

LNA and RFIN Matching

The LNA requires a simple two-element 50Ω matching network at the input. Use the layout and matching network provided in the EV kit as a reference. The LNA input is internally biased, so be sure to use a series 100pF DC blocking capacitor in front of the matching network.

The LNA offers a 23dB gain step with less than 10 degrees phase change, selectable with either a dedicated logic pin (G_LNA) or bit 3 in the operation control register (OPCTRL.GLNA).

LNA output matching is provided on-chip, offering better than 2:1 VSWR. The required DC blocking capacitor is provided on-chip, so the LNA output can be connected directly to the RF SAW filter or balun.

I/Q Mixers

The mixers' differential input impedance is 200Ω , allowing an easy interface to commercially available differential-output Rx SAW filters or 1:4 baluns. No DC blocks are required, but a single, small shunt inductor is required to resonate out the parasitic capacitance from the SAW filter and IC package.

The mixer offers an 11dB gain step, which is controlled by either the logic-control pin (G_MXR) or bit 1 of the operation control register (OPCTRL.GMXR). This offers the option to switch the mixer into a low-gain state if required, reducing current consumption by about 3mA. Use the mixer gain step and AGC before reducing LNA gain for optimum receiver dynamic range.

Baseband I/Q Filters

All receiver channel selectivity is implemented fully on-chip, with greater than 40dB adjacent channel selectivity (ACS). This eliminates the need for any additional filtering by any subsequent baseband processor.

The group delay of the integrated filters is compensated through on-chip equalizers for optimum EVM.

AGC

The AGC circuitry of the baseband amplifiers offers linear (dB/V) gain control for the receiver. With the AGC voltage from 0.3V to 2.4V, the VGA section provides 60dB gain-control range, for a total of 95dB including the LNA and mixer gain steps.

The AGC control line has an input impedance of more than $100k\Omega$ at DC. Internal capacitance creates a single

pole at approximately 2MHz; this provides some high-frequency filtering, thereby reducing AM distortion.

For applications using a baseband processor with digital-only AGC, Maxim offers an 8-bit voltage-output AGC DAC with an SPI/QSPI/MICROWIRE interface in a tiny 6-pin SOT23 package. Especially designed as a low-cost, all-in-one solution for cellular handset AGC, the MAX5383 offers the following features: a serial interface good to 10MHz, guaranteed operation from a 2.7V to 3.6V supply, on-chip 2V reference, $<\pm 10\%$ full-scale error, $<\pm 1\text{LSB}$ INL/DNL, $<1\mu\text{A}$ shutdown, and a miniscule $150\mu\text{A}$ supply current. See the *Typical Application Circuits* for example application circuits using an external AGC DAC.

DC Offset Correction

For optimum IP2 and lowest DC offset at the baseband outputs, a 3-pole Butterworth highpass filter is implemented on-chip. In normal operation, this highpass corner is set to 8.6kHz. The corner frequency is chosen to optimize DC settling time when the system is faced with large DC transients due to an LNA gain step or a large AGC change between receive bursts.

An additional adaptive DC-cancellation mode has been implemented, which is activated for any of the following events: IC is enabled with IDLE, IC is enabled with SHDN, an LNA gain step (through logic pin or register setting), or a mixer gain step (through logic pin or register setting). This adaptive DC correction loop further minimizes DC settling time for cases where large DC errors are introduced. For further flexibility, the SPI interface can be used to sequence the DC cancellation loop through different time constants (see Table 3).

Baseband I/Q Interface

The baseband I and Q differential outputs are designed for a $150\text{mV}_{\text{RMS}}$ W-CDMA combined signal plus noise. The 8dB peak-to-average ratio of the forward W-CDMA channel brings the typical voltage at the baseband outputs to $1.0\text{V}_{\text{P-P}}$. The baseband amplifiers' outputs are DC-coupled, and offer a programmable common-mode voltage to address the requirements of different baseband processors' ADCs. The output common-mode voltage is 1.2V with OPCTRL.VCM = 0, and 1.4V for VCM = 1 (see Table 2 for the OPCTRL register definitions).

These outputs are designed for a minimum load of $10k\Omega$ (differential) in parallel with 5pF.

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

Synthesizer and LO Generation

The MAX2390-MAX2393, MAX2401 incorporate an integer-N synthesizer on-chip, including the VCO, tank, all dividers, phase comparator, etc. Only a TCXO and a loop filter are required as external components. The LO leakage at the LNA input is minimized by running the VCO at 2x the desired LO frequency. The typical application uses a comparison frequency of 200kHz—the channel raster for 3GPP-FDD and -TDD systems.

There are no special requirements for the synthesizer loop filter. The EV kits use a classic Type-II loop filter, with a bandwidth of about 20kHz. This ensures a 200μs settling time for a 60MHz frequency jump.

Use a 1nF DC-blocking capacitor in series with the reference oscillator input so as not to disturb the DC bias.

The MAX2396/MAX2400 integrate the VCO and the divide-by-2 for the LO generation, but do not include the synthesizer. The LO leakage at the LNA input is minimized by running the VCO at twice the desired RF frequency. The VCO signal is made available to the external PLL through an on-chip divide-by-three prescaler. Since $f_{VCO_OUTPUT} = f_{VCO} / 3$, and $f_{RFLO} = f_{VCO} / 2$, then $f_{VCO_OUTPUT} = (2/3)f_{RFLO}$. That is, when the RFLO of the MAX2400 is running at midband (1960MHz), the VCO output and the synthesizer are running at 1306.67MHz.

Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

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