



CLP270M

Application Specific Discretes
A.S.D.

OVERVOLTAGE AND OVERCURRENT PROTECTION FOR TELECOM LINE

MAIN APPLICATIONS

Any telecom equipment submitted to transient overvoltages and lightning strikes such as :

- Analog and ISDN line cards
- PABX
- Main Distribution Frames
- Primary protection modules

DESCRIPTION

The CLP270M is designed to protect telecommunication equipment. It provides both a transient overvoltage protection and an overcurrent protection.
It is housed in a PowerSO-10™ package.

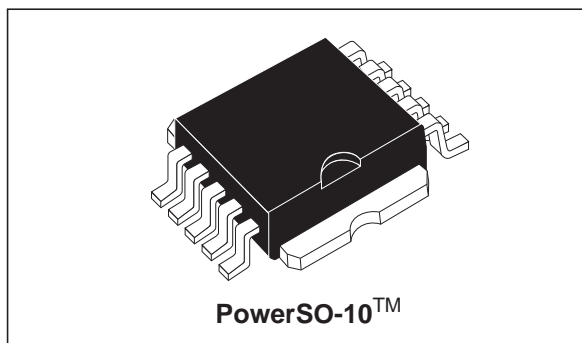
FEATURES

- DUAL BIDIRECTIONAL PROTECTION DEVICE.
- HIGH PEAK PULSE CURRENT :
I_{pp} = 100A (10/1000 μs SURGE)
I_{pp} = 500A (2/10 μs SURGE)
- MAX. VOLTAGE AT SWITCHING-ON : 380V
- MIN. CURRENT AT SWITCHING-OFF : 150mA
- FAILURE STATUS OUTPUT PIN

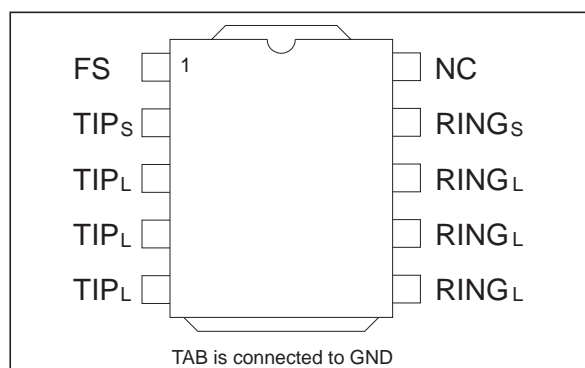
BENEFITS

- Both primary and secondary protection levels in one device.
- Voltage and current controlled suppression.
- Surface Mounting with PowerSO-10™ package.
- Line card cost reduction thanks to the very low power rating of external components required : balanced resistors, ring relay, low voltage SLIC protection.

PRELIMINARY DATASHEET



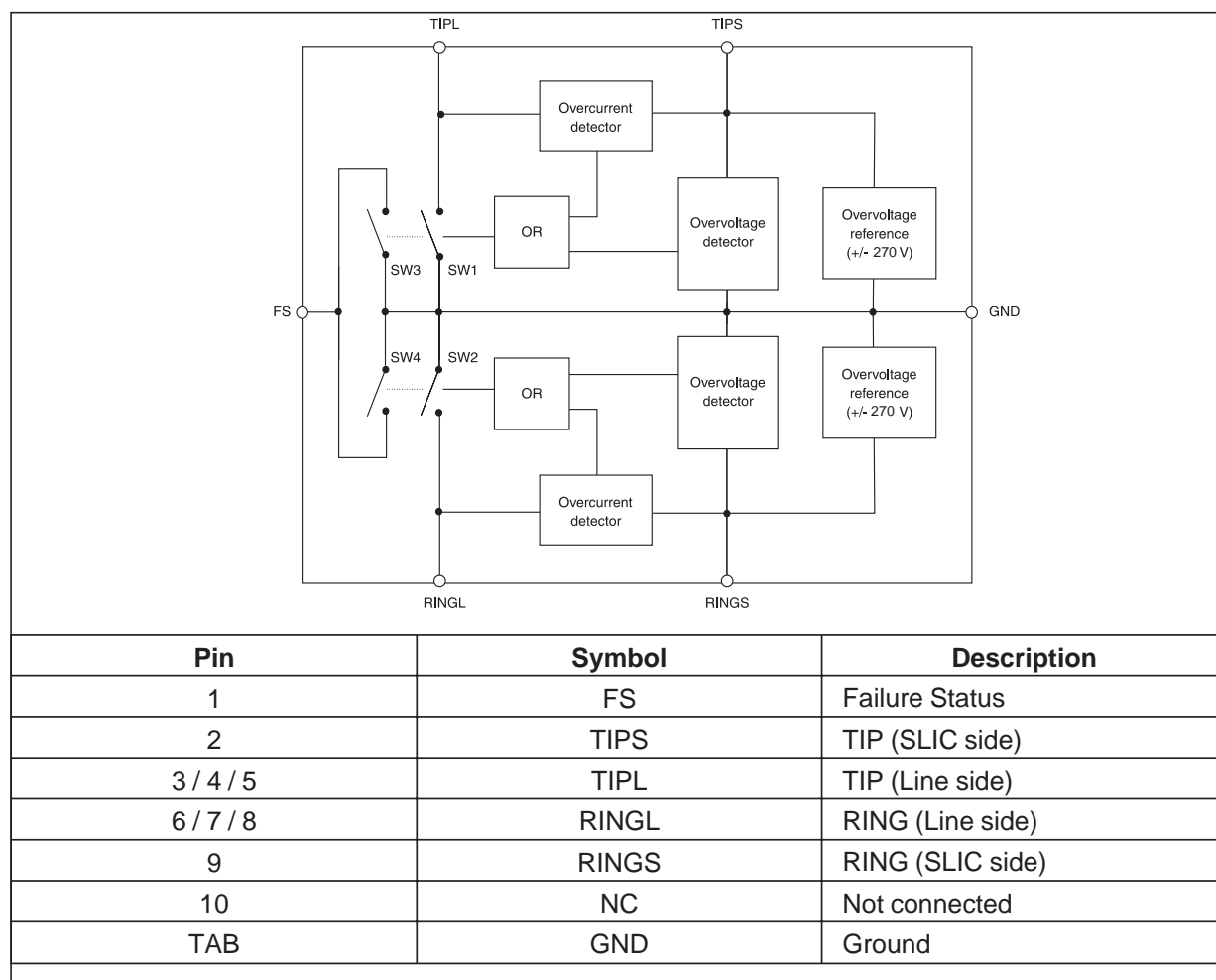
SCHEMATIC DIAGRAM



CLP270M

COMPLIES WITH THE FOLLOWING STANDARDS:	Peak Surge Voltage (V)	Voltage Waveform (μ s)	Current Waveform (μ s)	Admissible I_{pp} (A)	Necessary Resistor (Ω)
ITU K20	6000	10/700	5/310	150	-
VDE0433	6000	10/700	5/310	150	-
VDE0878	4000	1.2/50	1/20	100	-
IEC61000-4-5	6000	10/700	5/310	150	-
	4000	1.2/50	8/20	100	-
FCC Part 68, lightning surge type A	1500	10/160	10/160	200	-
	800	10/560	10/560	100	-
FCC Part 68, lightning surge type B	100	9/720	5/320	25	-
BELLCORE TR-NWT-001089 First level	2500	2/10	2/10	500	-
	1000	10/1000	10/1000	100	-
BELLCORE TR-NWT-001089 Second level	5000	2/10	2/10	500	-
CNET I31-24	4000	0.5/700	0.8/310	100	-

BLOCK DIAGRAM

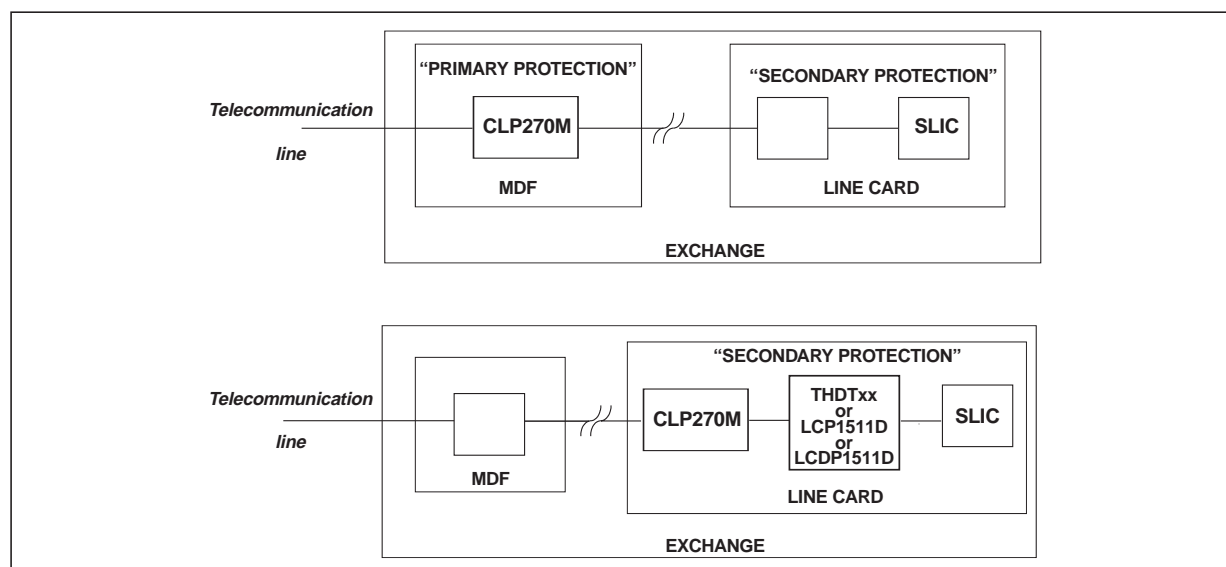


APPLICATION NOTE

1. INTRODUCTION

This device includes a primary protection level and is suitable for main distribution frames and line cards. This protection concept is explained and, in addition, the CLP270M performances are analysed when

Fig. 1: Subscriber line protection topology



facing different surges as described in the BELLCORE GR 1089 recommendations.

Figure 1 is a simplified block diagram of a subscriber line protection that is commonly used.

This shows two different topologies :

- A “primary protection” located on the Main Distribution Frame (MDF) eliminates coarsely the high energy environmental disturbances (lightning transients and AC power mains disturbances)
- A “secondary protection” located on the line card includes a primary protection level (first stage) and a residual protection (second stage) which eliminates finely the remaining transients that have not been totally suppressed by the first stage.

2. STMicroelectronics CLP270M CONCEPT

2.1. Evolution of the SLIC protection

Over the years, the silicon protection performances have considerably changed.

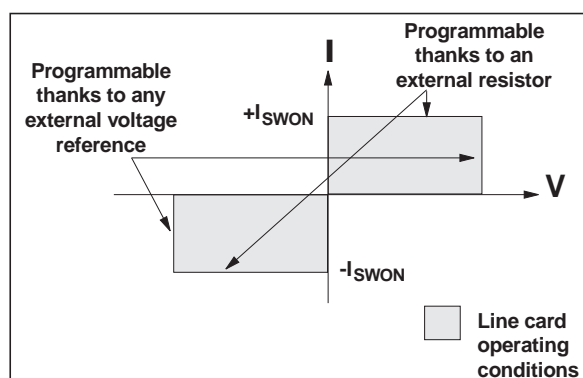
The first generation of products like SMTHBTxx and SMTHDTxx offered fixed overvoltage protection against surges on either TIP or RING line in four packages.

The following generation like THBTxx and THDTxx still offered fixed overvoltage protection against surges on both TIP and RING lines in two packages.

The next step was the introduction of the LCP1511D which brought the advantage of full programmable voltage.

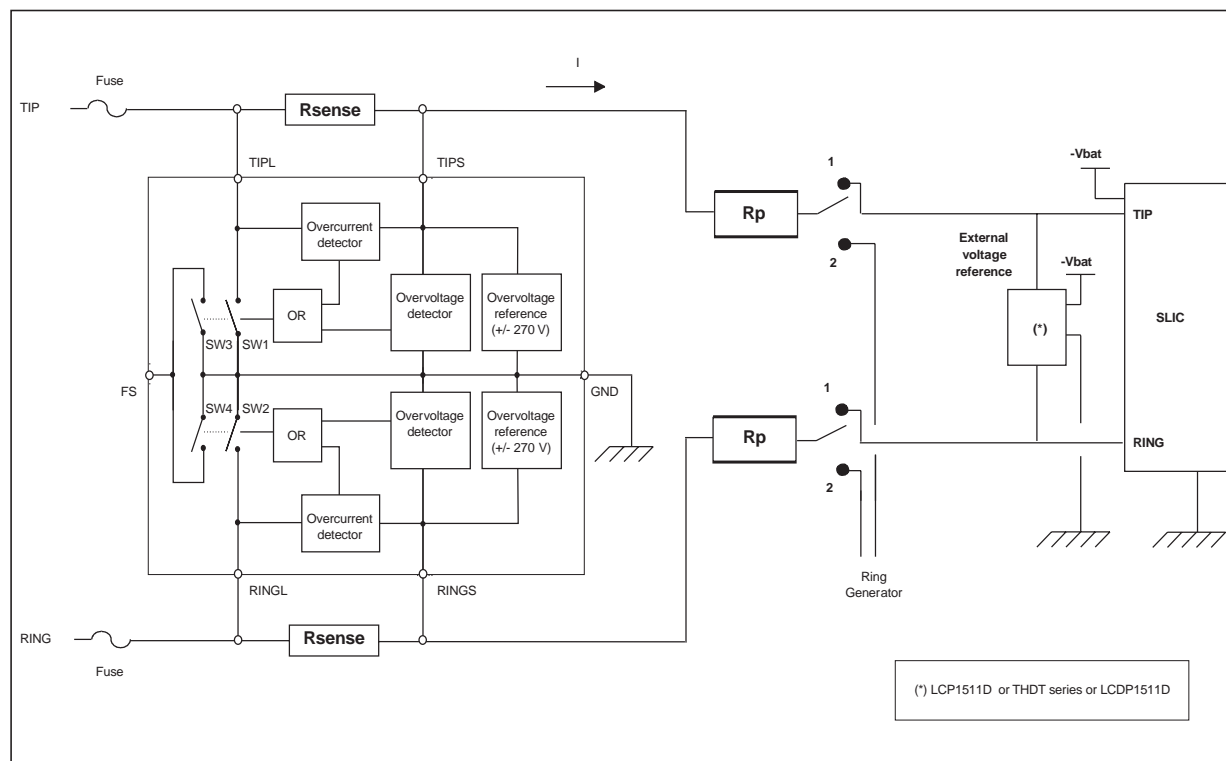
Today, the CLP270M combines the features of all the previous generations. In addition to that, it offers an overcurrent detection when operating in speech mode and also a Failure Status output signal.

Fig. 2: Line card protection



The figure 2 summarizes the firing modes of the CLP270M which basically hold the SLIC inside its correct

Fig. 3 : CLP270M in line card



voltage and current values.

2.2 Application circuit: CLP270M in line card.

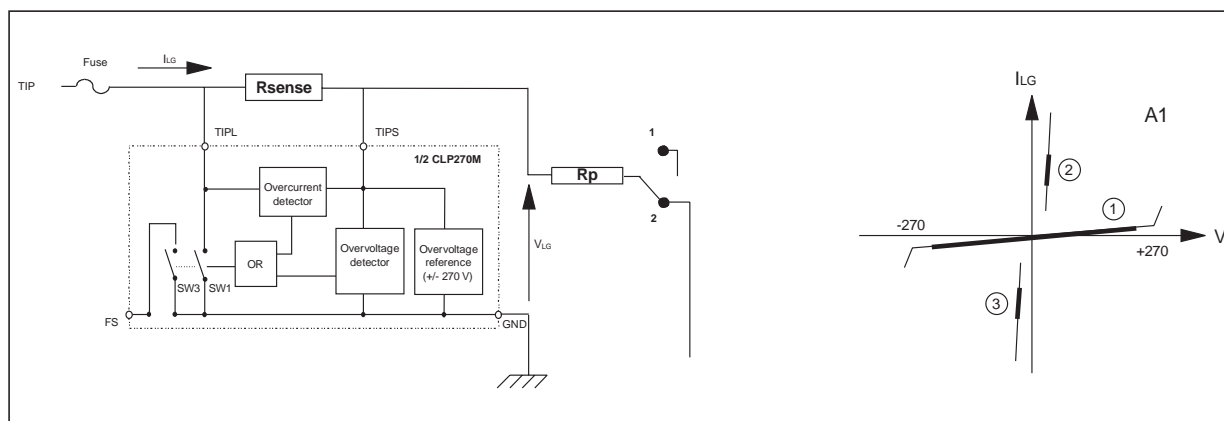
Figure 3 above shows the topology of a protected analog subscriber line at the exchange side. The CLP270M is connected to the ring relay via two balanced R_p resistors, and to the Subscriber Line Interface Circuit. A second device is located near the SLIC : it can be either a LCP1511D, a THDT series or a LCDP1511D.

These two devices are complementary and their functions are explained below :

- The first stage based on CLP270M manages the high power issued from the external surges. When used in ringing mode, the CLP270M operates in voltage mode and provides a symmetrical and bidirectional overvoltage protection at ± 270 V on both TIP and RING lines. When used in speech mode, the CLP270M operates in current mode and the activation current of the CLP270M is adjusted by R_{sense} .
- The second stage is the external voltage reference device which defines the firing threshold voltage during the speech mode and also assumes a residual power overvoltage suppression. This protection stage can be either a fixed or programmable breakover device. The THDTxx family acts as a fixed breakover device while the LCP1511D or the LCDP1511D operates as a programmable protection.

Thanks to this topology, the surge current in the line is reduced after the CLP270M. Because the remaining surge energy is low, the power ratings of R_p , the ring relay contacts and the external voltage reference circuit can be downsized. This results in a significant cost reduction.

Fig. 4: Switching by voltage during ringing mode.



2.3. Ringing mode

In ringing mode (Ring relay in position 2), the only protection device involved is the CLP270M.

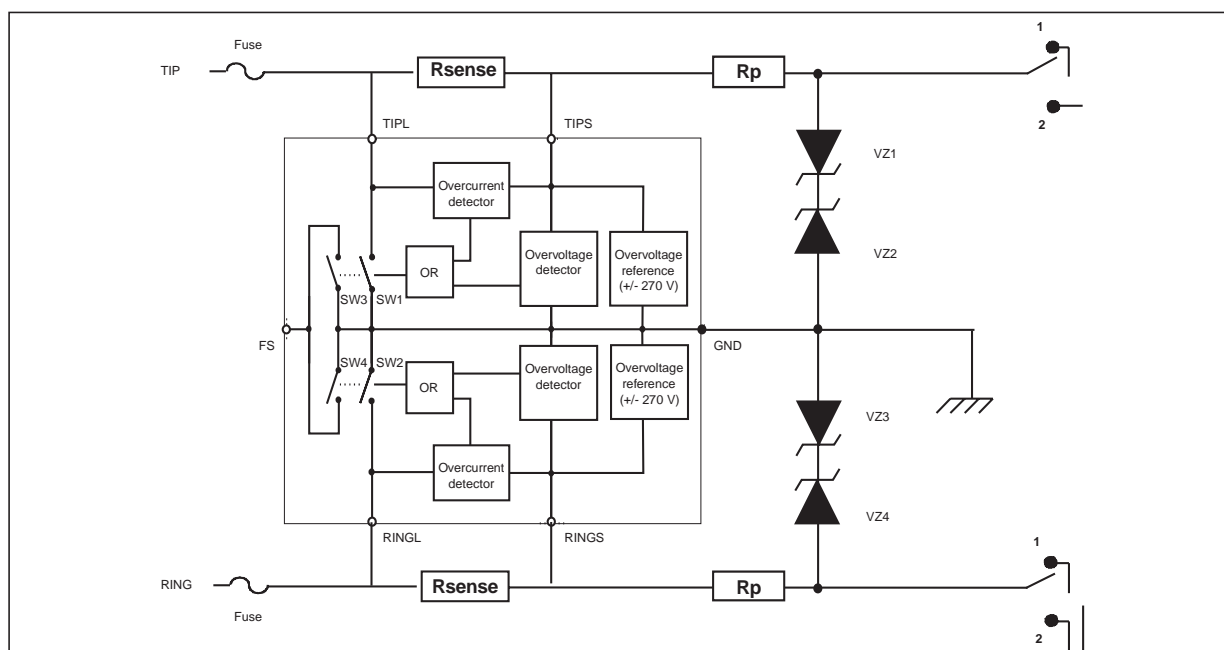
In normal conditions, the CLP270M operates in region 1 of **A1** curve, and is idle.

If an overvoltage occurring between TIP (or RING) and GND reaches the internal overvoltage reference (+/- 270 V), the CLP270M acts and the line is short-circuited to GND. At this time the operating point moves to region 2 for positive surges (region 3 for negative surges). Once the surge current falls below the switch off current $I_{S\text{W}\text{OFF}}$, the device returns to its initial state (region 1).

For surges occurring between TIP and RING, the CLP270M acts in the same way. This means that the CLP270M ensures a tripolar protection.

When used alone, the CLP270M acts at the internal overvoltage reference level (+/- 270 V). Furthermore, it is possible to adjust this threshold level to a lower voltage by using:

Fig. 5a: Method to adjust the reference voltage.



CLP270M

Fig. 5b: Method to adjust the reference voltage.

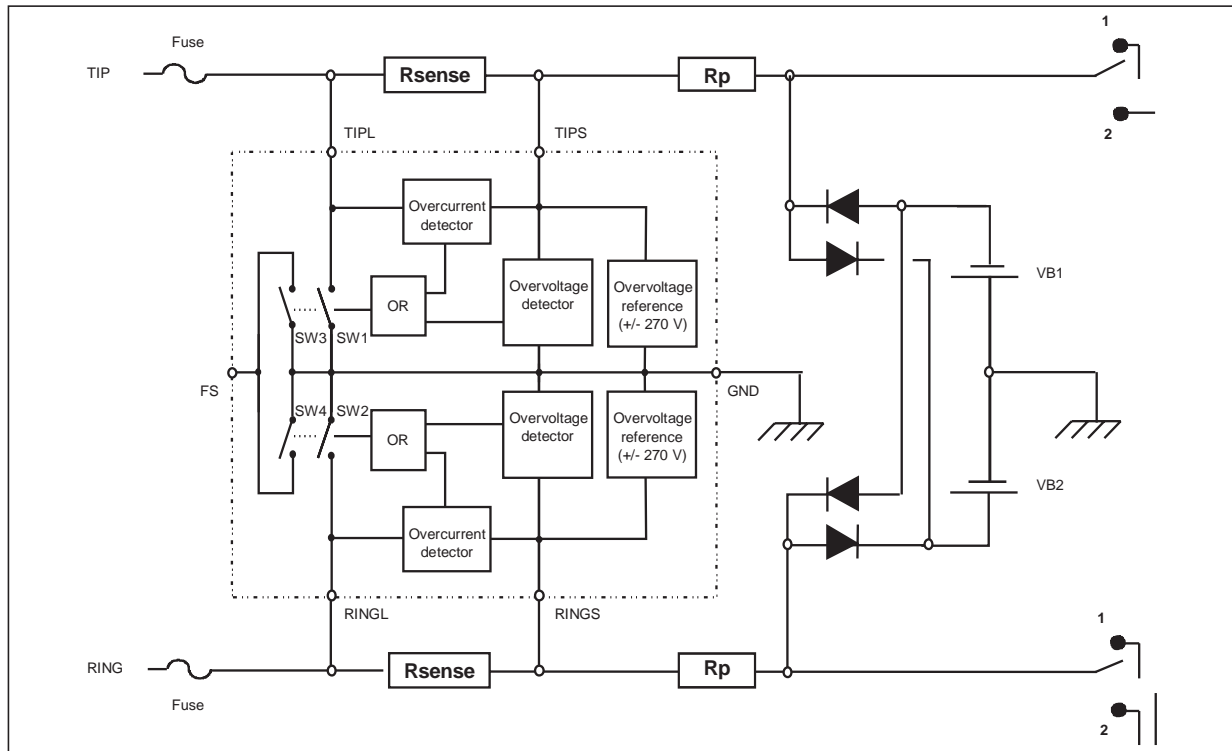
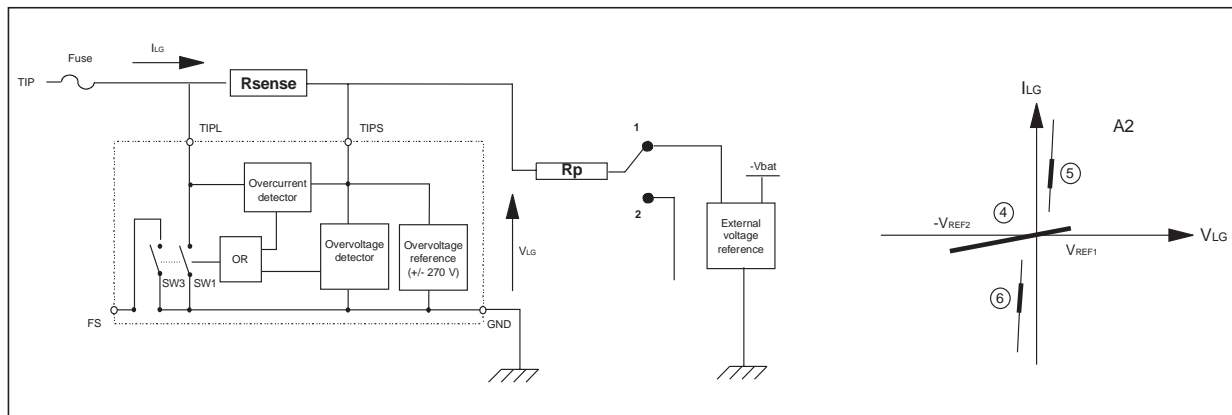


Fig. 6: Switching by current during speech mode.



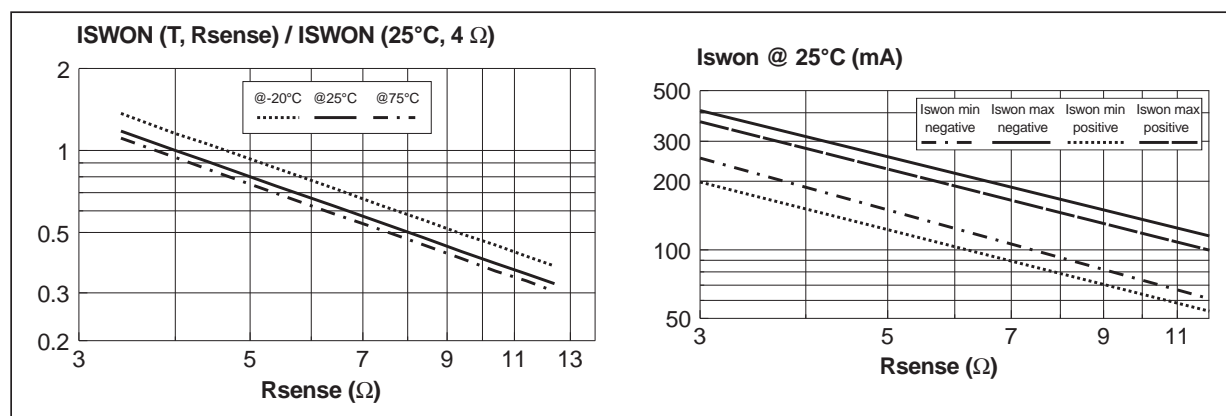
- up to 4 fixed external voltage reference (V_{Z1} to V_{Z4}) (see fig. 5a, here-below).
- external reference supplies, V_{b1} and V_{b2} (see fig. 5b, on next page).

2.4. Speech mode

In speech mode (Ring relay in position 1), the protection is provided by the combination of both CLP270M and the external voltage reference device.

In normal conditions, the working point of this circuit is located in region 4 of **A2** curve : the CLP270M is idle. When a surge occurs on the line, the external voltage reference device clamps at GND or $-V_{bat}$ respectively for positive and negative surges.

This generates a current which is detected by R_{sense} and causes the protection to act : the line is short-circuited to GND.

Fig. 7a and 7b: Switching-on current versus R_{sense} .

The operating point moves to region 5 for positive surges or region 6 for negative surges. Once the surge current falls below the switching-off current I_{SWOFF} , the CLP270M returns to its initial state (region 4).

The choice of the switching-on currents is function of the R_{sense} resistors.

In normal operating condition the current (typically below -100 mA) should not activate the protection device CLP270M. Therefore the level of activation is to be chosen just above this limit (-200 mA). This level is adjusted through R_{sense} .

Figures 7a and 7b enable the designers to choose the right R_{sense} value.

EXAMPLE :

The choice of $R_{sense} = 4 \Omega$ ensures a negative triggering of -190 mA min and -320 mA max. In this case, the positive triggering will be 150mA min and 280 mA max.

2.5. Failure Status

The CLP270M has an internal feature that allows the user to get a Failure Status (FS) indication. When the CLP270M is short-circuiting the line to GND, a signal can be managed through pin 1. This signal can be used to turn a LED on in order to provide a surge indication. It may also be used with a logic circuitry to

Fig. 8: Failure Status circuit and diagnostic.

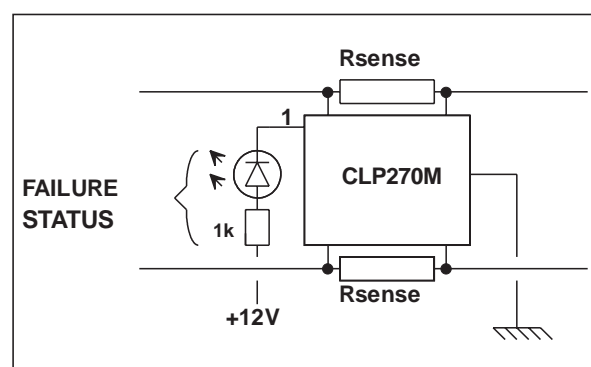
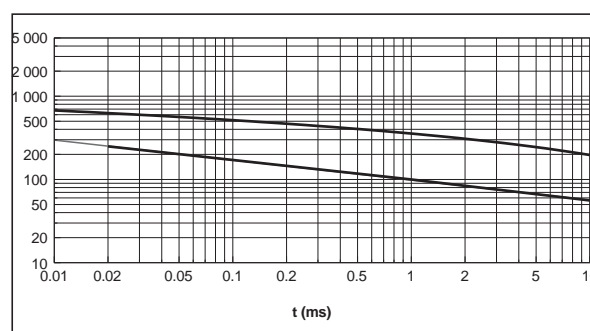


Fig. 9 : Operation limits and destruction zone of the CLP270M.



count the number of disturbances appearing on the lines.

If a surge exceeding the maximum ratings of the CLP270M occurs on the line, the device will fail in a short-circuit state.

CLP270M

The figure 9 shows two different curves :

- The lower one indicates the maximum guaranteed working limits of the CLP270M.

Table 1: First level lightning surge.

Surge	Minimum peak voltage (volts)	Minimum peak current per conductor (Amps)	Maximum rise / Minimum decay time for voltage and current (μs)	Repetitions, each polarity	Test connections per table 4.1
1	+/- 600	100	10/1000	25	A
2	+/- 1000	100	10/360	25	A
3	+/- 1000	100	10/1000	25	A
4	+/- 2500	500	2/10	10	B
5	+/- 1000	25	10/360	5	B

Table 2: Second level lightning surge.

Surge	Minimum peak voltage (volts)	Minimum peak current per conductor (Amps)	Maximum rise / Minimum decay time for voltage and current (μs)	Repetitions, each polarity	Test connections per table 4.1
1	+/- 5000	500	2/10	1	B

- The upper curve shows the limit above which the CLP270M is completely destructed . In this case, the Fail Diagnostic pin is on.

3. CLP270M TEST RESULTS ACCORDING TO BELLCORE 1089 REQUIREMENTS.

Table 3: First level AC power fault (table 4-7 of GR-1089-CORE issue 2, december 1997).

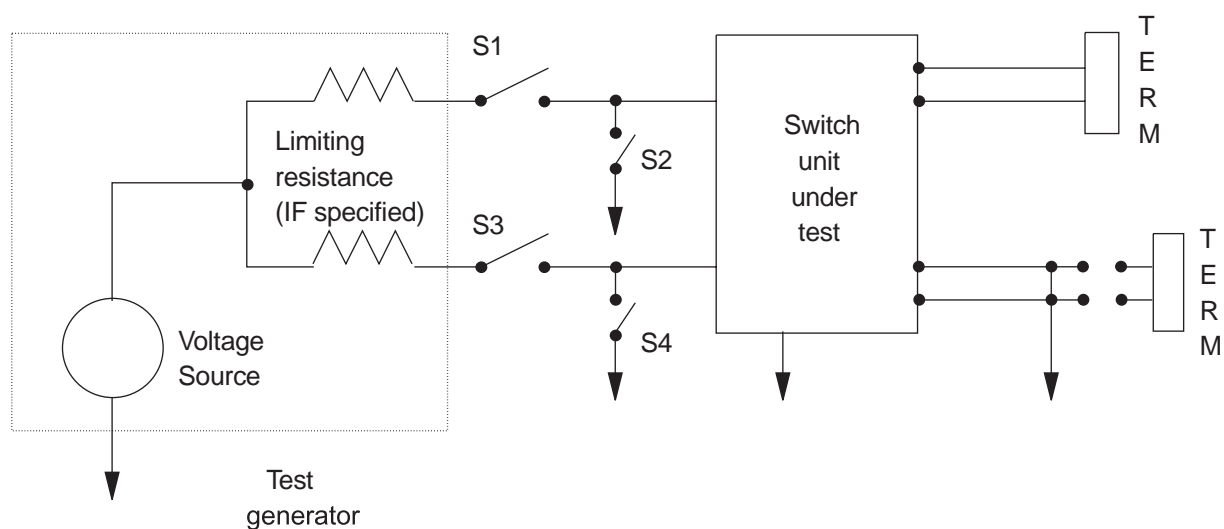
Test	Voltage (V _{RMS})	Short circuit current per conductor (Amps)	Duration	Primary protection	Test connections per table 4.1
1	50	0.33	15 minutes	Removed	A
2	100	0.17	15 minutes	Removed	A
3	200, 400 and 600	1 (at 600V)	60 1 s application of each voltage	Removed	A
4	1000	1	60 1s applications	Operative protector in place	B
5	see figure 4-3	see figure 4-3	60 5s applications	Removed	see figure 4-3
6	600	0.5	30s	Removed	A
7	600	2.2	2s	Removed	A
8	600	3	1s	Removed	A
9	1000	5	0.5s	Operative protector in place	B

Table 4: Second level AC power fault (table 4-8 of GR-1089-CORE issue 2, december 1997).

Test	Test for	Voltage (V _{RMS})	Short circuit current per conductor (Amps)	Duration	Test connections per table 4.1
1	Secondary contact	120, 277	25	15 minutes	A
2	Primary contact	600	60	5 seconds	A
3	Short-term fault induction	600	7	5 seconds	A
4	Long-term fault induction	100-600	2.2 (at 600 V)	15 minutes	A
5	High impedance induction			15 minutes	

Table 5: Test connection (table 4-1 of GR-1089-CORE).

Test	Two-wire interface	Four-wire interface
A	1. Tip to generator, Ring to ground	1. Each lead (T, R, T1, R1) to generator with other three leads grounded
	2. Ring to generator, Tip to ground	2. Tip and Ring to generator simultaneously, T1 and R1 to ground
	3. Tip to generator, Ring to generator simultaneously	3. T1 and R1 to generator simultaneously, Tip and Ring to ground
B	Tip to generator, Ring to generator simultaneously	T, R, T1, R1 to generator simultaneously

**Table 6:** Application of lightning and AC power fault test voltages (table 4-2 of GR-1089-CORE).

Test	S1	S2	S3	S4
T to generator, R to ground (condition A1 of table 4-1)	Closed	Open	Open	Closed
R to generator, T to ground (condition A2 of table 4-1)	Open	Closed	Closed	Open
T to generator, R to generator simultaneously (condition A3 of table 4-1)	Closed	Open	Closed	Open

3.1. BELLCORE GR-1089-CORE requirements:

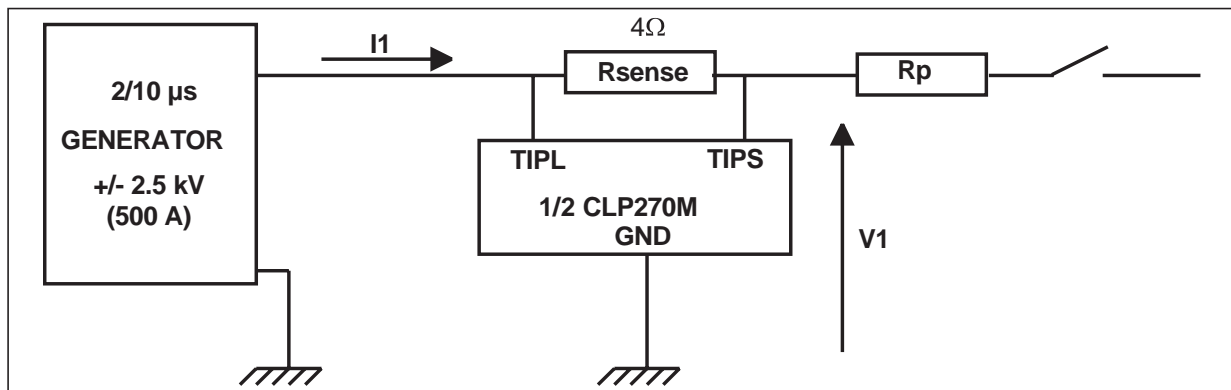
Tables 1 and 2 summarize the lightning surges required by the bellcore 1089.

Tables 1 to 6 summarize the surge needs defined by Bellcore regarding both lightning and AC power fault. In case of first level test, the equipment under test shall be operating after the surge. For the second level tests, the equipment under test may be damaged, but no fire or electrical safety hazard may occur.

3.2. First level lightning surge:

3.2.1. ringing mode

Fig. 10: Lightning simulation test.



Lightning phenomena are the most common surge causes. The purpose of this test is to check the behavior of the CLP270M against these lightning strikes.

Fig. 11: CLP270M response to a positive surge.

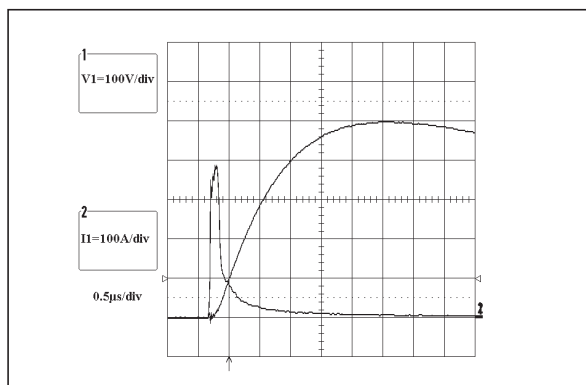
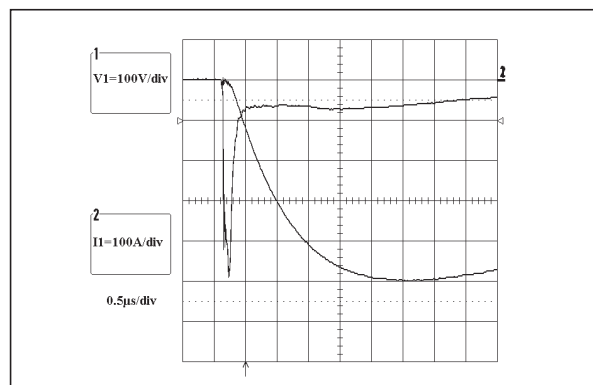


Fig. 12 : CLP270M response to a negative surge.



Figures 11 and 12 show that the remaining overvoltage does not exceed +/- 500 V. The CLP270M

Fig. 13: Lightning test in speech mode.

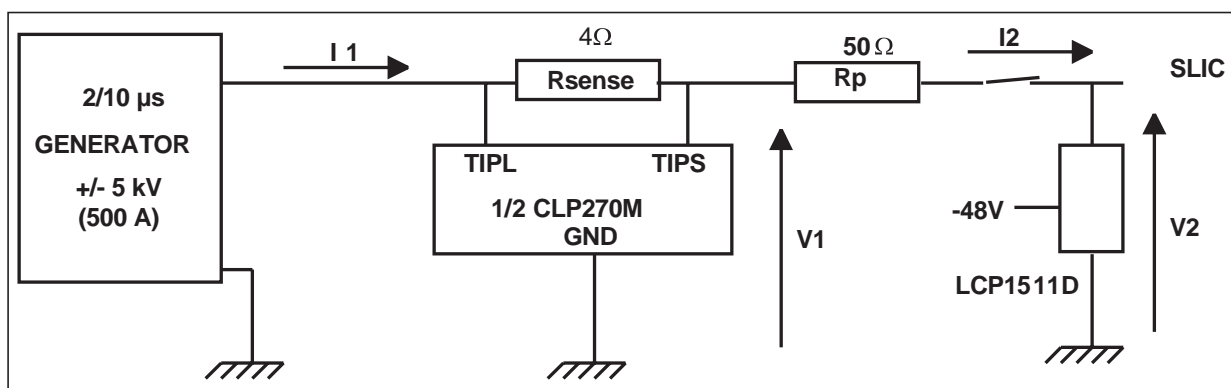
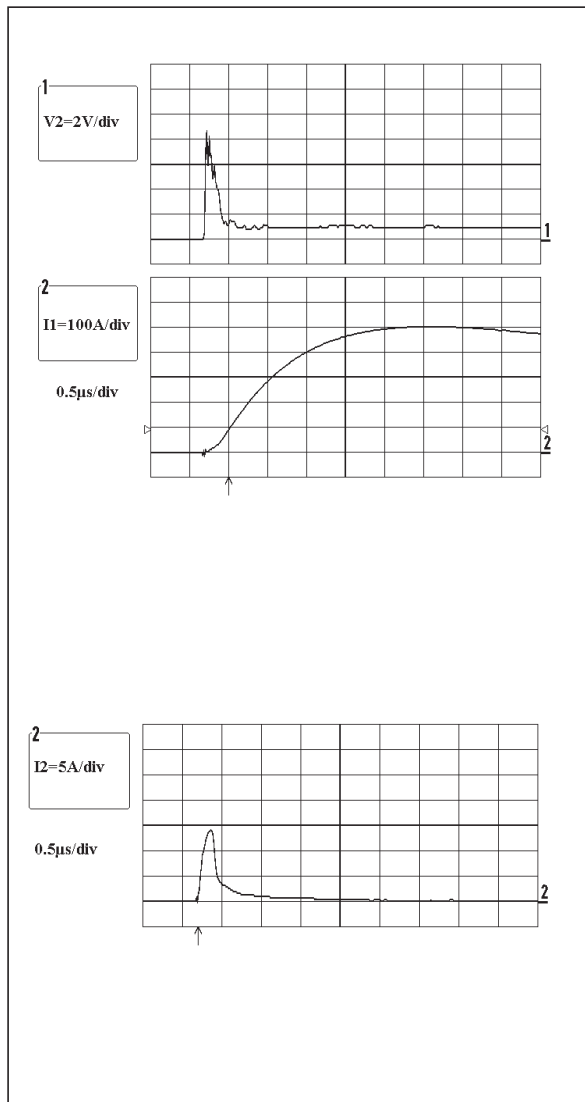
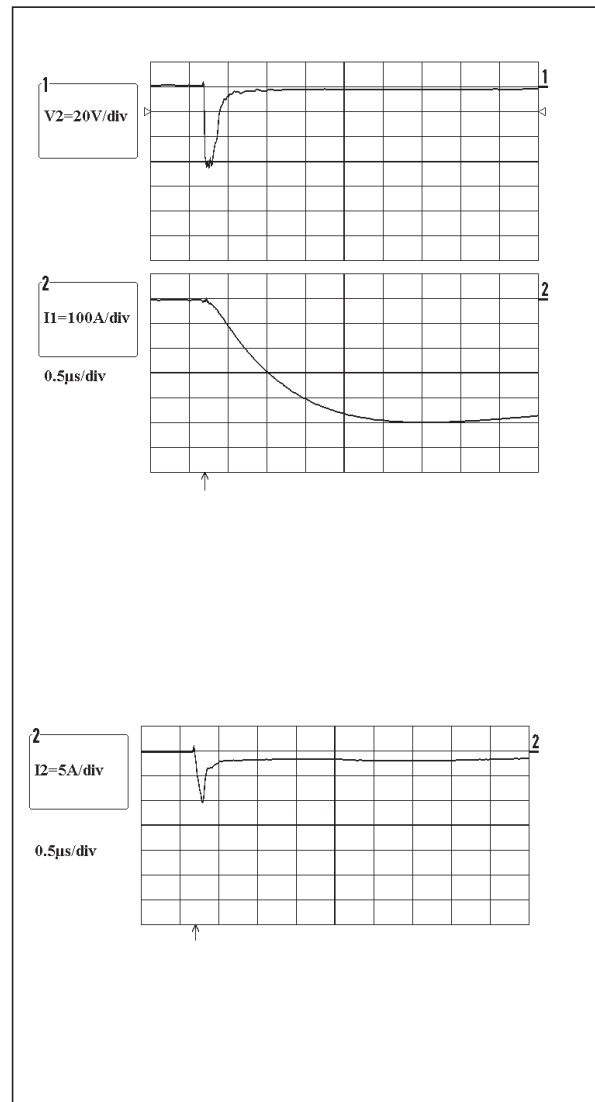


Fig. 14: CLP270M response to a positive surge.**Fig. 15:** CLP270M response to a negative surge.

switches on within 250ns and withstands the 500A given by the BELLCORE 2/10μs generator.

3.2.2. Speech mode

Figures 14 and 15 give the voltage and current behavior during positive and negative 2.5kV, 2/10μs, 500A surge tests using a LCP1511D as second stage protection device. The firing threshold values are now adjusted to GND and to -Vbat (-48V) by the action of the second stage protection which acts as an external voltage reference.

As shown on these figures, the maximum remaining voltage does not exceed +8.5V for positive surges and -65V for negative surges.

Fig. 16: Lightning test in Ringing mode.

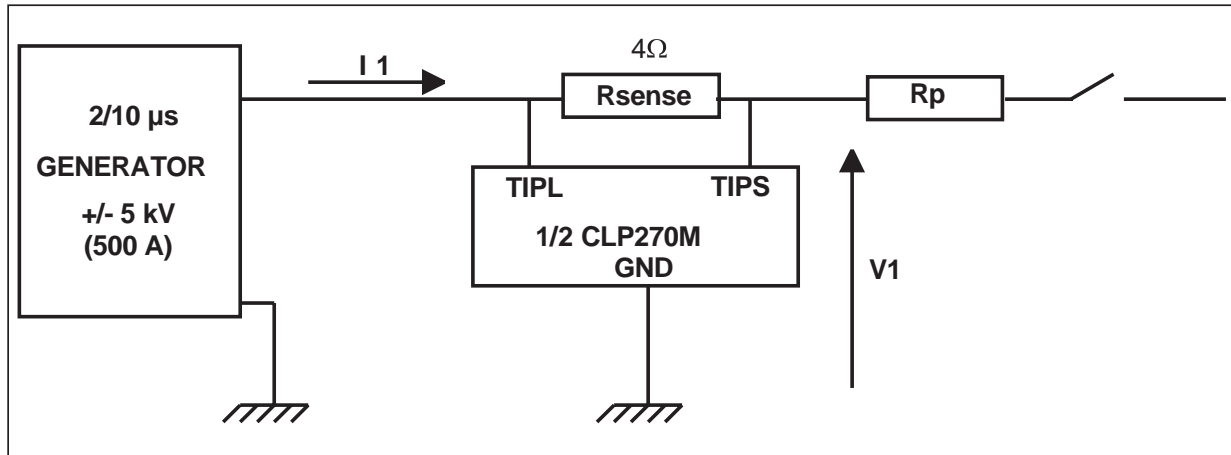


Fig. 17: CLP270M response to a positive surge.

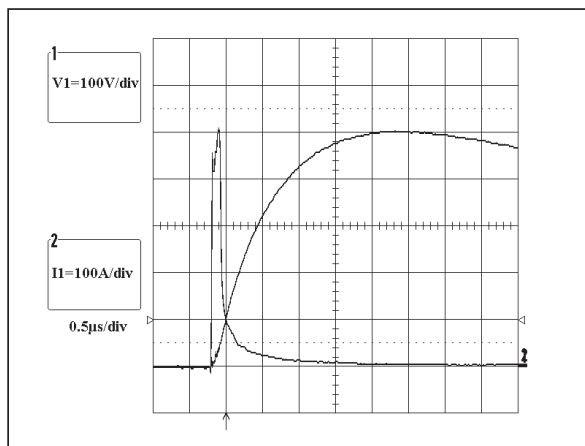
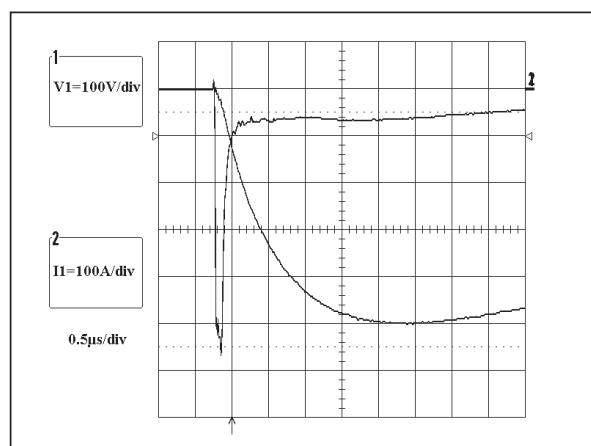


Fig. 18: CLP270M response to a negative surge.



3.3. Second level lightning surge

3.3.1. Lightning test in ringing mode

CLP270M

The figures 17 and 18 give the voltage and current behavior during positive and negative 5kV, 2/10 μ s,500A surge with the CLP270M acting in Ringing mode.

Fig. 19: Lightning test in Speech mode.

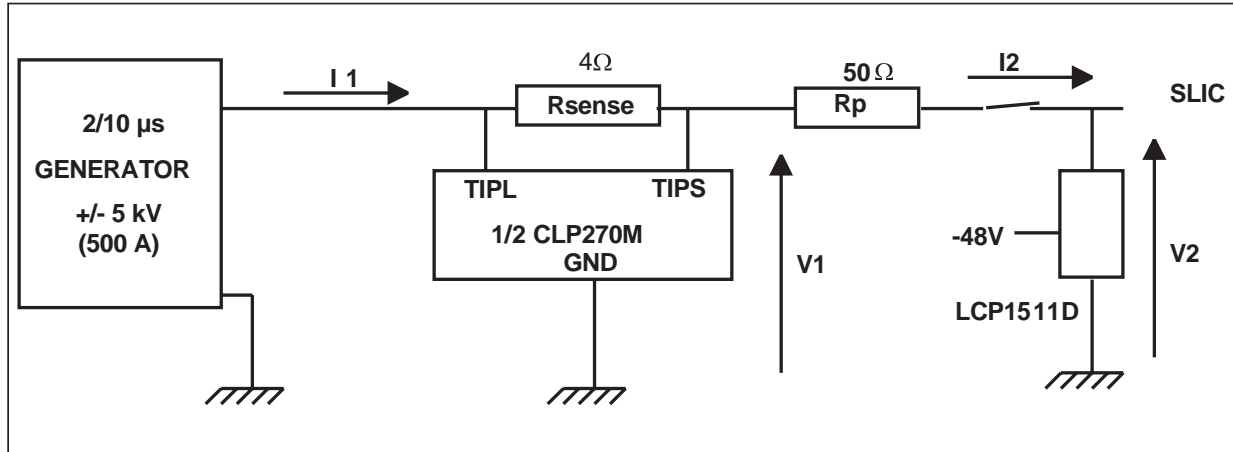


Fig. 20: CLP270M response to a positive surge.

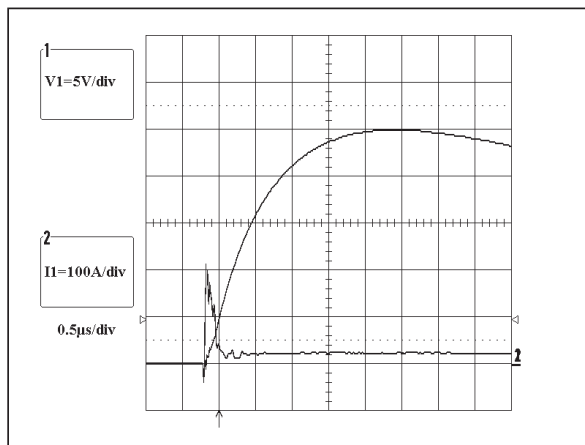
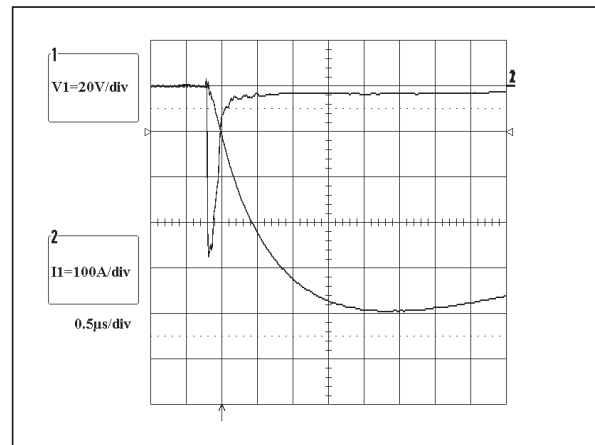


Fig. 21: CLP270M response to a negative surge.



3.3.2. Speech mode

The figures 20 and 22 give the voltage and current behavior during positive and negative 5kV, 2/10 μ s,500A surge with the CLP270M acting in speech mode.

The CLP270M withstands the second level lightning surge test without trouble.

3.4. FIRST AND SECOND LEVEL AC POWER FAULT

Fig. 22: AC power fault test in Ringing mode.

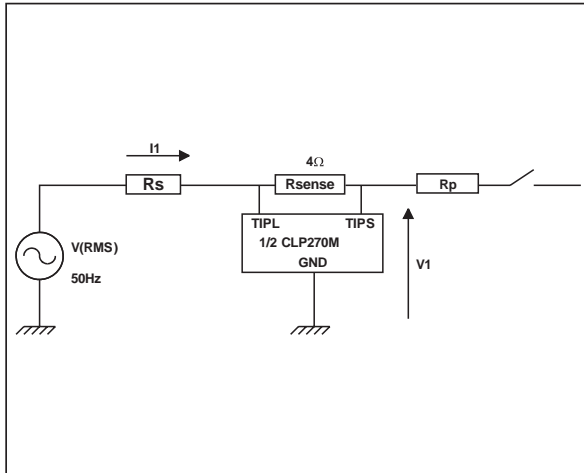


Fig. 23: Example of behavior when facing test 3 (400V, 600Ω).

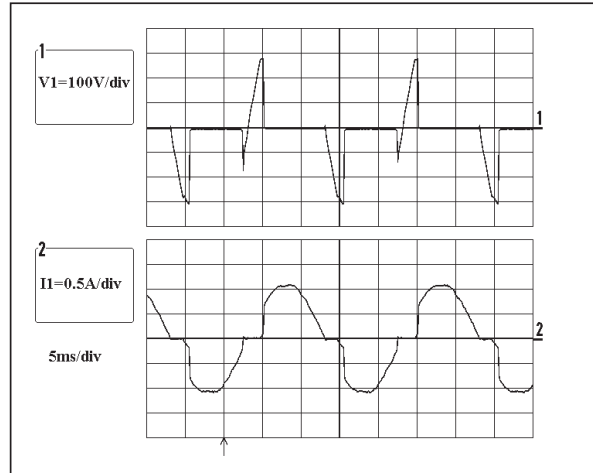


Fig. 24: AC power fault test in Speech mode.

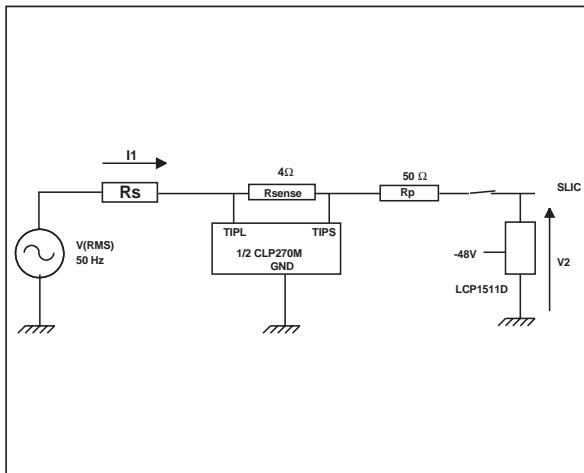
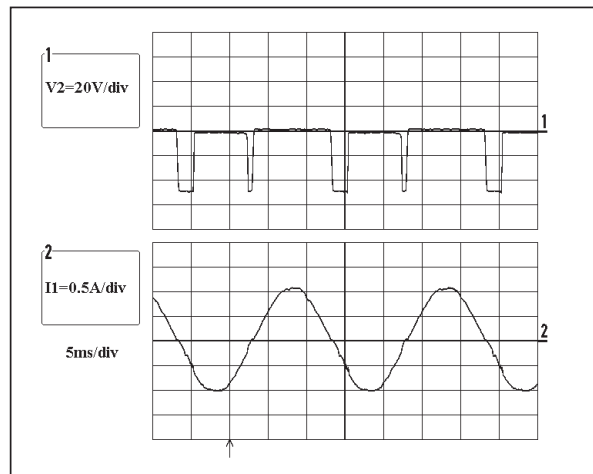


Fig. 25: Example of behavior when facing test 3 (400V, 600Ω).



3.4.1. Ringing mode

The figures 23 and 25 give the voltage and current at the CLP270M terminals in Ringing mode and Speech mode. The CLP270M is able to withstand all the first level AC power fault tests as required in the table 4-7 of GR-1089-CORE standard.

For the second level AC power fault tests serial protection as PTC or fuse are needed.

All these curves, lightning and AC power fault represent the behavior of the CLP270M in worst case tests, any how the CLP270M withstands all the others surges of the Bellcore GR1098 standard. For the second level AC power fault test, the use of series protection elements (PTC or fuses) are needed.

CLP270M**ABSOLUTE MAXIMUM RATINGS** ($R_{\text{SENSE}} = 4 \Omega$, and $T_{\text{amb}} = 25^\circ\text{C}$)

Symbol	Parameter	Test Conditions	Value	Unit
I_{PP}	Line to GND peak surge current	10/1000 μs (open circuit voltage wave shape 10/1000 μs)	100	A
		5/310 μs (open circuit voltage wave shape 10/700 μs)	150	
		2/10 μs (open circuit voltage wave shape)	500	
I_{TSM}	Non repetitive surge peak on-state current (TIP or RING versus Ground) F = 50 Hz	$t_p = 20 \text{ ms}$	60	A
		$t_p = 200 \text{ ms}$	30	A
		$t_p = 2 \text{ s}$	15	A
T_{stg} T_j	Storage temperature range Maximum junction temperature		- 40 to + 150 150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering during 10 s		260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($R_{\text{SENSE}} = 4 \Omega$, and $T_{\text{amb}} = 25^\circ\text{C}$)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{LGL}	Line to GND leakage current	. $V_{\text{LG}} = 240 \text{ V}$. Measured between TIP (or RING) and GND			10	μA
V_{ref}	Overvoltage internal reference	. $I_{\text{LG}} = 1 \text{ mA}$. Measured between TIP (or RING) and GND	265			V
V_{SWON}	Line to GND voltage at SW1 or SW2 switching-on	. Measured at 50 Hz between TIPL (or RINGL) and GND			400	V
I_{SWOFF}	Line to GND current at SW1 or SW2 switching-off (negative current)	. Refer to test circuit page 17	150			mA
I_{SWON}	Line current at SW1 or SW2 switching-on	. Positive pulse . Negative pulse	150 190		280 320	mA
C	RING to GND capacitance TIP to GND capacitance TIP to RING capacitance	. $V_{\text{RINGL}} = -1 \text{ V}$. $V_{\text{TIPL}} = -48 \text{ V}$. $V_{\text{GND}} = 0 \text{ V}$. F = 1 MHz $V_{\text{RMS}} = 1 \text{ V}$		180 62 57		pF

TEST CIRCUIT FOR I_{SWOFF} PARAMETER : GO-NO GO TEST

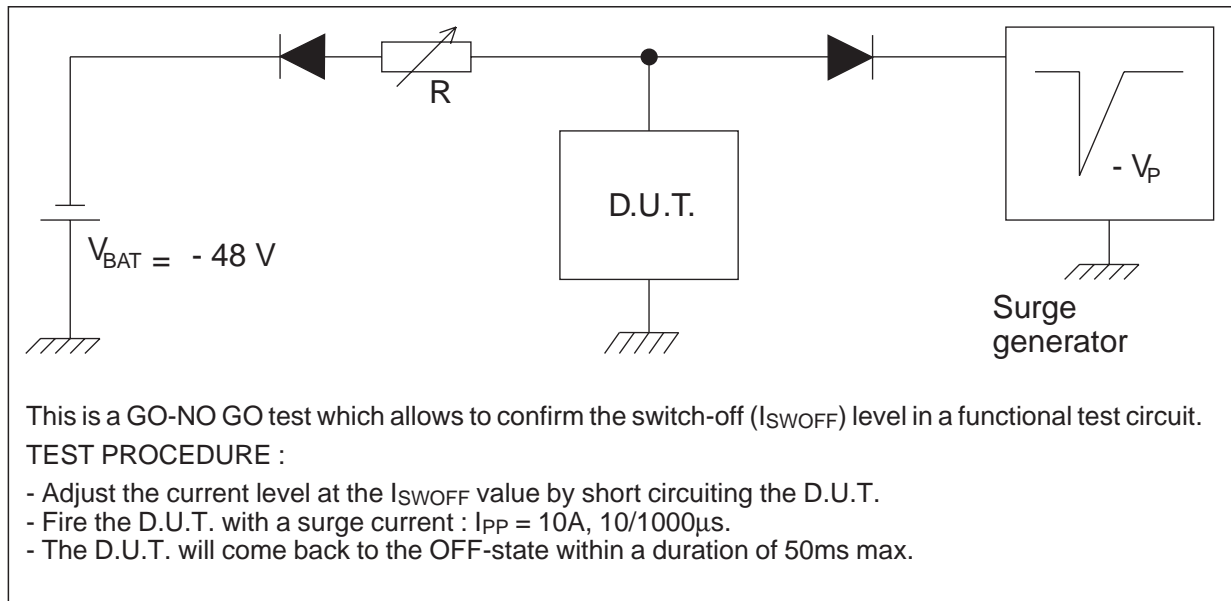


Fig. 26: Typical relative variation of switching-on current (positive or negative) versus R_{SENSE} resistor and junction temperature (see test condition Fig. 28).

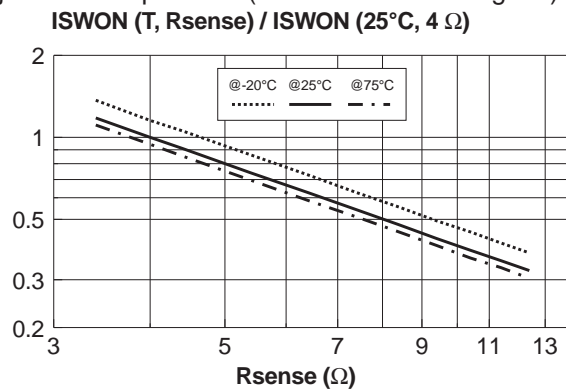


Fig. 28: I_{SWON} MEASUREMENT

- $I_{swon} = I_1$ when the CLP270M switches on (I_1 is progressively increased using R)
- Both TIP and RING sides of the CLP270M are checked
- $R_L = 10 \Omega$.

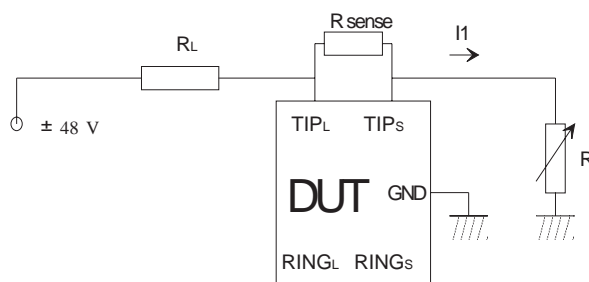


Fig. 27: Variation of switching-on current versus R_{SENSE} at $25^\circ C$.

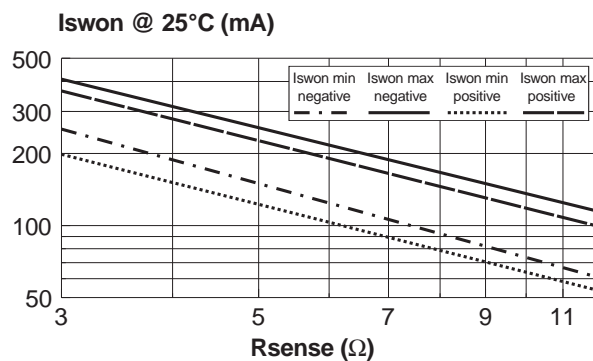
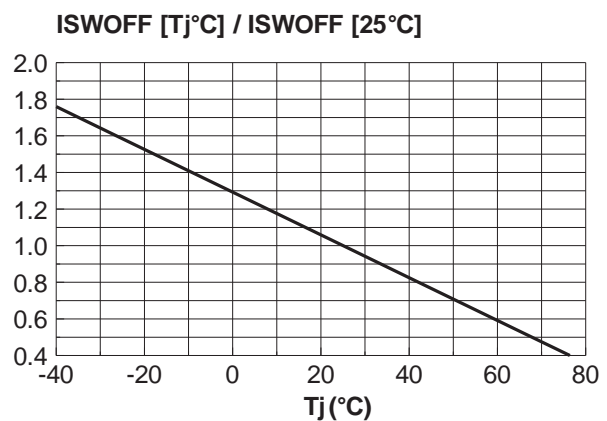


Fig. 29: Relative variation of switching-off current versus junction temperature for R_{SENSE} between 3 and 10Ω .



CLP270M

Fig. 30: Relative variation of switching-off current versus R_{SENSE} (between 3 and 10 Ω).

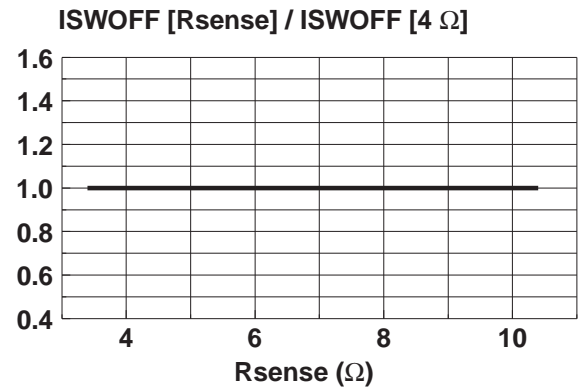


Fig. 31: Residual current I1 after the CLP270M. The residual current I1 is defined by its peak value (I_P) and its duration (τ) @ $I_P/2$ (see below circuit test).

Current surge input		Residual current after the CLP270M	
waveform(μs)	$I_{PP}(A)$	Peak current $I_P (A)$	waveform t(μs)
5/310	130A	4.2	1
	negative surge	1.1	0.5

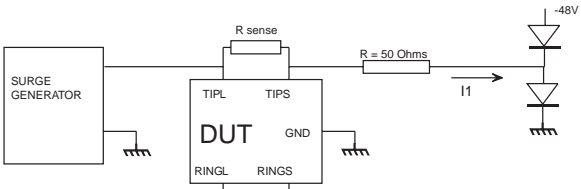


Fig. 32: Relative variation of switching-on voltage versus dV/dt with an external resistor of 4 Ω .

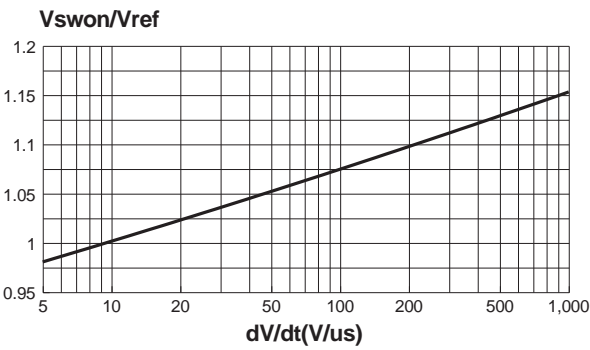


Fig. 33: Relative variation of internal reference voltage versus junction temperature ($I_{LG}=1mA$).

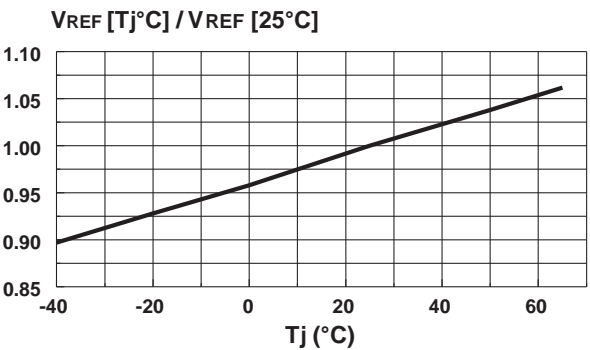


Fig. 34: Typical junction capacitance (TIPL/GND) versus applied voltage.

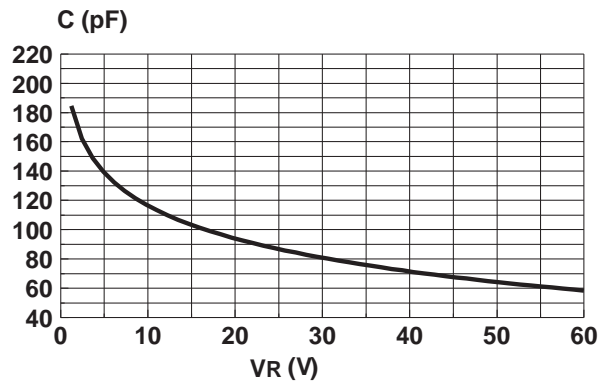
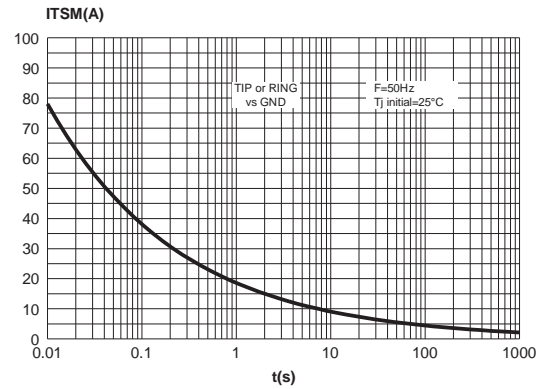


Fig. 35: Maximum non repetitive surge RMS on state current versus overload duration .



SOLDERING RECOMMENDATION

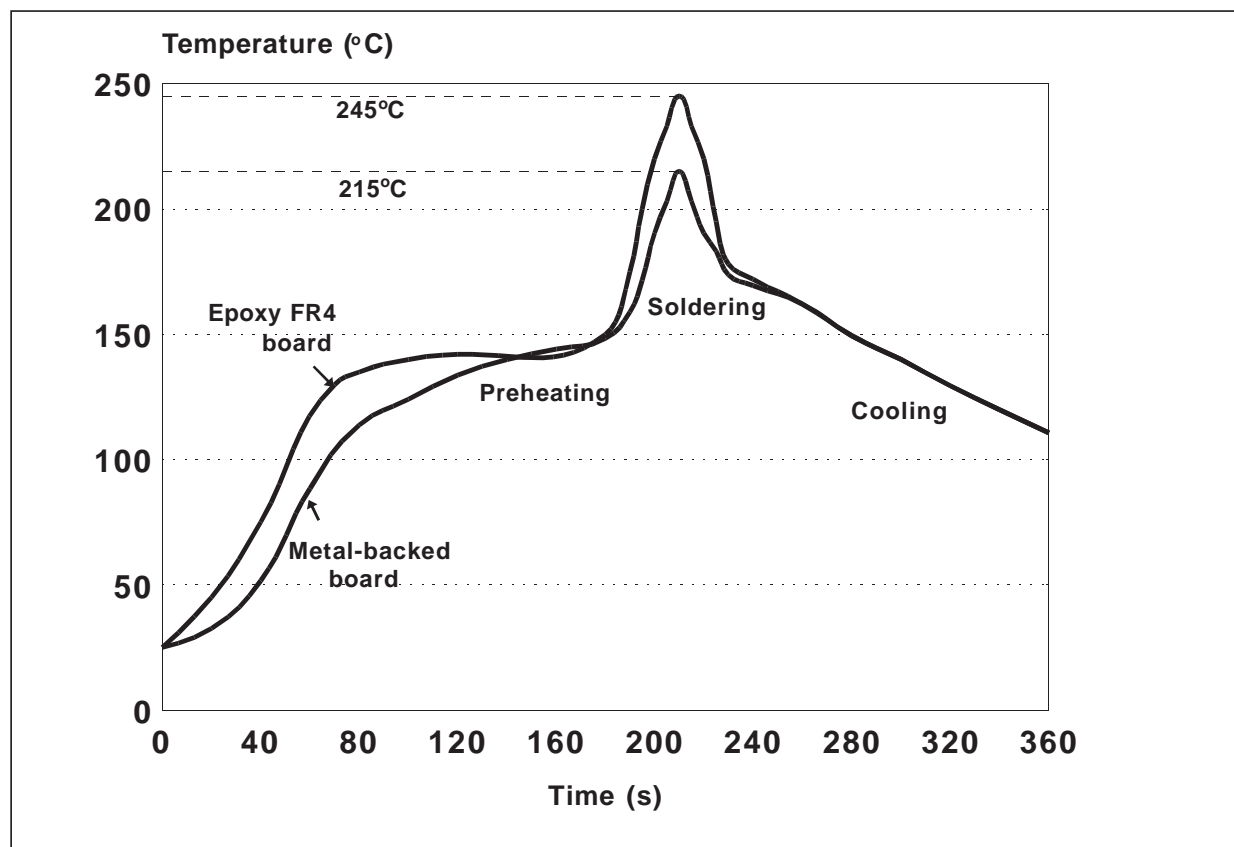
The soldering process causes considerable thermal stress to a semiconductor component. This has to be minimized to assure a reliable and extended lifetime of the device. The PowerSO-10™ package can be exposed to a maximum temperature of 260°C for 10 seconds. However a proper soldering of the package could be done at 215°C for 3 seconds. Any solder temperature profile should be within these limits. As reflow techniques are most common in surface mounting, typical heating profiles are given in Figure 36, either for mounting on FR4 or on metal-backed boards. For each particular board, the appropriate heat profile has to be adjusted experimentally. The present proposal is just a starting point. In any case, the following precautions have to be considered :

- always preheat the device
- peak temperature should be at least 30 °C higher than the melting point of the solder alloy chosen
- thermal capacity of the base substrate

Voids pose a difficult reliability problem for large surface mount devices. Such voids under the package result in poor thermal contact and the high thermal resistance leads to component failures. The PowerSO-10 is designed from scratch to be solely a surface mount package, hence symmetry in the x- and y-axis gives the package excellent weight balance. Moreover, the PowerSO-10 offers the unique possibility to control easily the flatness and quality of the soldering process. Both the top and the bottom soldered edges of the package are accessible for visual inspection (soldering meniscus).

Coplanarity between the substrate and the package can be easily verified. The quality of the solder joints is very important for two reasons : (I) poor quality solder joints result directly in poor reliability and (II) solder thickness affects the thermal resistance significantly. Thus a tight control of this parameter results in thermally efficient and reliable solder joints.

Fig 36 : Typical reflow soldering heat profile



SUBSTRATES AND MOUNTING INFORMATION

The use of epoxy FR4 boards is quite common for surface mounting techniques, however, their poor thermal conduction compromises the otherwise outstanding thermal performance of the PowerSO-10. Some methods to overcome this limitation are discussed below.

One possibility to improve the thermal conduction is the use of large heat spreader areas at the copper layer of the PC board. This leads to a reduction of thermal resistance to 35 °C for 6 cm² of the board heatsink (see fig. 37).

Use of copper-filled through holes on conventional FR4 techniques will increase the metallization and

decrease thermal resistance accordingly. Using a configuration with 16 holes under the spreader of the package with a pitch of 1.8 mm and a diameter of 0.7 mm, the thermal resistance (junction - heatsink) can be reduced to 12°C/W (see fig. 38). Beside the thermal advantage, this solution allows multi-layer boards to be used. However, a drawback of this traditional material prevent its use in very high power, high current circuits. For instance, it is not advisable to surface mount devices with currents greater than 10 A on FR4 boards. A Power Mosfet or Schottky diode in a surface mount power package can handle up to around 50 A if better substrates are used.

Fig 37 : Mounting on epoxy FR4 head dissipation by extending the area of the copper layer

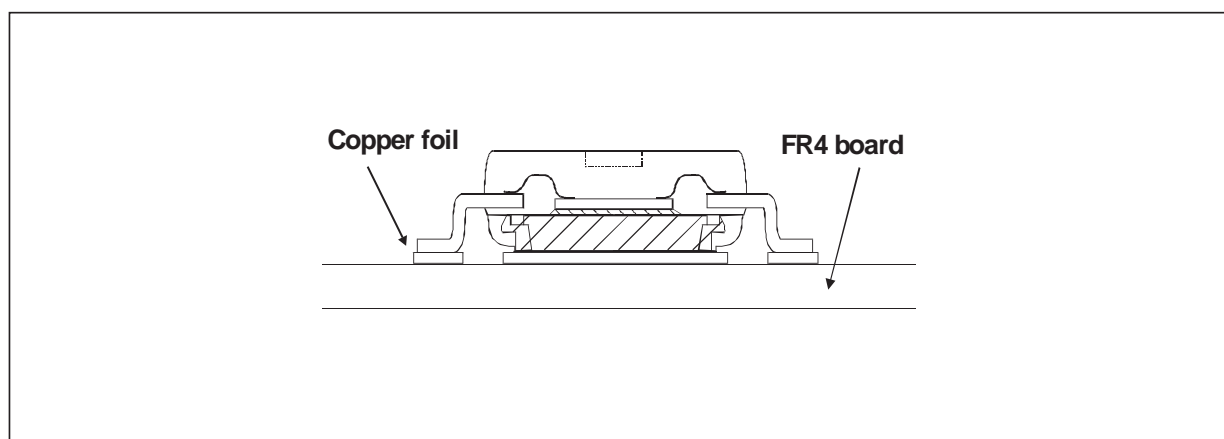
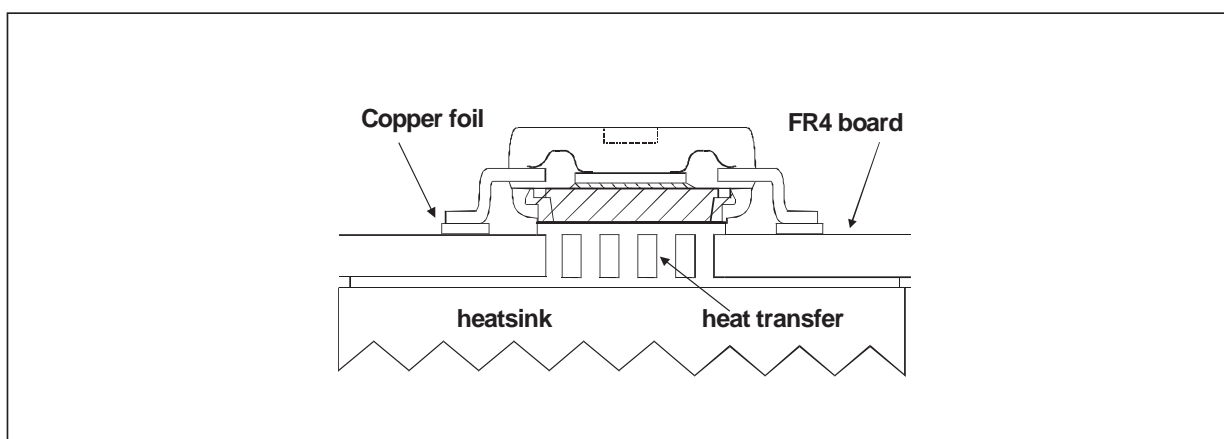
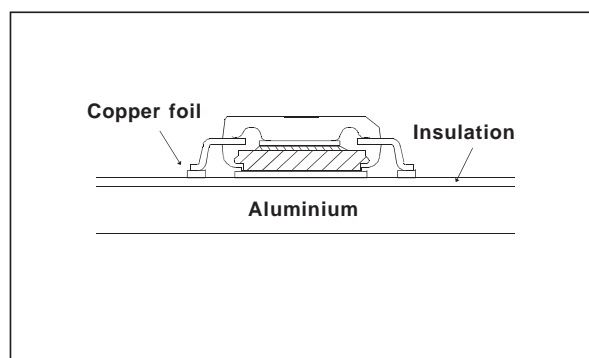


Fig 38 : Mounting on epoxy FR4 by using copper-filled through holes for heat transfer



A new technology available today is IMS - an Insulated Metallic Substrate. This offers greatly enhanced thermal characteristics for surface mount components. IMS is a substrate consisting of three different layers, (I) the base material which is available as an aluminium or a copper plate, (II) a thermal conductive dielectrical layer and (III) a copper foil, which can be etched as a circuit layer. Using this material a thermal resistance of 8°C/W with 40 cm^2 of board floating in air is achievable (see fig. 39). If even higher power is to be

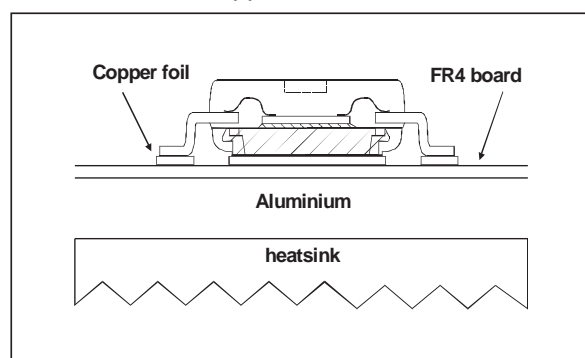
Fig 39 : Mounting on metal backed board



The PowerSO-10 concept also represents an attractive alternative to C.O.B. techniques. PowerSO-10 offers devices fully tested at low and high temperature. Mounting is simple - only conventional SMT is required - enabling the users to get rid of bond wire problems and the problem to

dissipated an external heatsink could be applied which leads to an $R_{th(j-a)}$ of 3.5°C/W (see Fig. 40), assuming that R_{th} (heatsink-air) is equal to R_{th} (junction-heatsink). This is commonly applied in practice, leading to reasonable heatsink dimensions. Often power devices are defined by considering the maximum junction temperature of the device. In practice, however, this is far from being exploited. A summary of various power management capabilities is made in table 1 based on a reasonable ΔT of 70°C junction to air.

Fig 40 : Mounting on metal backed board with an external heatsink applied



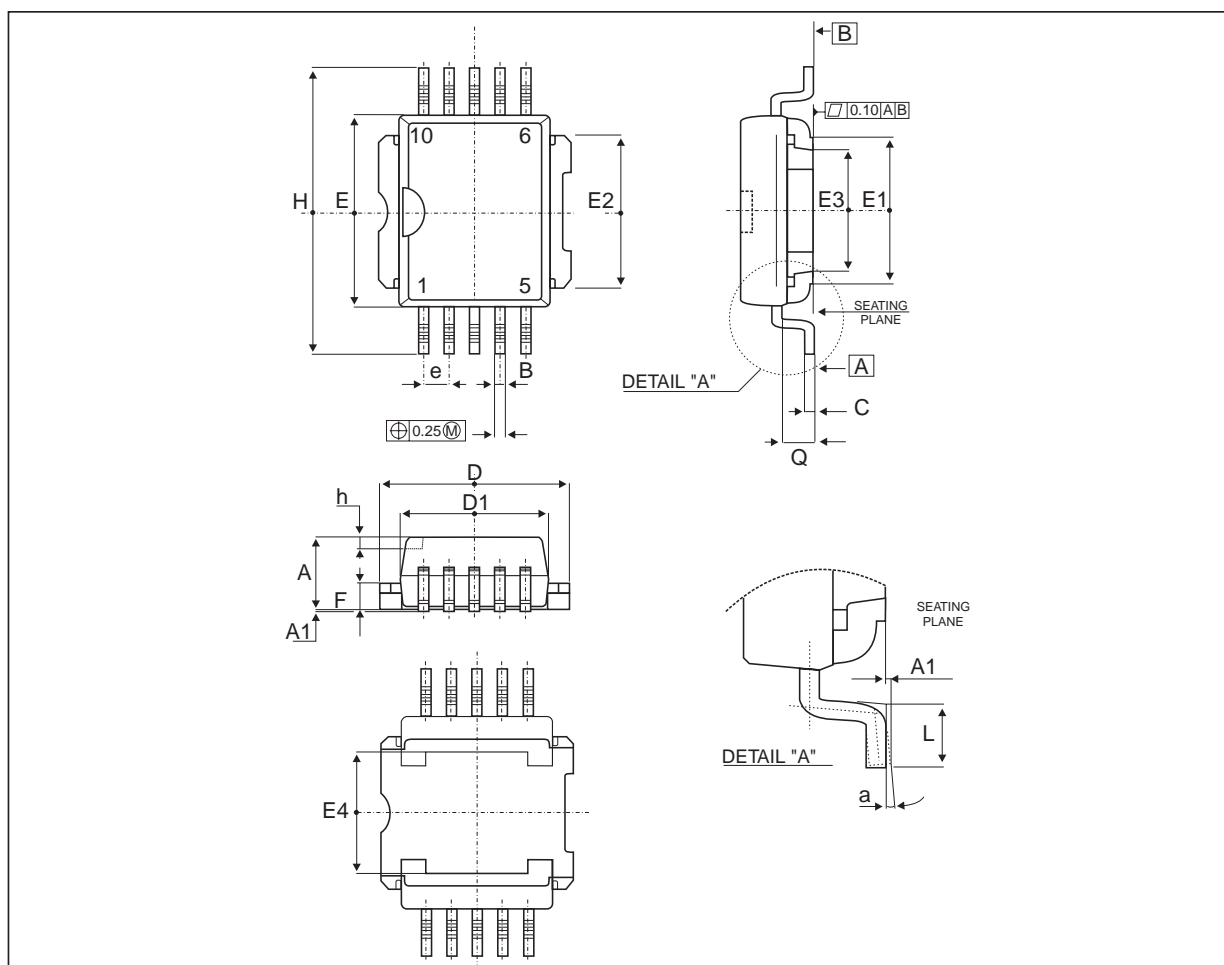
control the high temperature soft soldering as well. An optimized thermal management is guaranteed through PowerSO-10 as the power chips must in any case be mounted on heat spreaders before being mounted onto the substrate.

TABLE 7 : THERMAL IMPEDANCE VERSUS SUBSTRATE

PowerSo-10 package mounted on	$R_{th(j-a)}$	P Diss (*)
1.FR4 using the recommended pad-layout	50°C/W	1.5 W
2.FR4 with heatsink on board (6cm^2)	35°C/W	2.0 W
3.FR4 with copper-filled through holes and external heatsink applied	12°C/W	5.8 W
4. IMS floating in air (40 cm^2)	8°C/W	8.8 W
5. IMS with external heatsink applied	3.5°C/W	20 W

(*) Based on a ΔT of 70°C junction to air.

PACKAGE MECHANICAL DATA



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.35		3.65	0.131		0.143
A1	0.00		0.10	0.00		0.0039
B	0.40		0.60	0.0157		0.0236
C	0.35		0.55	0.0137		0.0217
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.299
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.299

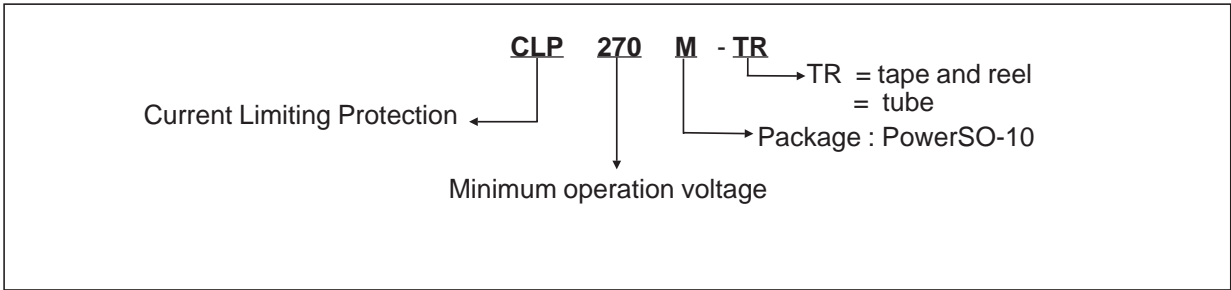
REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.05	
F	1.25		1.35	0.0492		0.0531
H	13.8 0		14.4 0	0.543		0.567
h		0.50			0.019	
L	1.20		1.80	0.0472		0.0708
Q		1.70			0.067	

MARKING

Package	Type	Marking	Packing	Base Quantity
PowerSO-10™	CLP270M	CLP270M	Tube	50
			Tape and reel	60

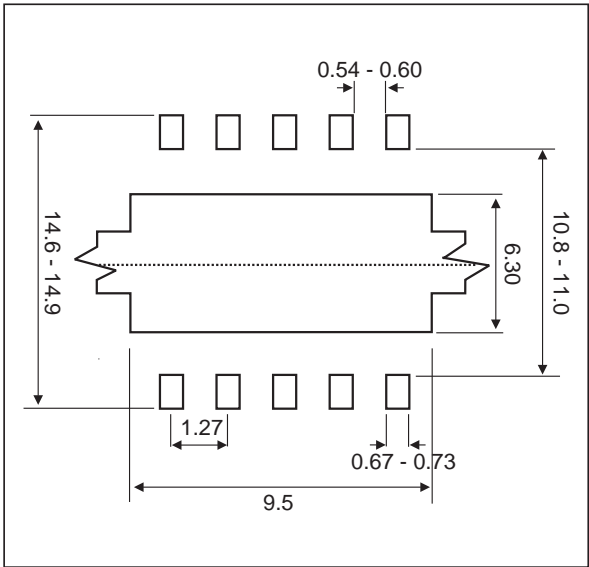
CLP270M

ORDER CODE



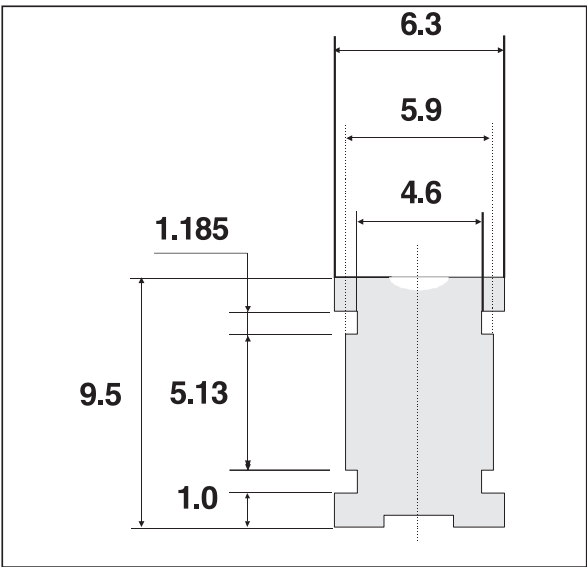
FOOT PRINT

**MOUNTING PAD LAYOUT
RECOMMENDED**



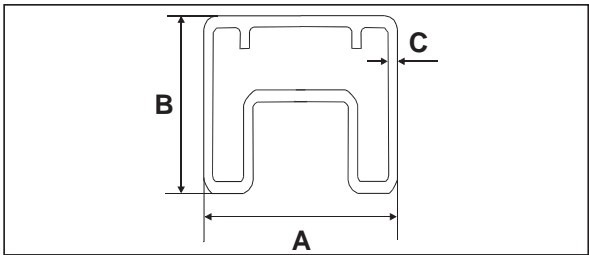
Dimensions in millimeters

HEADER SHAPE



Dimensions in millimeters

SHIPPING TUBE



	DIMENSIONS (mm)
	TYP
A	18
B	12
C	0,8
Length tube	532

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All rights reserved.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany

Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore

Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>

