ICS87608I

LOW VOLTAGE/LOW SKEW, 1:8 PCI/PCI-X ZERO DELAY CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS87608I has a selectable REF_CLK or crystal input. The REF_CLK input accepts LVCMOS or LVTTL input levels. The ICS87608I has a fully integrated PLL along with frequency configurable clock and feedback outputs for multiplying and regenerating clocks with "zero delay".

The ICS87608I is a 1:8 PCI/PCI-X Clock Generator. The ICS87608I has a selectable REF_CLK or crystal input. The REF_CLK input accepts LVCMOS or LVTTL input levels. The ICS87608I has a fully integrated PLL along with frequency configurable clock and feedback outputs for multiplying and regenerating clocks with "zero delay". The PLL's VCO has an operating range of 250MHz-500MHz, allowing this device to be used in a variety of general purpose clocking applications. For PCI/PCI-X applications in particular, the VCO frequency should be set to 400MHz. This can be accomplished by supplying 33.33MHz, 25MHz, 20MHz, or 16.66MHz on the reference clock or crystal input and by selecting ÷12, ÷16, ÷20, or ÷24, respectively as the feedback divide value. The dividers on each of the two output banks can then be independently configured to generate 33.33MHz (÷12), 66.66MHz (÷6), 100MHz (÷4), or 133.33MHz (÷3).

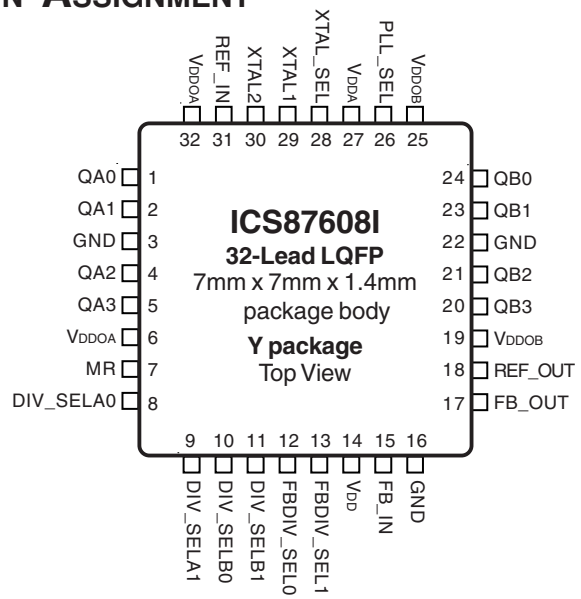
The ICS87608I is characterized to operate with its core supply at 3.3V and each bank supply at 3.3V or 2.5V. The ICS87608I is packaged in a small 7x7mm body LQFP, making it ideal for use in space-constrained applications.

FEATURES

- Fully integrated PLL
- Eight LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS/LVTTL REF_IN clock input
- Maximum output frequency: 166.67MHz
- Maximum crystal input frequency: 38MHz
- Maximum REF_IN input frequency: 41.67MHz
- Individual banks with selectable output dividers for generating 33.333MHz, 66.66MHz, 100MHz and 133.333MHz
- Separate feedback control for generating PCI / PCI-X frequencies from a 16.66MHz or 20MHz crystal, or 25MHz or 33.33MHz reference frequency
- VCO range: 200MHz to 500MHz
- Cycle-to-cycle jitter: 120ps (maximum), @ 3.3V
- Period jitter, RMS: 20ps (maximum)
- Output skew: 250ps (maximum)
- Bank skew: 60ps (maximum)
- Static phase offset: 160ps ± 160ps
- Voltage Supply Modes:
  V_{DD} (core/inputs), V_{DDA} (analog supply for PLL),
  V_{DDOA} (output bank A),
  V_{DDOB} (output bank B, REF_OUT, FB_OUT)

  $V_{DD}/V_{DDA}/V_{DDOA}/V_{DDOB}$
  3.3/3.3/3.3/3.3
  3.3/3.3/2.5/3.3
  3.3/3.3/3.3/2.5
  3.3/3.3/2.5/2.5
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

PIN ASSIGNMENT



BLOCK DIAGRAM

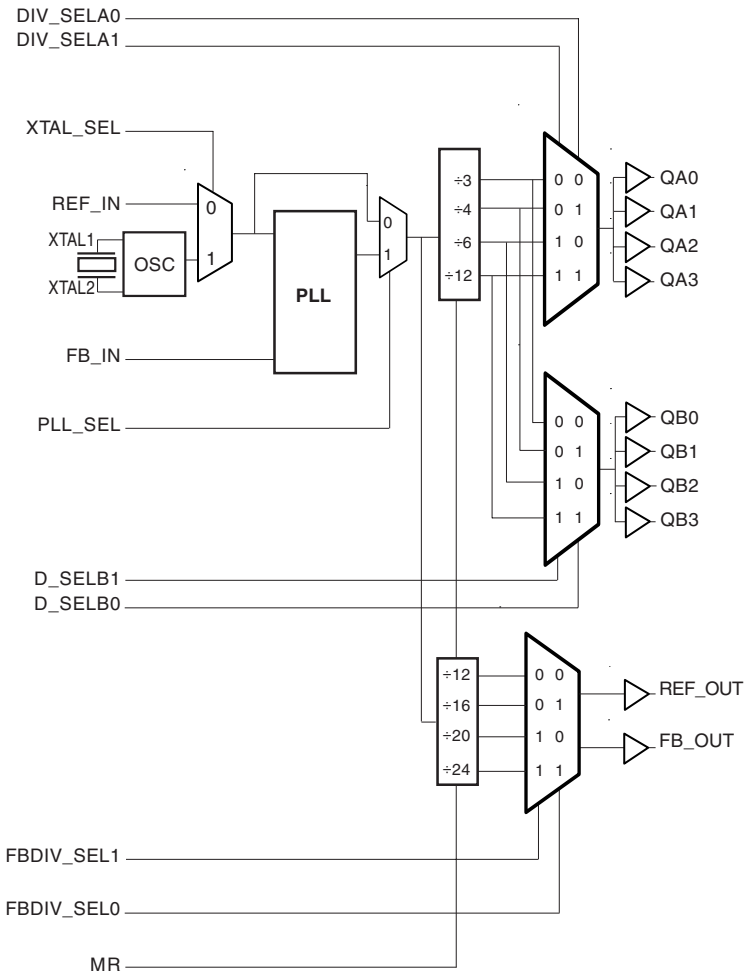


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 4, 5	QA0, QA1, QA2, QA3	Output		Bank A clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
3, 16, 22	GND	Power		Power supply ground.
6, 32	V_{DDOA}	Power		Output supply pins for Bank A outputs.
7	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
8, 9, 10, 11	DIV_SELA0, DIV_SELA1, DIV_SELB0, DIV_SELB1	Input	Pulldown	Selects divide value for clock outputs as described in Table 3. LVCMOS / LVTTL interface levels.
12, 13	FBDIV_SEL0, FBDIV_SEL1	Input	Pulldown	Selects divide value for reference clock output and feedback output. LVCMOS / LVTTL interface levels.
14	V_{DD}	Power		Core supply pin.
15	FB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with "zero delay". LVCMOS / LVTTL interface levels.
17	FB_OUT	Output		Feedback output. Connect to FB_IN. LVCMOS / LVTTL interface levels.
18	REF_OUT	Output		Reference clock output. LVCMOS / LVTTL interface levels.
19, 25	V_{DDOB}	Power		Output supply pins for Bank B and REF_OUT, FB_OUT outputs.
20, 21, 23, 24	QB3, QB2, QB1, QB0	Output		Bank B clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
26	PLL_SEL	Input	Pullup	Selects between PLL and bypass mode. When HIGH, selects PLL. When LOW, selects reference clock. LVCMOS / LVTTL interface levels.
27	V_{DDA}	Power		Analog supply pin. See Applications Note for filtering.
28	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or reference clock as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_IN when LOW. LVCMOS / LVTTL interface levels.
29, 30	XTAL1, XTAL2	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
31	REF_IN	Input	Pulldown	Reference clock input. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DD}, V_{DDA}, V_{DDOX} = 3.465V			9	pF
		V_{DD}, V_{DDA} = 3.465V; V_{DDOX} = 2.625V			11	pF
R_{OUT}	Output Impedance			15		Ω

V_{DDOX} denotes V_{DDOA} and V_{DDOB}.

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Inputs	Outputs	
MR	**QA0:QA3**	**QB0:QB3, FB_OUT, REF_OUT**
1	LOW	LOW
0	Active	Active

TABLE 3B. OPERATING MODE FUNCTION TABLE

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

TABLE 3C. PLL INPUT FUNCTION TABLE

Inputs	
XTAL_SEL	**PLL Input**
0	REF_IN
1	XTAL Oscillator

TABLE 3D. CONTROL FUNCTION TABLE

Inputs							Outputs		
							PLL_SEL =1	Frequency	
FBDIV_ SEL1	**FBDIV_ SEL0**	**Bank B DIV_ SELB1**	**Bank B DIV_ SELB0**	**Bank A DIV_ SELA1**	**Bank A DIV_ SELA0**	**Reference Frequency Range (MHz)**	**QX0:QX3**	**QX0:QX3 (MHz)**	**FB_OUT (MHz)**
0	0	0	0	0	0	16.67 - 41.67	x 4	66.68 - 166.68	16.67 - 41.67
0	0	0	1	0	1	16.67 - 41.67	x 3	50 - 125	16.67 - 41.67
0	0	1	0	1	0	16.67 - 41.67	x 2	33.34 - 83.34	16.67 - 41.67
0	0	1	1	1	1	16.67 - 41.67	x 1	16.67 - 41.67	16.67 - 41.67
0	1	0	0	0	0	12.5 - 31.25	x 5.33	66.63 - 166.56	12.5 - 31.25
0	1	0	1	0	1	12.5 - 31.25	x 4	50 - 125	12.5 - 31.25
0	1	1	0	1	0	12.5 - 31.25	x 2.667	33.34 - 83.34	12.5 - 31.25
0	1	1	1	1	1	12.5 - 31.25	x 1.33	16.63 - 41.56	12.5 - 31.25
1	0	0	0	0	0	10 - 25	x 6.667	66.67 - 166.68	10 - 25
1	0	0	1	0	1	10 - 25	x 5	50 - 125	10 - 25
1	0	1	0	1	0	10 - 25	x 3.33	33.30 - 83.25	10 - 25
1	0	1	1	1	1	10 - 25	x 1.66	16.60 - 41.50	10 - 25
1	1	0	0	0	0	8.33 - 20.83	x 8	66.64 - 166.64	8.33 - 20.83
1	1	0	1	0	1	8.33 - 20.83	x 6	50 - 125	8.33 - 20.83
1	1	1	0	1	0	8.33 - 20.83	x 4	33.32 - 83.32	8.33 - 20.83
1	1	1	1	1	1	8.33 - 20.83	x 2	16.66 - 41.66	8.33 - 20.83

NOTE: VCO frequency range for all configurations above is 200MHz to 500MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDOX} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDOX}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				185	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDOA}	Output Supply Current				20	mA
I_{DDOB}	Output Supply Current				20	mA

V_{DDOX} denotes V_{DDOA}, V_{DDOB}.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDOX} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	MR, DIV_ SELx0, DIV_SELx1, FBDIV_SEL0, FBDIV_SEL1, XTAL_SEL, FB_IN, PLL_SEL		2		V_{DD} + 0.3	V
		REF_IN		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	MR, DIV_ SELx0, DIV_SELx1, FBDIV_SEL0, FBDIV_SEL1, XTAL_SEL, FB_IN, PLL_SEL		-0.3		0.8	V
		REF_IN		-0.3		1.3	V
I_{IH}	Input High Current	DIV_ SELx0, DIV_SELx1, FBDIV_SEL0, FBDIV_SEL1, MR, FB_IN	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		XTAL_SEL, PLL_SEL	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_ SELx0, DIV_SELx1, FBDIV_SEL0, FBDIV_SEL1, MR, FB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		XTAL_SEL, PLL_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DD} = V_{IN}$ = 3.465V	2.6			V
			$V_{DD} = V_{IN}$ = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDOX}/2. See Parameter Measurement Information section, "3.3V Output Load Test Circuit".

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		38	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance			7		pF
Drive Level				1	mW

TABLE 6. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Reference Frequency		8.33		41.67	MHz

TABLE 7A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1	FREF = 25MHz	0	160	325	ps
*t*sk(b)	Bank Skew; NOTE 2, 6				60	ps
*t*sk(o)	Output Skew; NOTE 3, 6				250	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; 6				120	ps
*t*jit(per)	Period Jitter, RMS; NOTE 4, 6, 7				20	ps
*t*sl(o)	Slew Rate		1		4	v/ns
t_L	PLL Lock Time				10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle; NOTE 5		48		52	%

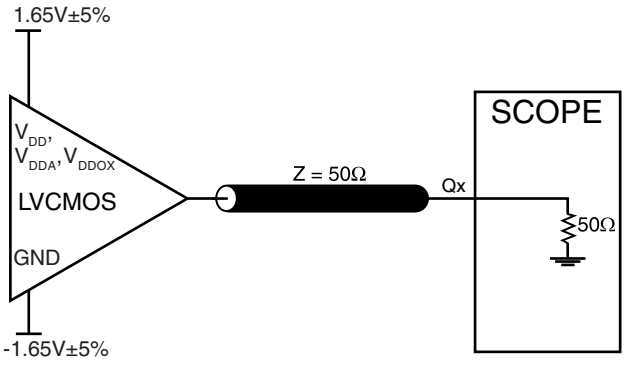
All parameters measured with feedback and output dividers set to DIV by 12 unless otherwise noted.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable. Measured at $V_{DD}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at $V_{DDOX}/2$.
NOTE 4: Jitter performance using LVCMOS inputs.
NOTE 5: Measured using REF_IN. For XTAL input, refer to Application Note.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 7: This parameter is defined as an RMS value.

TABLE 7B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDOX} = 2.5V±5\%$, T_A = -40°C TO 85°C

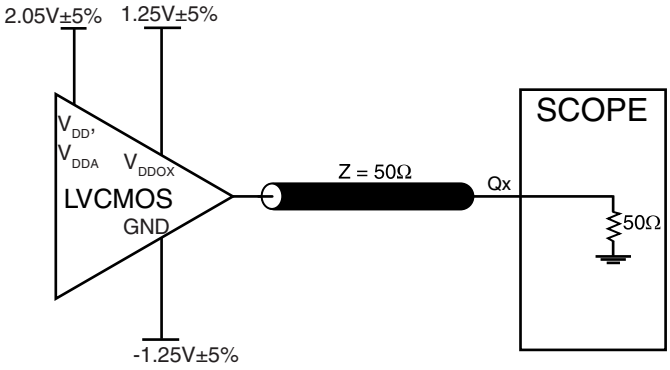
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1	FREF = 25MHz	-365	-105	160	ps
*t*sk(b)	Bank Skew; NOTE 2, 6				60	ps
*t*sk(o)	Output Skew; NOTE 3, 6				250	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; 6				170	ps
*t*jit(per)	Period Jitter, RMS; NOTE 4, 6, 7				20	ps
*t*sl(o)	Slew Rate		1		4	v/ns
t_L	PLL Lock Time				10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle; NOTE 5		48		52	%

All parameters measured with feedback and output dividers set to DIV by 12 unless otherwise noted.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable. Measured at $V_{DD}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at $V_{DDOX}/2$.
NOTE 4: Jitter performance using LVCMOS inputs.
NOTE 5: Measured using REF_IN. For XTAL input, refer to Application Note.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 7: This parameter is defined as an RMS value.

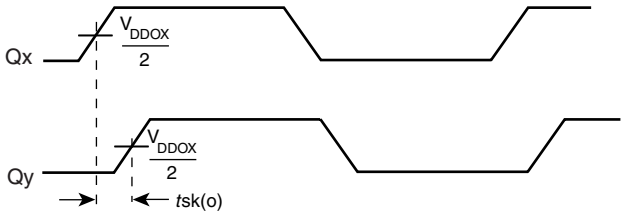
PARAMETER MEASUREMENT INFORMATION



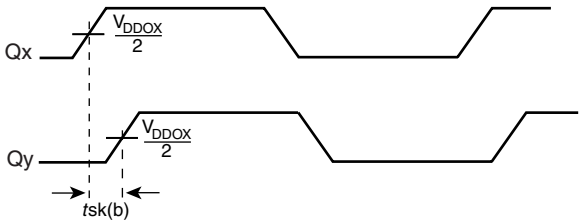
3.3V OUTPUT LOAD AC TEST CIRCUIT
(Where X denotes outputs in the same Bank)



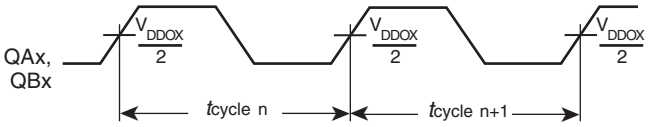
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW

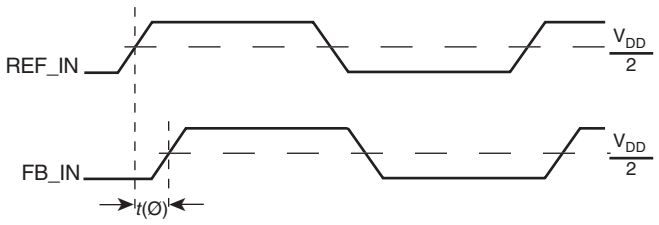


BANK SKEW

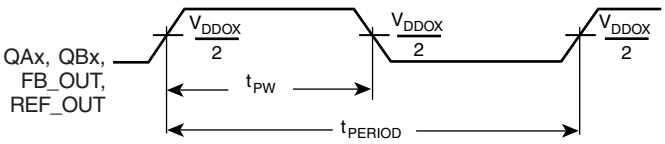


$t\text{jit(cc)} = t\text{cycle n} - t\text{cycle n+1}$
1000 Cycles

CYCLE-TO-CYCLE JITTER

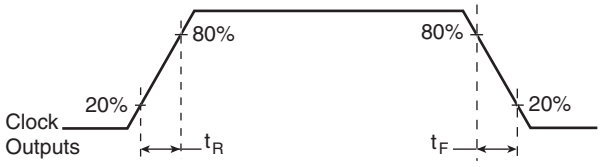


STATIC PHASE OFFSET



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT PULSE WIDTH/PULSE WIDTH PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87608I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDOX} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

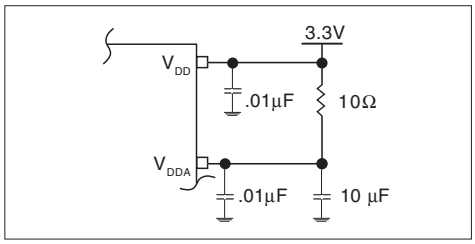


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

CRYSTAL INPUT INTERFACE

The ICS87608I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the frequency ppm error. The optimum C1 and C2 values can be slightly adjusted for optimum frequency accuracy.

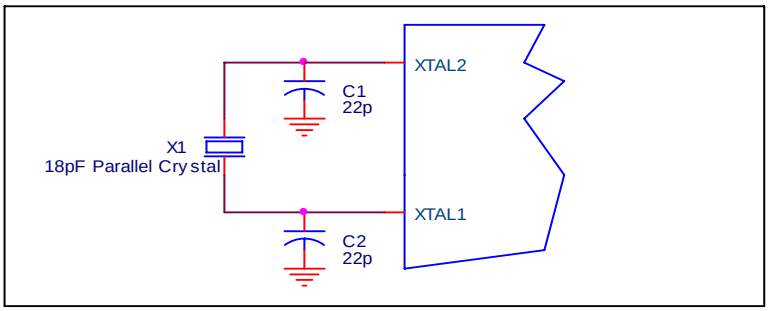


Figure 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

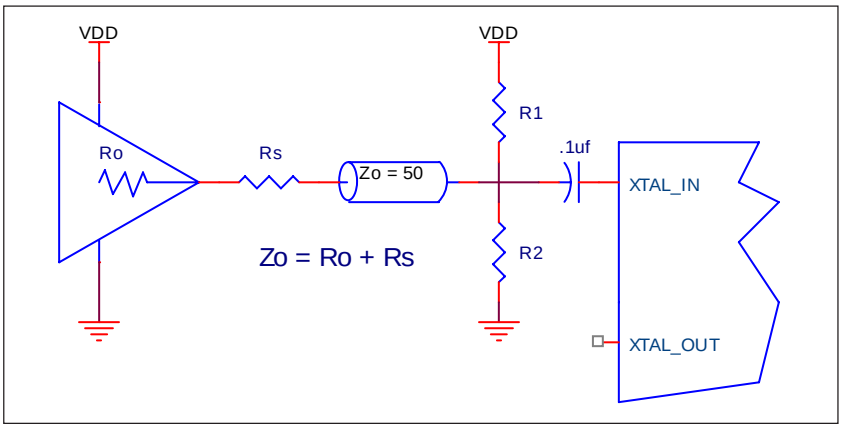


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87608I is: 5495

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

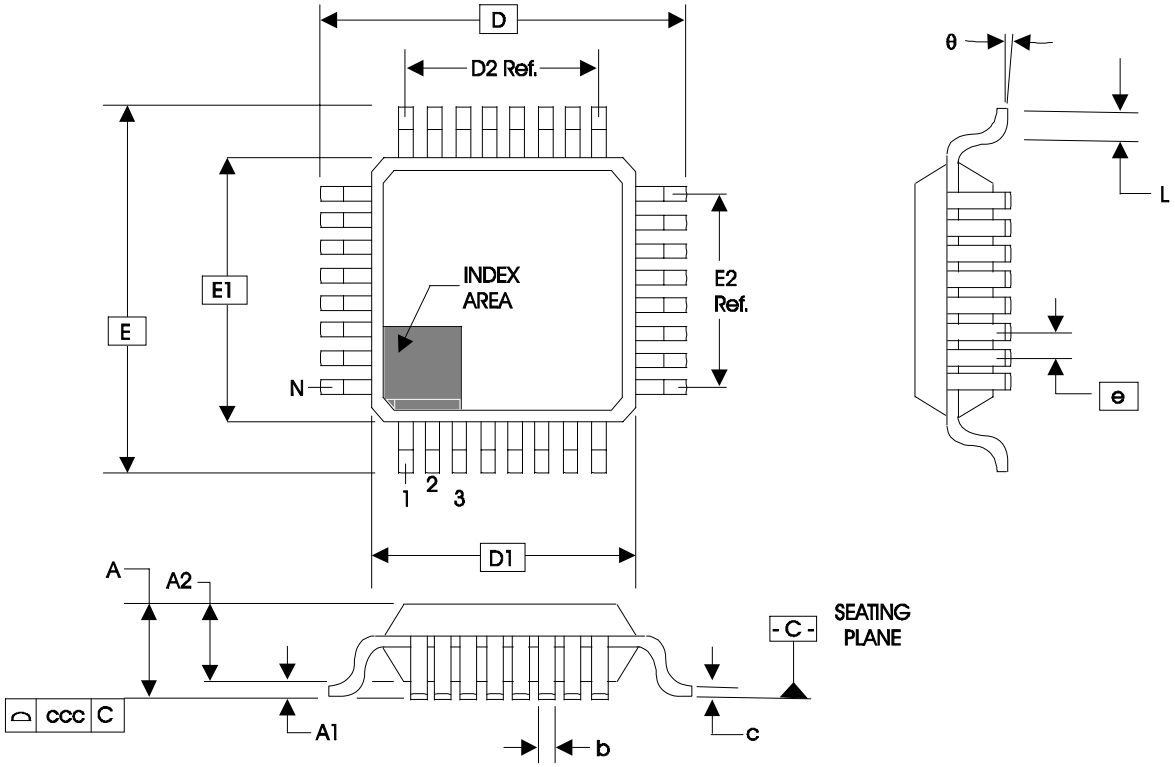


TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87608AYI	ICS87608AYI	32 Lead LQFP	tray	-40°C to 85°C
87608AYIT	ICS87608AYI	32 Lead LQFP	1000 tape & reel	-40°C to 85°C
87608AYILF	ICS87608AILF	32 Lead Lead-Free LQFP	tray	-40°C to 85°C
87608AYILFT	ICS87608AILF	32 Lead Lead-Free LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS complaint.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		2	Corrected MR in the Block Diagram.	4/6/04
A		7	Parameter Measurement Information - for 3.3V Outpt Load AC Test Circuit diagram corrected GND from "-1.165V±5%" to "-1.65V±5%".	4/23/04
A	T10	11	Ordering Information Table - added Lead-Free part number.	10/11/04
B	T7B	6	AC Characteristics Table - changed tjit(cc) from 120ps max to 170ps max.	1/28/05
B		1	Feature section, Cycle-to-Cycle Jitter note - added "@ 3.3V".	3/11/05
C	T2	3	Pin Characteristics Table - corrected $R_{PULLUP/DOWN}$ values from 51Ω max. to 51kΩ typical.	11/11/05
	T5	6	Crystal Characterisitics Table - Added Drive Level parameter.	
		9	Added *Recommendations for Unused Input and Output Pins.*	
	T10	12	Ordering Information Table - added lead-free note.	
C		10	Added *LVCMOS to XTAL Interface.*	4/28/06
	T10	12	Ordering Information Table - corrected lead-free marking.	
C	T10	13	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column.	10/13/10
		15	Added Contact Page.	

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www.IDT.com

6024 Silver Creek Valley Road
San Jose, CA 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775

Tech Support
netcom@idt.com