maxim integrated™

EVALUATION KIT AVAILABLE

MAX19794

10MHz to 500MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

General Description

The MAX19794 dual general-purpose analog voltage variable attenuator (VVA) is designed to interface with 50Ω systems operating in the 10MHz to 500MHz frequency range. This device includes a patented control circuit that provides 22.4dB of attenuation range (per attenuator) with a typical linear control slope of 8dB/V.

Both attenuators share a common analog control. They can be cascaded together to yield 44.7dB of total attenuation range with a typical combined linear control slope of 16dB/V (5V operation). Alternatively, the on-chip, 4-wire SPI-controlled 10-bit DAC can be used to control both attenuators. In addition, a step-up/down feature allows user-programmable attenuator stepping through command pulses without re-programming the SPI interface.

The MAX19794 is a monolithic device designed using one of Maxim's proprietary SiGe BiCMOS processes. The part operates from a single +5V supply or alternatively operates from a single +3.3V supply. It is available in a compact 36-pin TQFN package (6mm x 6mm x 0.8mm) with an exposed pad. Electrical performance is guaranteed over the -40°C to +100°C extended temperature range.

Applications

Broadband System Applications, Including Wireless Infrastructure Digital and Spread-Spectrum Communication Systems

WCDMA/LTE, TD-SCDMA/TD-LTE, WiMAX®, cdma2000®, GSM/EDGE and MMDS Base Stations

VSAT/Satellite Modems

Microwave Point to Point Systems

Lineup Gain Trim

Temperature Compensation Circuits

Automatic Level Control (ALC)

Transmitter Gain Control

Receiver Gain Control

General Test Equipment

Benefits and Features

- **Wide Band Coverage**
  - **RF Frequency Range from 10MHz to 500MHz**
- **High Linearity**
  - **Greater than +34.4dBm IIP3 over the Full Attenuation Range**
  - **+21.8dBm Input P_{1dB}**
- **Integrates Two Analog Attenuators in One Monolithic Device**
- **Two Convenient Control Options**
  - **Single Analog Voltage**
  - **On-Chip, SPI-Controlled 10-Bit DAC**
- **Step-Up/Down Pulse Command Inputs**
- **Flexible Attenuation Control Ranges**
  - **22.4dB (per Attenuator)**
  - **44.7dB (both Attenuators Cascaded)**
- **Linear dB/V Analog Control Response Curve Simplifies Automatic Leveling Control and Gain Trim Algorithms**
- **Excellent Attenuation Flatness over Wide Frequency Ranges and Attenuation Settings**
- **On-Chip Comparator (for Successive Approximation Measurement of Attenuator Control Voltage)**
- **Low 13mA Supply Current**
- **Single +5V or 3.3V Supply Voltage**
- **Pin Similar with MAX19791, MAX19792, and MAX19793**
- **Lead-Free Package**

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX19794.related.

10MHz to 500MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

ABSOLUTE MAXIMUM RATINGS

V_{CC} ....-0.3V to +5.5V
REF_IN.............................-0.3V to Minimum (V_{CC} + 0.3V, 3.6V)
REF_SEL, DAC_LOGIC,MODE, DWN, UP,
DIN, CLK, $\overline{CS}$................-0.3V to Minimum (V_{CC} + 0.3V, 3.6V)
COMP_OUT, DOUT...-0.3V to +3.6V
IN_A, OUT_A, IN_B, OUT_B .... -0.3V to V_{CC} + 0.3V
CTRL (except for test mode)....................... -0.3V to V_{CC} + 0.3V
Maximum CTRL Pin Load Current
(CTRL configured as an output)...................................0.3mA

RF Input Power at IN_A, IN_B, OUT_A, OUT_B .... +20dBm
Continuous Power Dissipation (Note 1) 2.8W
Operating Case Temperature Range (Note 2) ...-40°C to +100°C
Maximum Junction Temperature...................................... 150°C
Storage Temperature .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Application Information* section for details. The junction temperature must not exceed +150°C.

Note 2: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA})
(Notes 3, 4) .... +36°C/W

Junction-to-Case Thermal Resistance (θ_{JC})
(Notes 1, 4) .... +10°C/W

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

3.3V DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.15V to 3.45V, V_{CTRL} = 1V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, no RF signals applied, all input and output ports terminated with 50Ω through DC blocks, T_C = -40°C to +100°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.15	3.3	3.45	V
Supply Current	I_{CC}			9.5	14	mA
Control Voltage Range	V_{CTRL}		1.0		2.5	V
CTRL Input Resistance	R_{CTRL}			1.0		MΩ
Input CurrentLogic-High	I_{IH}		-1.0		+1.0	µA
Input Current Logic-Low	I_{IL}		-1.0		+1.0	µA
REF_IN Voltage				1.4		V
REF_IN Input Resistance				1.0		MΩ
DAC Number of Bits		Monotonic			10	bits
Input Voltage Logic-High	V_{IH}		2.0			V
Input Voltage Logic-Low	V_{IL}				0.8	V
COMP_OUT Logic-High		RDBK_EN (D9, REG3) = Logic 1, R_{LOAD} = 47kΩ		3.3		V
COMP_OUT Logic-Low		RDBK_EN (D9, REG3) = Logic 1, R_{LOAD} = 47kΩ		0		V

5V DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, no RF signals applied, all input and output ports terminated with 50Ω through DC blocks, T_C = -40°C to +100°C, unless otherwise noted. Typical values are at V_{CC} = 5.0V, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.0	5.25	V
Supply Current	I_{CC}			13	18.6	mA
Control Voltage Range	V_{CTRL}		1.0		4.0	V
CTRL Input Resistance	R_{CTRL}			124		kΩ
Input Current Logic-High	I_{IH}		-1.0		+1.0	µA
Input Current Logic-Low	I_{IL}		-1.0		+1.0	µA
REF_IN Voltage Range				1.4		V
REF_IN Input Resistance				1.0		MΩ
DAC Number of Bits		Monotonic		10		Bits
Input Voltage Logic-High	V_{IH}		2.0			V
Input Voltage Logic-Low	V_{IL}				0.8	V
COMP_OUT Logic-High		RDBK_EN (D9, REG3) = Logic 1, R_{LOAD} = 47kΩ		3.3		V
COMP_OUT Logic-Low		RDBK_EN (D9, REG3) = Logic 1, R_{LOAD} = 47kΩ		0		V

Recommended AC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Note 6)	10		500	MHz
RF Port Input Power	P_{RF}	Continuous operation			15	dBm

3.3V AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, one attenuator, V_{CC} = 3.15V to 3.45V, RF ports are driven from 50Ω sources and loaded into 50Ω, input P_{RF} = 0dBm, f_{RF} = 10MHz to 500MHz, V_{CTRL} = 1V to 2.5V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = -40°C to +100°C. Typical values are for T_C = +25°C, V_{CC} = 3.3V, input P_{RF} =0dBm, f_{RF} = 55MHz, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, unless otherwise noted.) (Notes 5, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss	IL	One attenuator		1.5		dB
		Two attenuators, f_{RF} = 55MHz, V_{CTRL} = 1.0V		3.0	5.0	
Loss Variation Over Temperature		T_C = -40°C to +100°C		0.28		dB
Input P1dB	IP1dB			16.4		dBm
Minimum Input Second-Order Intercept Point Over Full Attenuation Range (Note 8)	IIP2	One attenuator f_{RF1} +f_{RF2} term, f_{RF1} - f_{RF2} = 1MHz V_{CTRL} = 1.0V to 2.5V P_{RF} = 0dBm/tone applied to attenuator input		44.9		dBm
		Two attenuators f_{RF1} + f_{RF2} term, f_{RF1} - f_{RF2} = 1MHz V_{CTRL} = 1.0V to 2.0V P_{RF} = 0dBm/tone applied to attenuator input		42.7		
Minimum Input Third-Order Intercept Point Over Full Attenuation Range (Note 8)	IIP3	One attenuator V_{CTRL} =1.0V to 2.5V f_{RF1} - f_{RF2} = 1MHz P_{RF} = 0dBm/tone applied to attenuator input		30.8		dBm
		Two attenuators V_{CTRL} =1.0V to 2.0V f_{RF1} - f_{RF2} = 1MHz P_{RF} = 0dBm/tone applied to attenuator input		29.9		
Second Harmonic				62		dBc
Third Harmonic				89.7		dBc
Attenuation Control Range		One attenuator, V_{CTRL} = 1.0V to 2.5V, f_{RF} = 55MHz		22.5		dB
		Two attenuators, V_{CTRL} = 1.0V to 2.5V, f_{RF} = 55MHz	38.5	45		dB
Average Attenuation-Control Slope		V_{CTRL} = 1.4V to 2.3V		22.5		dB/V
Maximum Attenuation-Control Slope		V_{CTRL} = 1.0V to 2.5V		40		dB/V
S21 Attenuation Deviation from a straight line		V_{CTRL} = 1.4V to 2.1V		±0.4		dB

5V AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, one attenuator, V_{CC} = 4.75V to 5.25V, RF ports are driven from 50Ω sources and loaded into 50Ω, input P_{RF} = 0dBm, f_{RF} = 10MHz to 500MHz, V_{CTRL} = 1V to 4V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = -40°C to +100°C. Typical values are for T_C = +25°C, V_{CC} = 5.0V, input P_{RF} = 0dBm, f_{RF} = 55MHz, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, unless otherwise noted.) (Notes 5, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Insertion Loss	IL	One attenuator		1.5		dB
		Two attenuators		3.0	5.0	dB
Loss Variation Over Temperature		T_C = -40°C to +100°C		0.29		dB
Input P_{1dB}	IP_{1dB}			21.8		dBm
Minimum Input Second-Order Intercept Point Over Full Attenuation Range (Note 8)	IIP2	One attenuator f_{RF1} + f_{RF2} term, f_{RF1} - f_{RF2} = 1MHz V_{CTRL} = 1.0V to 4.0V P_{RF} = 0dBm/tone applied to attenuator input		48.1		dBm
		Two attenuators f_{RF1} +f_{RF2} term, f_{RF1} - f_{RF2} = 1MHz V_{CTRL} = 1.0V to 4.0V P_{RF} = 0dBm/tone applied to attenuator input		46.5		
Minimum Input Third-Order Intercept Point Over Full Attenuation Range (Note 8)	IIP3	One attenuator V_{CTRL} from 1.0V to 4.0V f_{RF1} - f_{RF2} = 1MHz P_{RF} = 0dBm/tone applied to attenuator input		34.4		dBm
		Two attenuators V_{CTRL} from 1.0V to 4.0V f_{RF1} - f_{RF2} = 1MHz P_{RF} = 0dBm/tone applied to attenuator input		32.3		
Second Harmonic				63		dBc
Third Harmonic				97		dBc
Attenuation Control Range		One attenuator, V_{CTRL} = 1.0V to 4.0V, f_{RF} = 55MHz		22.4		dB
		Two attenuators V_{CTRL} = 1.0V to 4.0V, f_{RF} = 55MHz	38.5	44.7		dB
Average Attenuation-Control Slope		V_{CTRL} = 1.5V to 3.1V		8.0		dB/V
		V_{CTRL} = 1.5V to 3.5V		9.4		
Maximum Attenuation-Control Slope		V_{CTRL} = 1.5V to 3.5V		30		dB/V
Attenuation Flatness over any 125MHz band		V_{CTRL} = 1.0V to 3.1V, f_{RF} = 10MHz to 250MHz		0.15		dB
		V_{CTRL} = 1.0V to 3.1V, f_{RF} = 250MHz to 500MHz		0.2		

5V AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, one attenuator, V_{CC} = 4.75V to 5.25V, RF ports are driven from 50Ω sources and loaded into 50Ω, input P_{RF} = 0dBm, f_{RF} = 10MHz to 500MHz, V_{CTRL} = 1V to 4V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = -40°C to +100°C. Typical values are for T_C = +25°C, V_{CC} = 5.0V, input P_{RF} = 0dBm, f_{RF} = 55MHz, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, unless otherwise noted.) (Notes 5, 7)

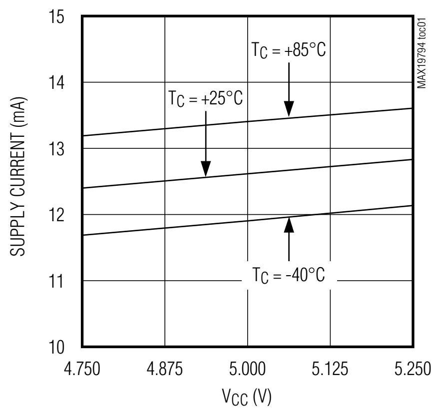
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
CTRL Switching Time (Note 9)		15dB to 0dB range		390		ns
		0dB to 15dB range		780		
$\overline{CS}$ Switching Time (Note 10)		15dB to 0dB range		700		ns
		0dB to 15dB range		2600		
MODE Switching Time (Note 11)		15dB to 0dB range (MODE 1 to 0)		700		ns
		0dB to 15dB range (MODE 0 to 1)		2600		
Input Return Loss				31		dB
Output Return Loss				28		dB
Group Delay				40		ps
Group Delay Flatness		f_{RF} = 30MHz to 88MHz		25		ps
Group Delay Change		V_{CTRL} = 1.0V to 4.0V		-400		ps
Insertion Phase Change vs. Attenuation Control		V_{CTRL} = 1.0V to 4.0V		5		deg
S21 Attenuation Deviation from a Straight Line		V_{CTRL} = 1.5V to 3.1V		±0.35		dB
SERIAL PERIPHERAL INTERFACE (SPI)						
Maximum Clock Speed				20		MHz
Data-to-Clock Setup Time	t_{CS}	(Note 12)		2		ns
Data-to-Clock Hold Time	t_{CH}	(Note 12)		2.5		ns
$\overline{CS}$ to CLK Setup Time	t_{EWS}	(Note 12)		3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}	(Note 12)		7		ns
Clock Pulse Width	t_{CW}	(Note 12)		5		ns

Note 5: Production tested at T_C = +100°C. All other temperatures are guaranteed by design and characterization.
Note 6: Recommended functional range. Not production tested. Operation outside this range is possible, but with degraded performance of some parameters.
Note 7: All limits include external component losses, connectors and PCB traces. Output measurements taken at the RF port of the typical application circuit.
Note 8: f_{RF1} = 56MHz, f_{RF2} = 55MHz, P_{RF} = 0dBm/tone applied to attenuator input.
Note 9: Switching time is measured from 50% of the CTRL signal to when the RF output settles to ±1dB. R3 = 0Ω
Note 10: Switching time is measured from when $\overline{CS}$ is asserted to when the RF output settles to ±1dB.
Note 11: Switching time is measured from when MODE is asserted to when the RF output settles to ±1dB.
Note 12: Typical minimum time for proper SPI operation.

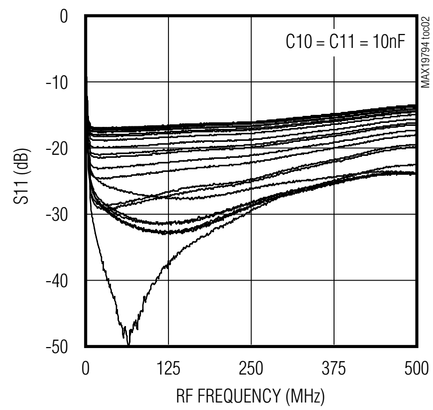
Typical Operating Characteristics

(*Typical Application Circuit*, V_{CC} **= 5.0V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

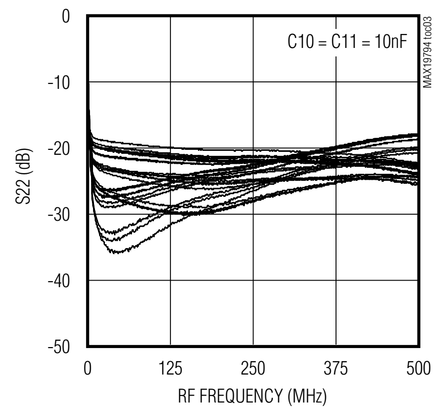
SUPPLY CURRENT vs. V_{CC}



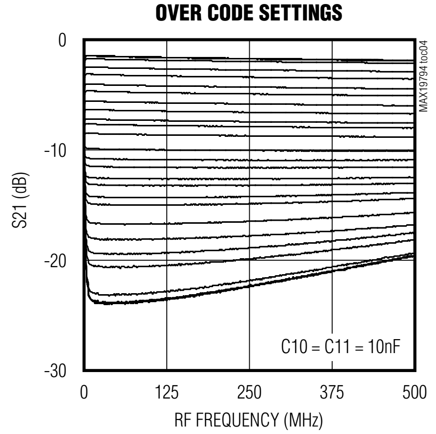
INPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



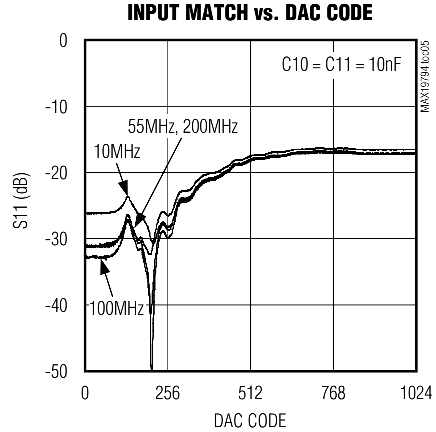
OUTPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



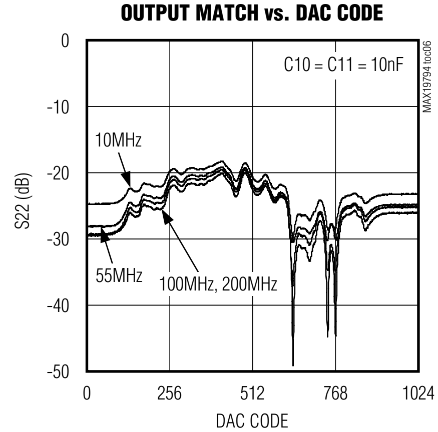
ATTENUATION vs. RF FREQUENCY OVER CODE SETTINGS



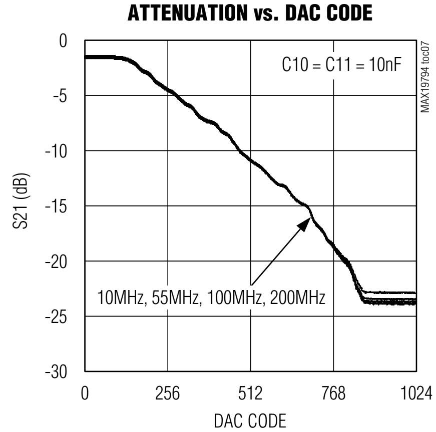
INPUT MATCH vs. DAC CODE



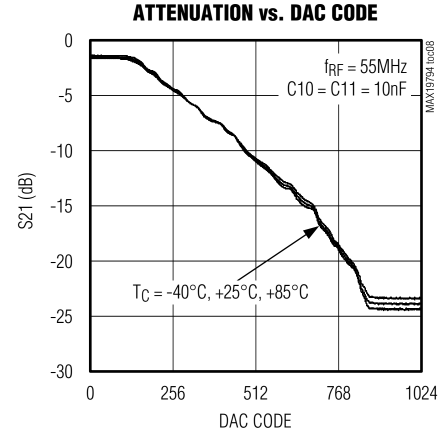
OUTPUT MATCH vs. DAC CODE



ATTENUATION vs. DAC CODE



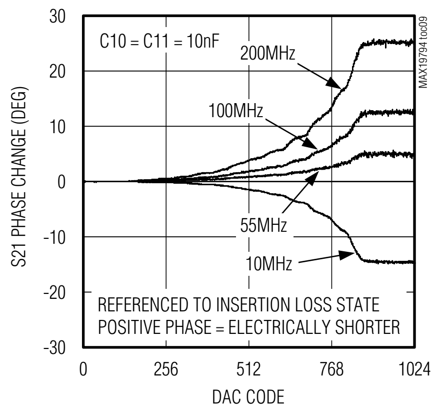
ATTENUATION vs. DAC CODE



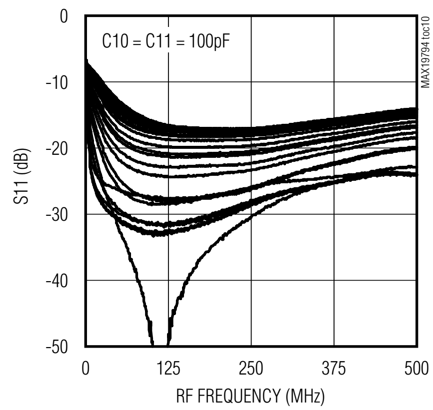
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

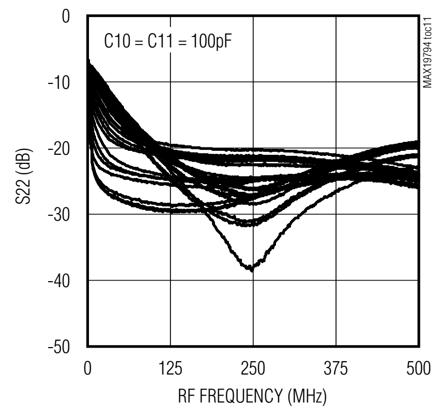
S21 PHASE CHANGE vs. DAC CODE



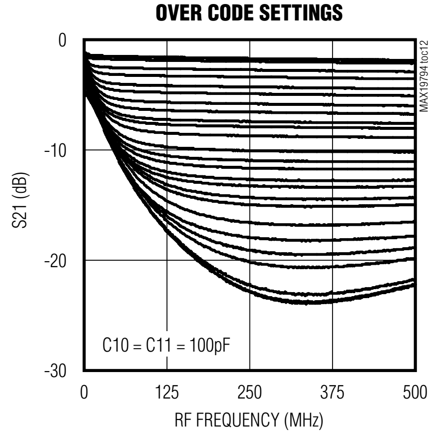
INPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



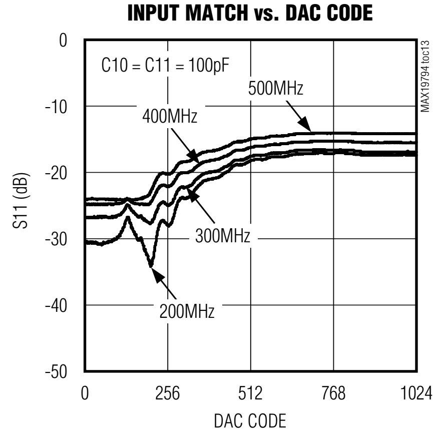
OUTPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



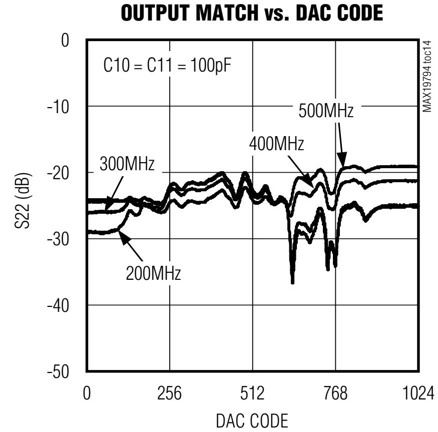
ATTENUATION vs. RF FREQUENCY OVER CODE SETTINGS



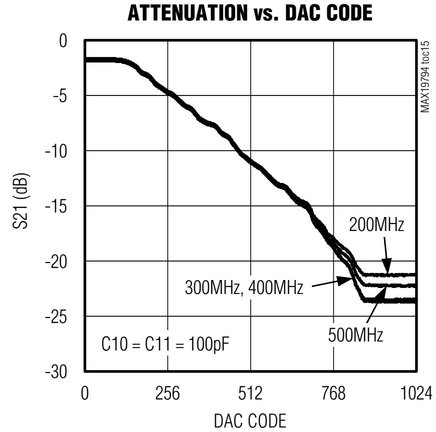
INPUT MATCH vs. DAC CODE



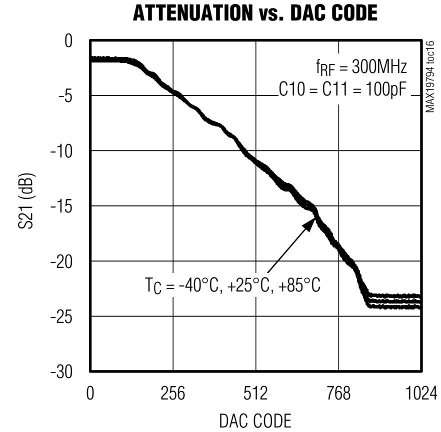
OUTPUT MATCH vs. DAC CODE



ATTENUATION vs. DAC CODE



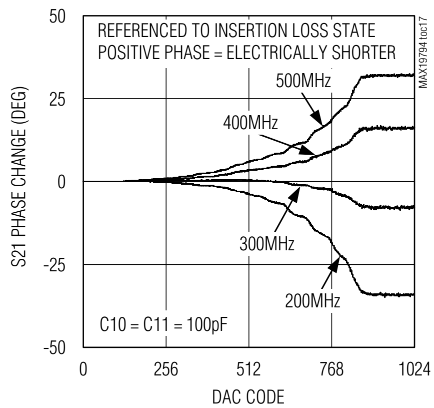
ATTENUATION vs. DAC CODE



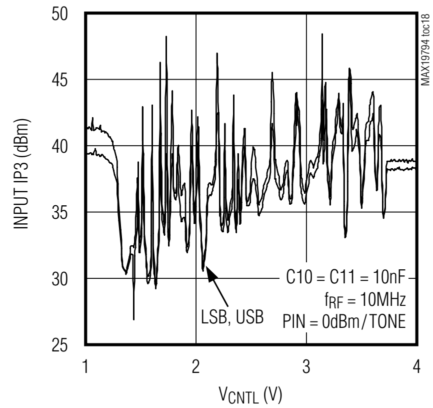
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

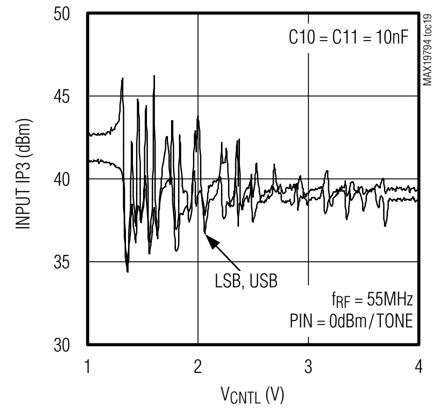
S21 PHASE CHANGE vs. DAC CODE



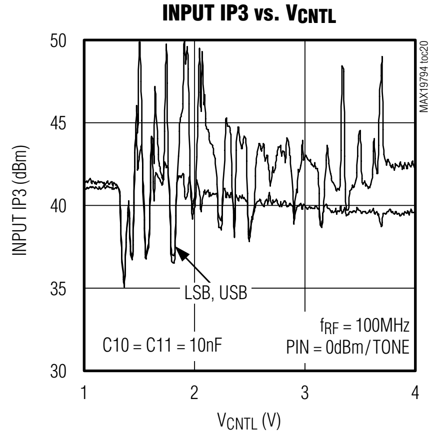
INPUT IP3 vs. V_{CNTL}



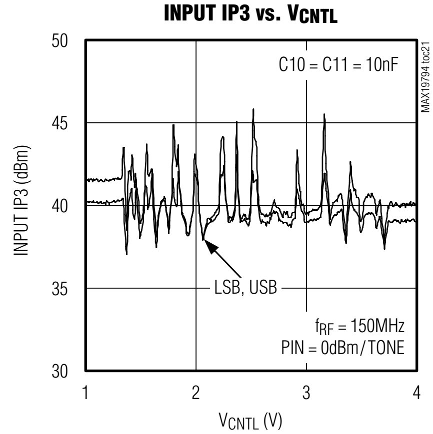
INPUT IP3 vs. V_{CNTL}



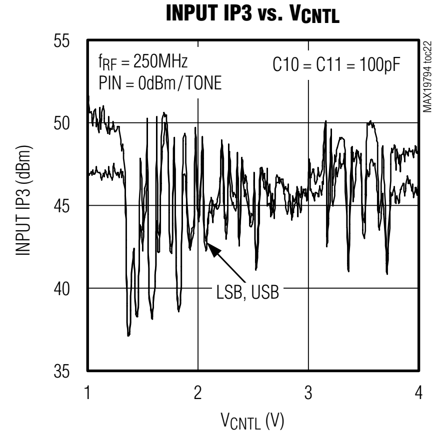
INPUT IP3 vs. V_{CNTL}



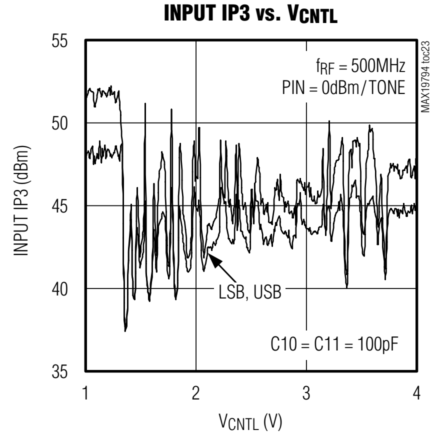
INPUT IP3 vs. V_{CNTL}



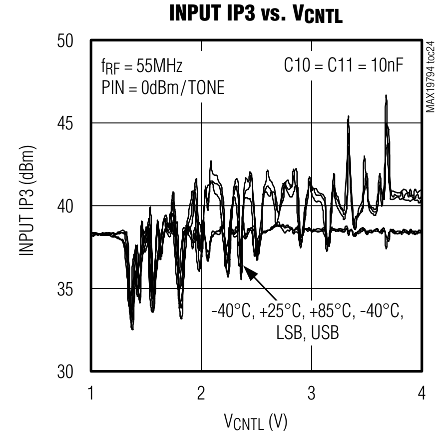
INPUT IP3 vs. V_{CNTL}



INPUT IP3 vs. V_{CNTL}

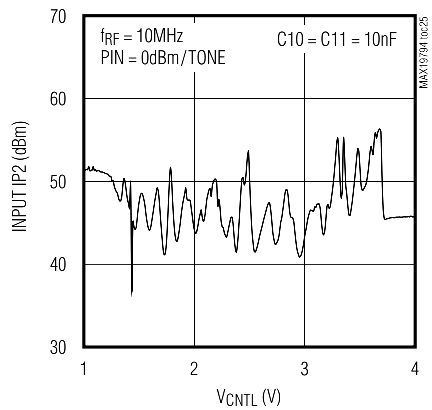


INPUT IP3 vs. V_{CNTL}

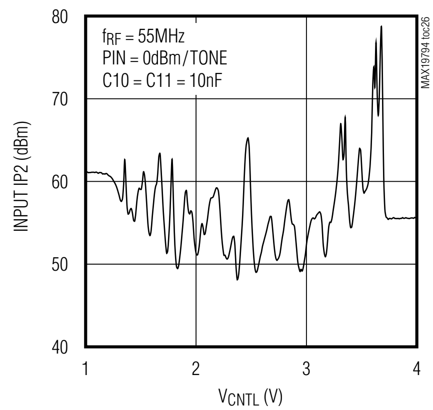


Typical Operating Characteristics (continued)

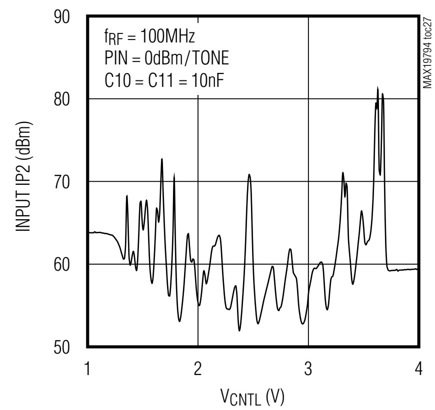
(Typical Application Circuit, V_{CC} = 5.0V, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = 25°C, unless otherwise noted.).



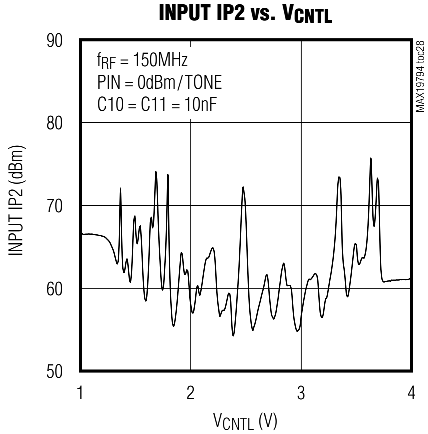
INPUT IP2 vs. VCNTL



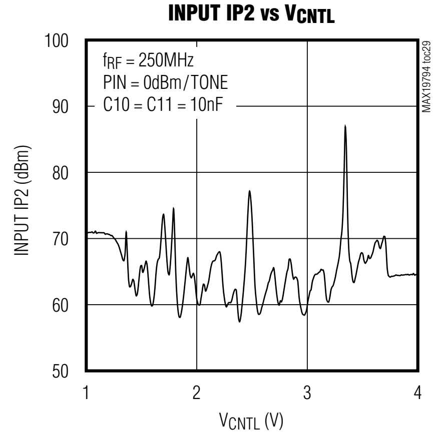
INPUT IP2 vs. VCNTL



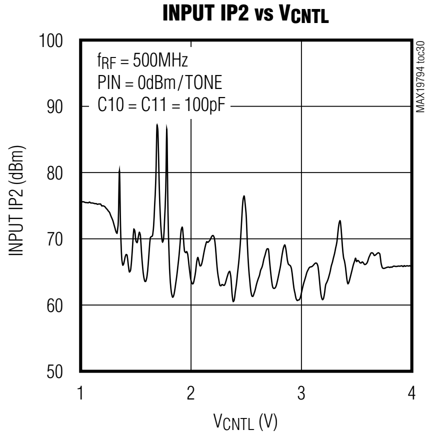
INPUT IP2 vs. VCNTL



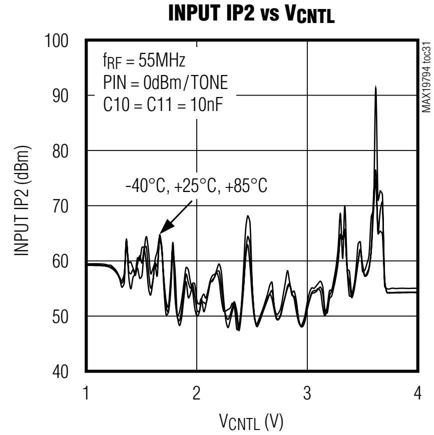
INPUT IP2 vs. VCNTL



INPUT IP2 vs VCNTL



INPUT IP2 vs VCNTL

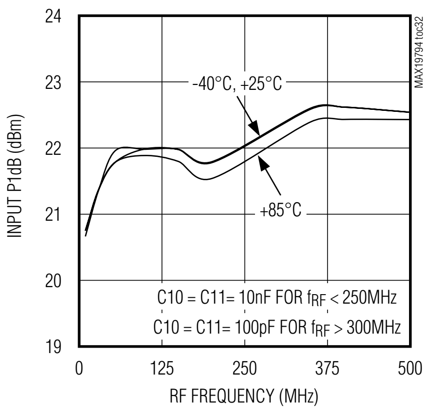


INPUT IP2 vs VCNTL

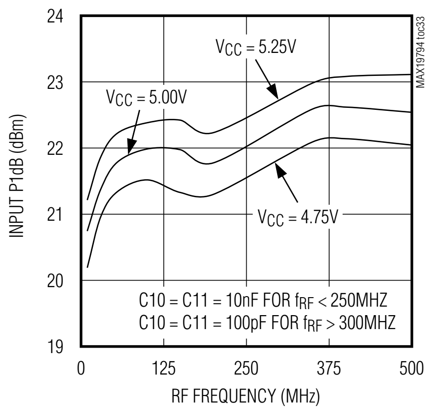
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = 25°C, unless otherwise noted.).

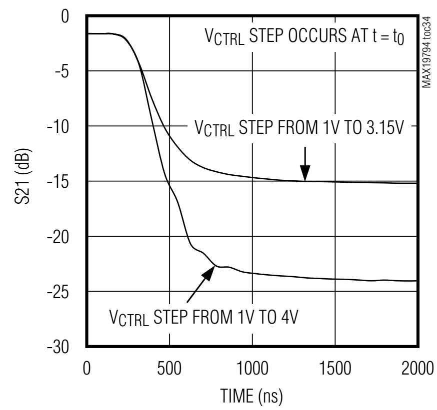
INPUT P1dB vs. RF FREQUENCY



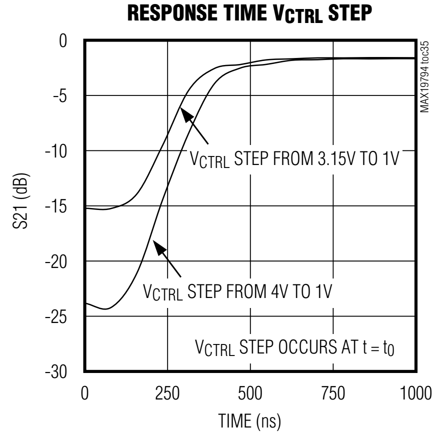
INPUT P1dB vs. RF FREQUENCY



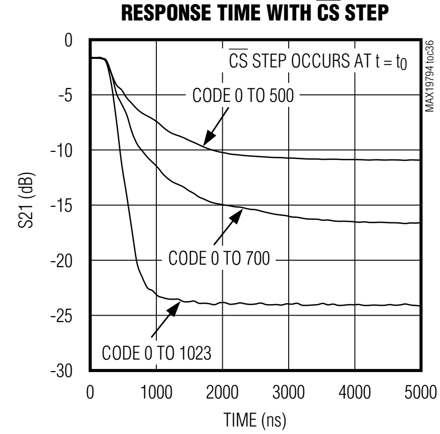
RESPONSE TIME V_{CTRL} STEP



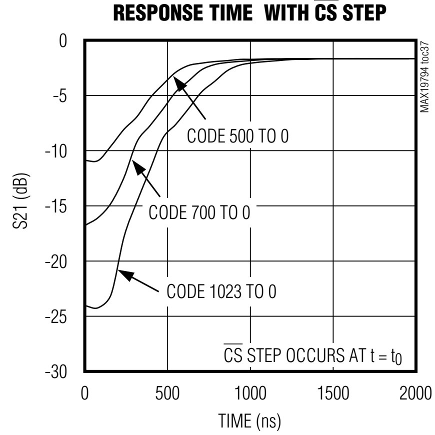
RESPONSE TIME V_{CTRL} STEP



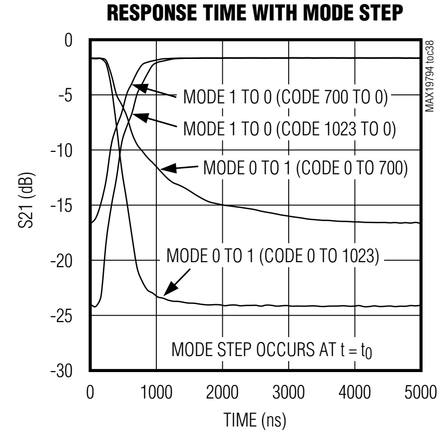
RESPONSE TIME WITH $\overline{CS}$ STEP



RESPONSE TIME WITH $\overline{CS}$ STEP



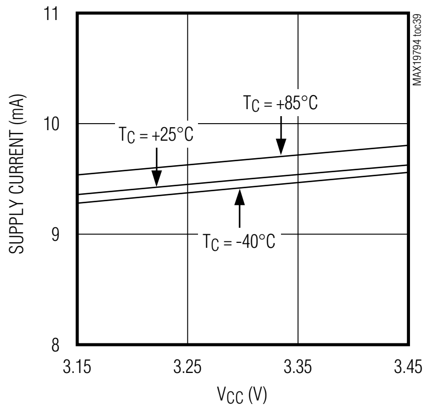
RESPONSE TIME WITH MODE STEP



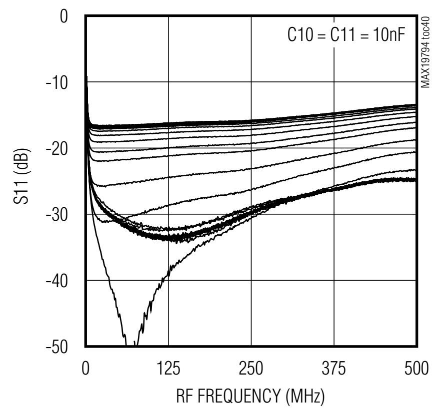
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 3.3V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

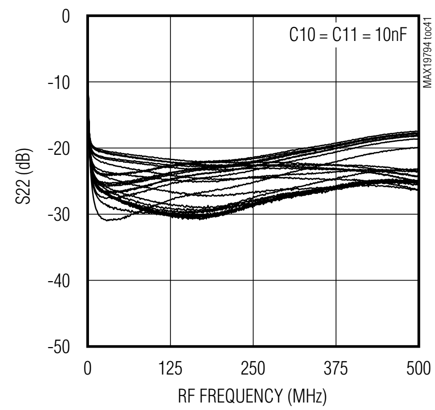
SUPPLY CURRENT vs. VCC



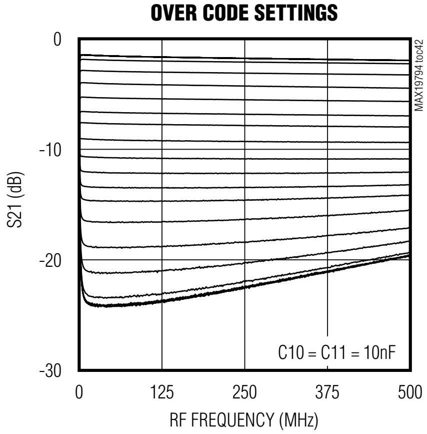
INPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



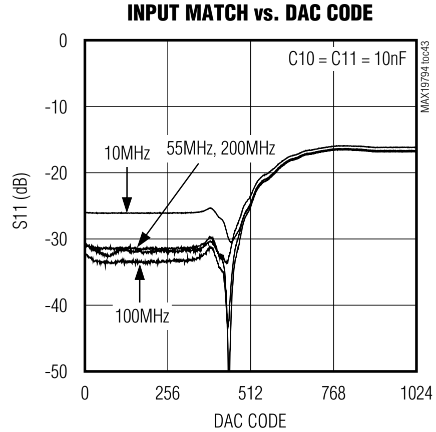
OUTPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



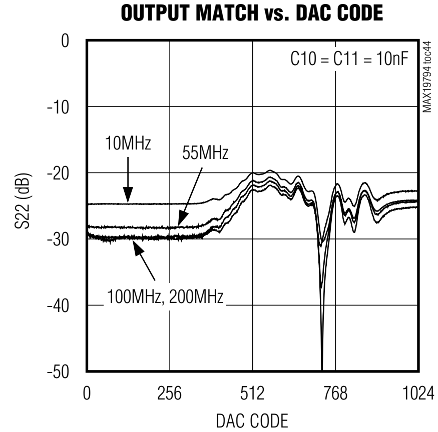
ATTENUATION vs. RF FREQUENCY OVER CODE SETTINGS



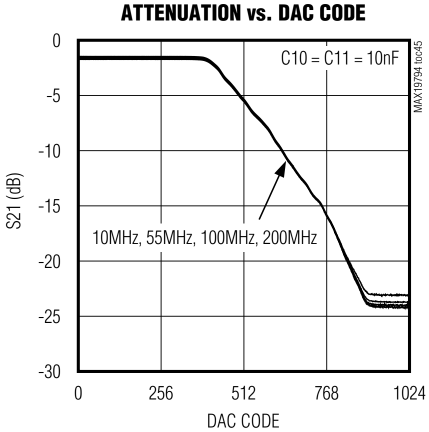
INPUT MATCH vs. DAC CODE



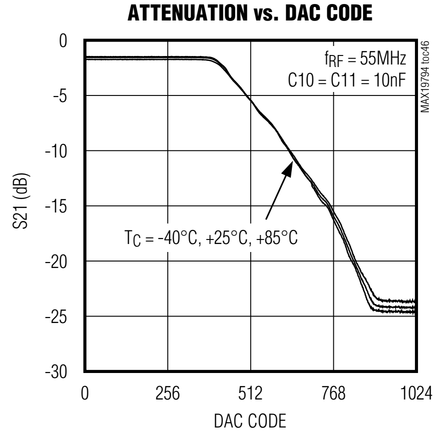
OUTPUT MATCH vs. DAC CODE



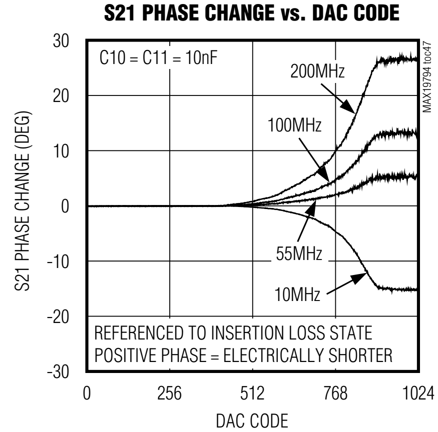
ATTENUATION vs. DAC CODE



ATTENUATION vs. DAC CODE



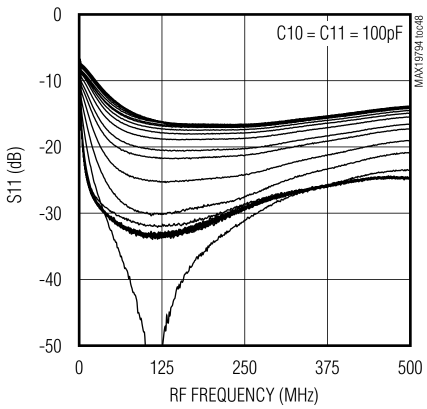
S21 PHASE CHANGE vs. DAC CODE



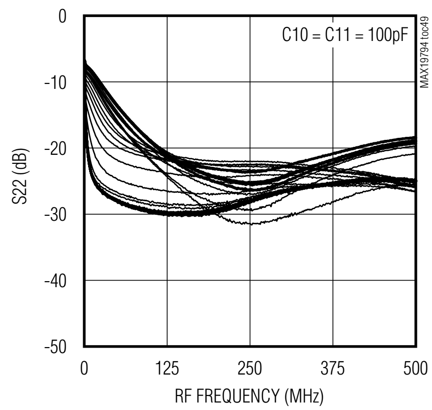
Typical Operating Characteristics (continued)

(Typical Application Circuit, **V_{CC} = 3.3V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

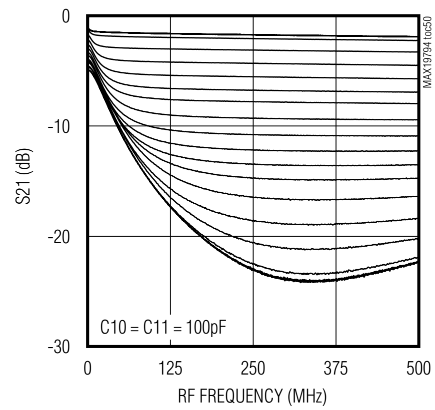
INPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



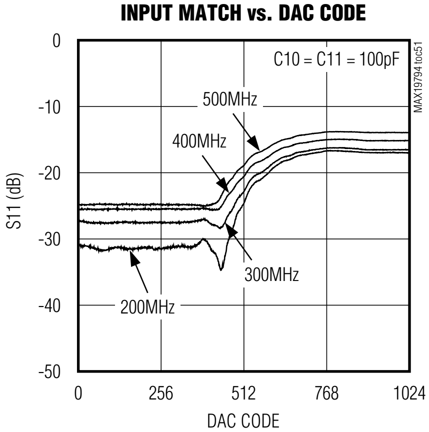
OUTPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



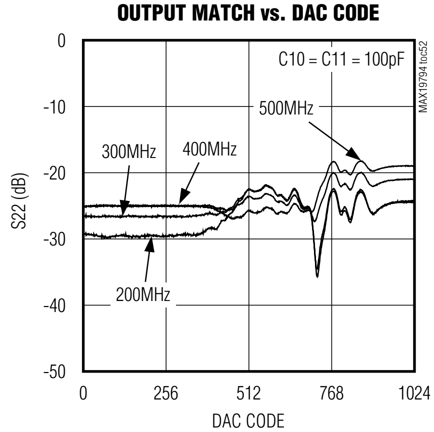
ATTENUATION vs. RF FREQUENCY OVER CODE SETTINGS



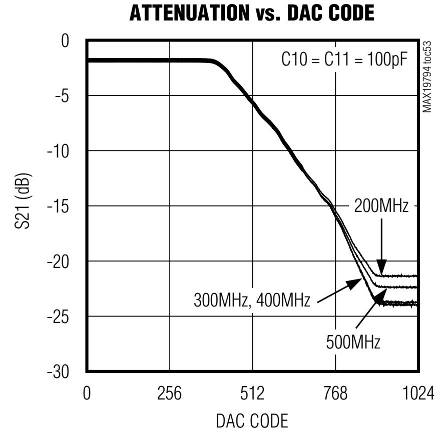
INPUT MATCH vs. DAC CODE



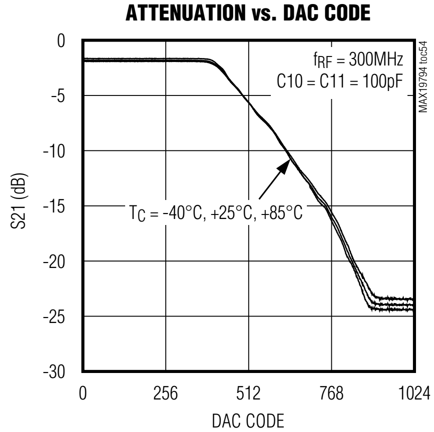
OUTPUT MATCH vs. DAC CODE



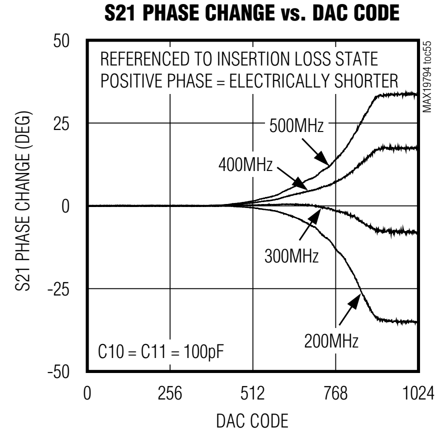
ATTENUATION vs. DAC CODE



ATTENUATION vs. DAC CODE



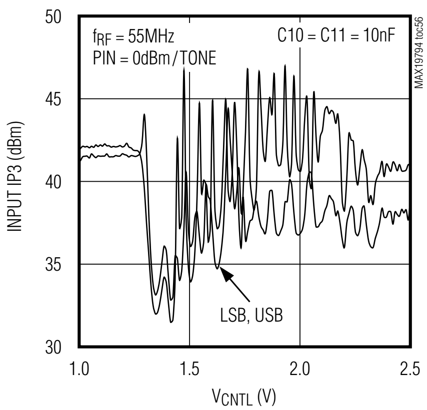
S21 PHASE CHANGE vs. DAC CODE



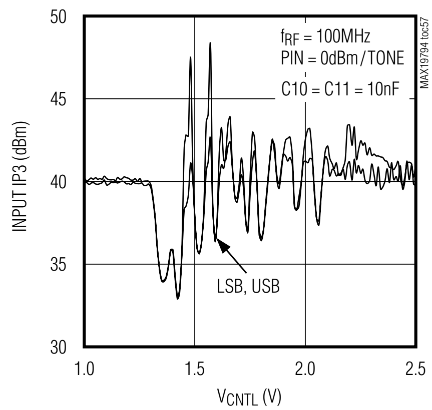
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 3.3V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

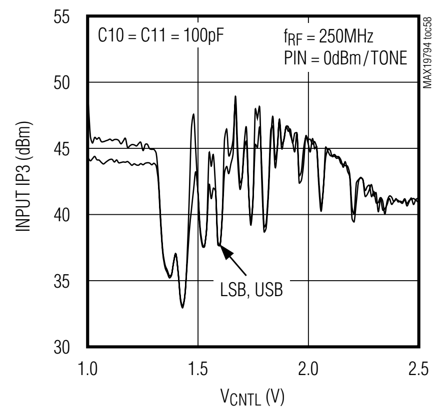
INPUT IP3 vs. V_{CNTL}



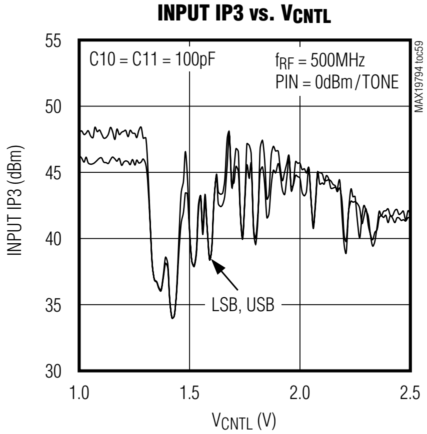
INPUT IP3 vs. V_{CNTL}



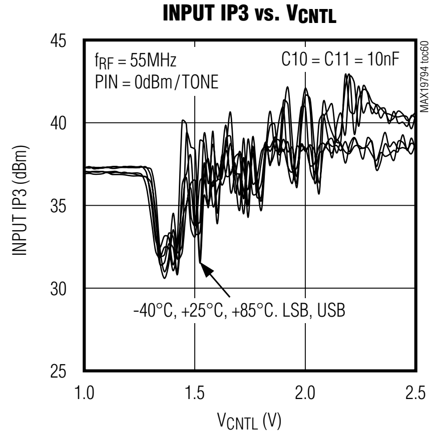
INPUT IP3 vs. V_{CNTL}



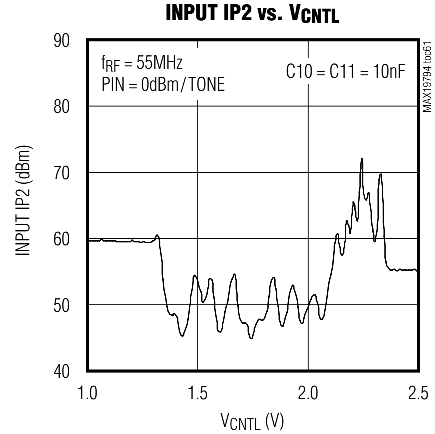
INPUT IP3 vs. V_{CNTL}



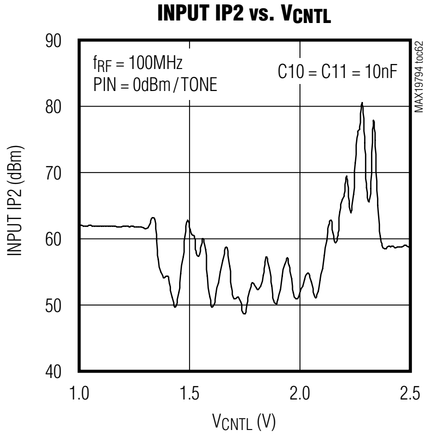
INPUT IP3 vs. V_{CNTL}



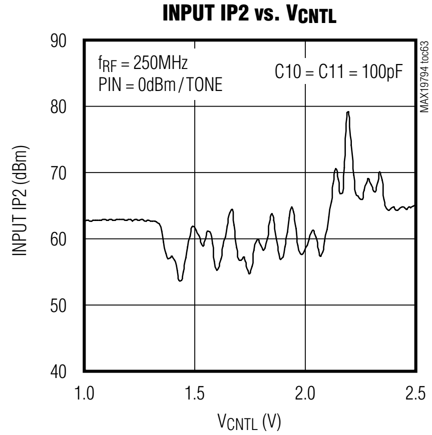
INPUT IP2 vs. V_{CNTL}



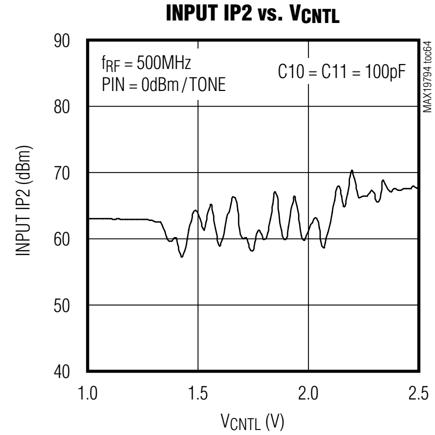
INPUT IP2 vs. V_{CNTL}



INPUT IP2 vs. V_{CNTL}



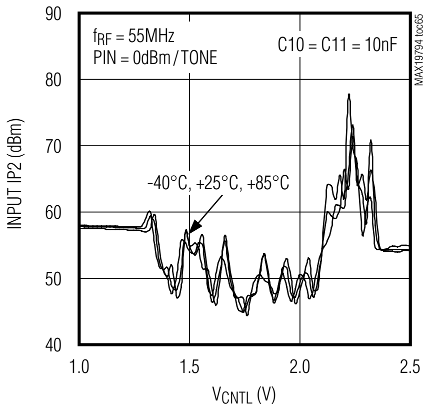
INPUT IP2 vs. V_{CNTL}



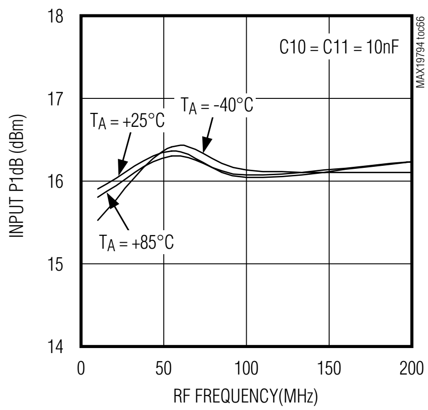
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CC} **= 3.3V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

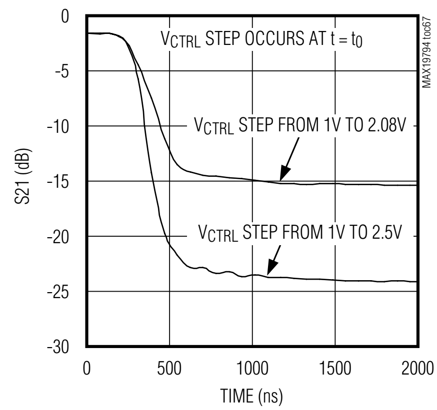
INPUT IP2 vs. V_{CNTL}



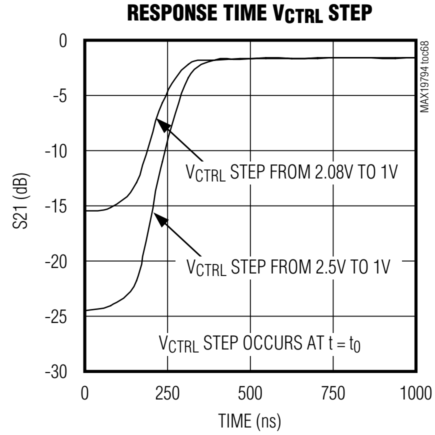
INPUT P1dB vs. RF FREQUENCY



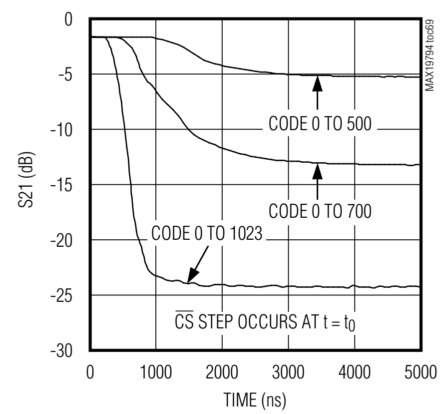
RESPONSE TIME V_{CTRL} STEP



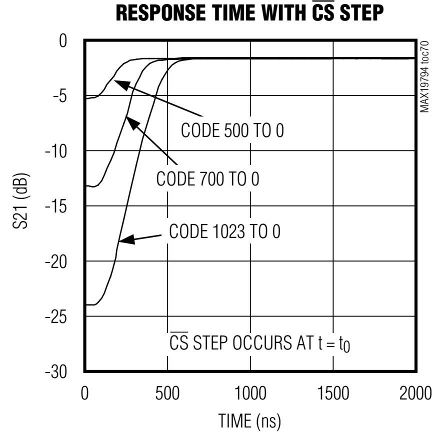
RESPONSE TIME V_{CTRL} STEP



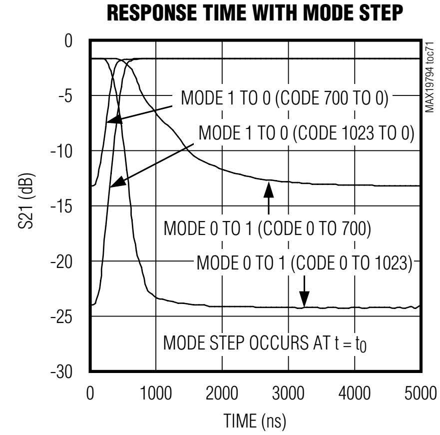
RESPONSE TIME WITH $\overline{CS}$ STEP



RESPONSE TIME WITH $\overline{CS}$ STEP

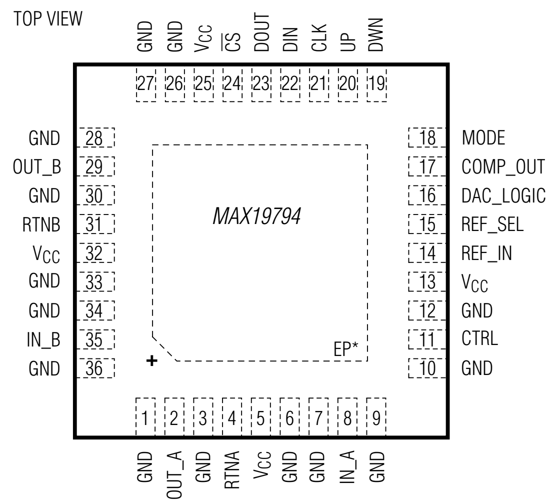


RESPONSE TIME WITH MODE STEP



10MHz to 500MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Pin Configuration



TQFN
6mm x 6mm

*INTERNALLY CONNECTED TO GND.

Pin Description

PIN	NAME	DESCRIPTION
1, 3, 6, 7, 9, 10, 12, 26, 27, 28, 30, 33, 34, 36	GND	Ground. Connect to the board's ground plane using low-inductance layout techniques.
2	OUT_A	Attenuator A RF Output. Internally matched to 50Ω over the operating frequency band. This pin, if used, requires a DC block. If this attenuator is not used, the pin can be left unconnected.
4, 31	RTNA, RTNB	Attenuator Ground Returns. These pins require a cap to ground and need to be placed close to each pin. This capacitor centers the RF band of operation. See the *Typical Operating Characteristics* section.
5	V_{CC}	Attentuator A Power Supply. Bypass to GND with a capacitor and a resistor as shown in the *Typical Application Circuit*.
8	IN_A	Attenuator A RF Input. Internally matched to 50Ω over the operating frequency band. This pin, if used, requires a DC block. If this attenuator is not used, the pin can be left unconnected.
11	CTRL	Attenuator Control Voltage Input. **Except in the test mode where no voltage can be applied to this pin.** V_{CC} must be present unless using a current-limiting resistor as noted in the *Applications Information* section.

Pin Description (continued)

PIN	NAME	DESCRIPTION
13	V_{CC}	Analog Supply Voltage. Bypass to GND with capacitor as close as possible to the device. See the *Typical Application Circuit*.
14	REF_IN	DAC Reference Voltage Input (Optional)
15	REF_SEL	DAC Reference Voltage Selection Logic Input Logic = 0 enable on-chip DAC reference. Logic = 1 use off-chip DAC reference (pin 14).
16	DAC_LOGIC	DAC Logic Control Input. See Table 1.
17	COMP_OUT	Comparator Logic OutputA 4.7pF capacitor could be used to reduce any potential rise time glitching when the comparator changes state.
18	MODE	Attenuator Control Mode Logic Input Logic = 1 enable attenuator step control. Logic = 0 enable attenuator SPI control.
19	DWN	Down Pulse Input Logic pulse = 0 for each step-down.
20	UP	Up Pulse Input Logic pulse = 0 for each step-up.
19, 20	DWN/UP	Logic = 0 to both pins to reset the attenuator to a minimum attenuation state
21	CLK	SPI Clock Input
22	DIN	SPI Data Input
23	DOUT	SPI Data Output
24	$\overline{CS}$	SPI Chip Selection Input
25	V_{CC}	Digital Supply Voltage. Bypass to GND with capacitor as close as possible to the device as possible. See the *Typical Application Circuit*.
29	OUT_B	Attenuator B RF Output. Internally matched to 50Ω over the operating frequency band. This pin, if used, requires a DC block. If this attenuator is not used, the pin can be left unconnected.
32	V_{CC}	Attenuator B Power Supply. Bypass to GND with capacitor and resistor as shown in the *Typical Application Circuit*.
35	IN_B	Attenuator B RF Input. Internally matched to 50Ω over the operating frequency band. This pin, if used, requires a DC block. If this attenuator is not used, the pin can be left unconnected.
—	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance. See the *Layout Considerations* section.

Detailed Description

The MAX19794 is a dual, general-purpose analog voltage variable attenuator (VVA) designed to interface with 50Ω systems operating in the 10MHz to 500MHz frequency range. Each attenuator provides 22.4dB of attenuation range with a linear control slope of 8dB/V. Both attenuators share a common analog control and can be cascaded together to yield 44.7dB of total dynamic range with a combined linear control slope of 16dB/V. Alternatively, the on-chip, 4-wire SPI-controlled 10-bit DAC can be used to control both attenuators. In addition, a step-up/down feature allows user-programmable attenuator stepping through command pulses without reprogramming the SPI interface.

Application Information

Attenuation Control and Features

The device has various states that are used to control the analog attenuator along with some monitoring conditions. The device can be controlled by an external control voltage, an internal SPI bus, or a combination of the two. The various states are described in Table 1. The SPI bus has multiple registers that are used to control the device when not configured for the analog only mode. For the cases where CTRL is used, the control range is 1V to 4V for V_{CC} = 5V, and is 1V to 2.5V for V_{CC} = 3.3V.

Up to 22.4dB of attenuation-control range is provided per attenuator. At the insertion-loss setting, the single attenuator's loss is approximately 1.5dB. If a larger attenuation-control range is desired, the second on-chip attenuator can be connected in series to provide an additional 22.4dB of gain-control range.

The on-chip control driver simultaneously adjusts both on-chip attenuators. It is suggested that a current-limiting resistor be included in series with CTRL to limit the input current to less than 40mA, should the control voltage be applied when V_{CC} is not present. A series resistor of greater than 200Ω provides complete protection for +5.0V control voltage ranges.

Analog Mode Only Control

In Table 1 state (0, 0), the attenuators are controlled using a voltage applied to the CTRL pin of the device and the on-chip DAC is disabled. In the case where none of the features of the SPI bus are needed, the part can be operated in a pure analog control mode by grounding pins 14 through 25.

DAC Mode Control

In Table 1 state (1, 0), the attenuators are controlled by the on chip 10-bit DAC register. See the Register/Mode section. In this condition, no signal is applied to the CTRL pin and the load on the CTRL pin should be >100kΩ. The DAC is set using the SPI loaded code in the registers along with the setting of the mode pin.

Analog Mode Control with Alarm Monitoring

In Table 1 state (0, 1), the attenuators are controlled using a voltage applied to the CTRL pin of the device. See Register/Mode section. In this condition, the DAC

Table 1. Attenuator Control Logic States

DAC_LOGIC	RDBK_EN (D9, REG3)	INTERNAL SWITCH STATES	ATTENUATOR	10-BIT DAC
0	0	S1 = closed S2, S3, S4 = open	Controlled by external analog voltage on CTRL (pin 11).	Disabled
1	0	S1, S3, S4 = open S2 = closed	Controlled by on-chip DAC. No voltage applied to pin 11.	Enabled
0	1	S1, S3, S4 = closed S2 = open	Controlled by external analog voltage on CTRL (pin 11). CTRL is compared with DAC output. Comparator drives COMP_OUT (pin 17).	Enabled (update DAC code to estimate CTRL voltage on pin 11)
1	1	S1, S2 = closed S3, S4 = open	Controlled by on-chip DAC. The DAC output is connected to pin 11. Use this state to test the DAC output. **In this condition, no voltage can be applied to pin 11 and the load on pin 11 must be > 100kΩ.**	Enabled

is enabled and a voltage is also applied to CTRL (pin 11). The on-chip switches are set to compare the DAC voltage to the CTRL voltage at the comparator input, and the output of the comparator COMP_OUT trips from high to low when the CTRL exceeds the on-chip DAC voltage.

DAC Test Mode

In Table 1 state (1, 1), the attenuators are controlled by the on chip 10-bit DAC register. See *Register MODE UP/DWN Operation* section. In this condition, the DAC is enabled and the DAC voltage appears at the CTRL pin. In this condition, no signal can be applied to the CTRL pin and the load on the CTRL pin should be > 100kΩ. This mode is used only in production testing of the DAC voltage and is not recommended for customer use.

Register MODE UP/DWN Operation

The device uses four 13-bit registers for the operation of the device. The first bit is the read/write bit,the following two are address bits, while the remaining 10 are the desired data bits. The read/write bit determines whether the register is being written to or read from. The next two address bits select the desired register to write or read from. These address bits can be seen in Table 2. Table 3 describes the contents of the four registers.

Figure 1 shows the configuration of the internal registers of the device, and Figure 2 shows the timing of the SPI bus. Register 0 is used to set the DAC code to the desired value, register 1 selects the step-up code, and register 2 selects the step-down code.

The part also contains a MODE control pin (Table 4), along with UP and DWN controls(Table 5). When MODE is 0, the contents of register 0 get loaded into the 10-bit DAC register and set the value of the on-chip DAC. In this condition, the UP and DWN control pins have no effect on the part. In MODE 1, the effective DAC code fed to the 10-bit DAC register is equal to:

$$m \times \text{Register 1} - n \times \text{Register 2}$$

where m and n are the number of UP and DWN control steps accumulated, respectively.

After powering up the part, UP and DWN should both be set to 0 to reset the m and n counters to be 0. This results in a 10-bit all 0 code out of the mathematical block in Figure 1. This is applied to the 10-bit DAC register that drives the DAC. To increase (decrease) the code using the UP (DWN) pin, the DWN (UP) pin must be high and the UP (DWN) pin should be pulsed low to high. The part is designed to produce no wraparounds when using UP and DWN stepping, so the DAC code maxes out at 1023 or goes no lower than 0. See Figure 3 for the UP and DWN control operation.

Switching back to MODE 0 produces the same 10-bit DAC code as was previously loaded into register 0. Switching back to MODE = 1 results in the previous 10-bit DAC code from the register 1 and 2 combiner/multiplier block.

Register 3 is used to set the RDBK_EN register in the write mode and is used to read back the RDBK_EN register and COMP_OUT in the read mode.

SPI Interface

The device can be controlled with a 4-wire SPI-compatible serial interface. Figure 2 shows a timing diagram for the interface. In the write mode, a 13-bit word is loaded into the device through the DIN pin with $\overline{CS}$ set low. The first bit of the word in the write mode is 0, and the next two bits select the register to be written to. See Table 2. The next 10 bits contain the data to be written to the selected register. After the 13 bits are shifted in, a low to high $\overline{CS}$ command is applied and this latches the 10 bits into the selected register. The entire write command is ignored if $\overline{CS}$ is pulsed low to high before the last data bit is successfully captured.

For the read cycle, the first bit clocked in is a 1 and this establishes that a register is to be read. The next two clocked bits form the address of the register to be read. See Table 2. In this read mode, data starts to get clocked out of the DOUT pin after A0 is captured. The DOUT pin goes to a high-impedance state after the 10 bits are transmitted, or if $\overline{CS}$ goes high at any point in time during the transmission.

Voltage Reference

The device has an on-chip voltage reference for the DAC and also has a provision to operate with an off-chip reference. Table 6 provides details in selecting the desired reference.

Table 2. Component Suppliers

R/W	A1	A0	DESCRIPTION
0	0	0	Write to register 0 using DIN
0	0	1	Write to register 1 using DIN
0	1	0	Write to register 2 using DIN
0	1	1	Write to register 3 using DIN
1	0	0	Read from register 0 using DOUT
1	0	1	Read from register 1 using DOUT
1	1	0	Read from register 2 using DOUT
1	1	1	Read from register 3 using DOUT

Table 3. Register Definitions

Register 0 (Read/Write 10-Bit DAC Code)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DAC MSB									DAC LSB

Register 1 (Read/Write 10-Bit Step-Up Code)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Step-up MSB									Step-up LSB

Register 2 (Read/Write 10-Bit Step-Down Code)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Step-down MSB									Step-down LSB

Register 3 Write Bits

RDBK_EN= Enable bit for voltage comparator that drives COMP_OUT (pin 17).

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDBK_EN	Not used, set = 0								

Register 3 Read Bits

RDBK_EN= Enable bit for voltage comparator that drives COMP_OUT (pin 17),

COMP_OUT=Read Logic level of COMP_OUT (pin 17).

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDBK_EN	COMP_OUT	Not used, set = 0							

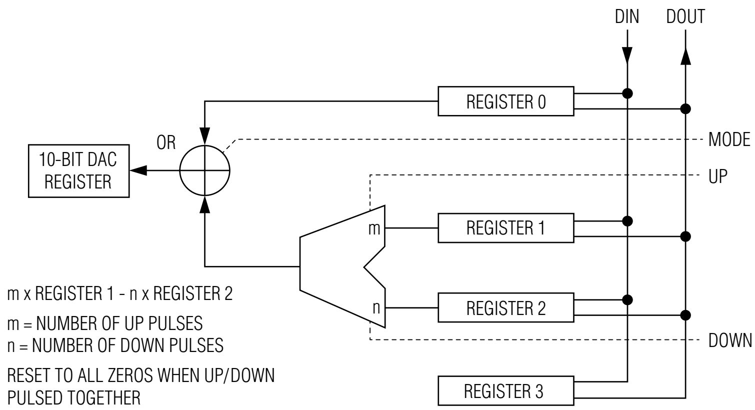


Figure 1. Register Configuration Diagram

Table 4. Attenuator Control Mode Logic State

MODE (PIN 17)	ATTENUATOR
0	SPI Control Mode (DAC code is located in register 0)
1	Step Control Mode using UP and DWN pins. The step-up code is located in register 1 and step-down code in register 2).

Table 5. Step Mode Logic State (MODE = 1)

UP	DWN	ATTENUATOR
Logic 0	Logic 0	Reset DAC for minimum attenuation state (DAC code = 0000000000).
Logic 0 Pulse	Logic 1	Increase DAC code* by amount located in register 1. UP pulsed from high to low to high (Figure 3).
Logic 1	Logic 0 Pulse	Decrease DAC code* by amount located in register 2. DWN pulsed from high to low to high (Figure 3).

**Continued up or down stepping results in saturation (no code wrapping).*

Table 6. REF_SEL Logic State

REF_SEL	DAC REFERENCE
0	Uses on-chip DAC reference.
1	User provides off-chip DAC reference voltage on REF_IN (pin 14).

SPI Interface Programming

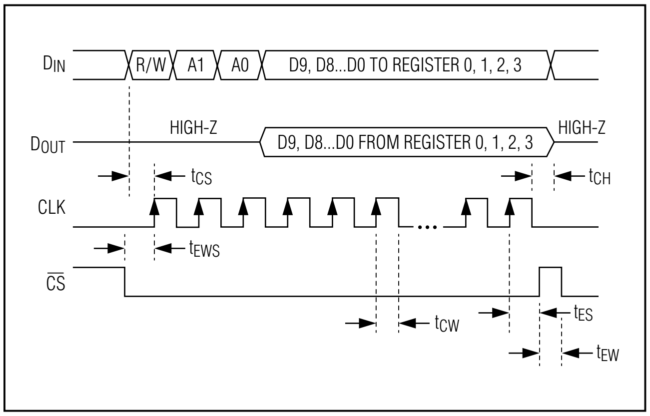


Figure 2. SPI Timing Diagram

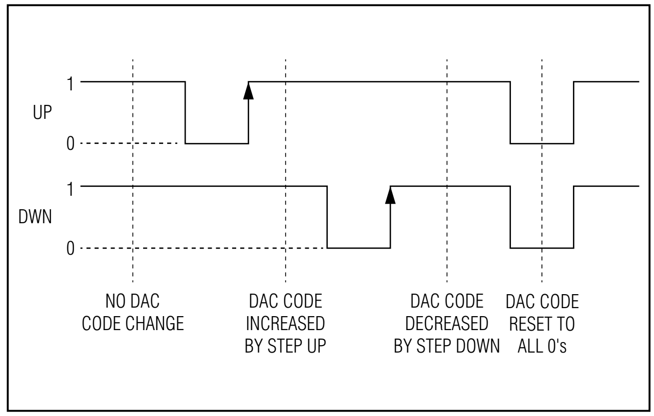


Figure 3. UP DWN Control Diagram (Mode = 1)

Table 7. Typical Application Circuit Component Values

DESIGNATION	QTY	DESCRIPTION	
C1, C2, C4	3	0.01µF ±5% 50V X7R ceramic capacitors (0402).	
C3	0	Not installed for two attenuators in cascade	
C5–C9	5	1000pF ±5% 50V COG ceramic capacitors (0402)	
C10, C11	2	10MHz to 200MHz	0.01µF ±10% 50V X7R ceramic capacitors (0402)
		250MHz to 500MHz	100pF ±5% 50V COG ceramic capacitors (0402)
C12	1	120pF ±5% 50V COG CER CAP (0402).Provides some external noise filtering along with R3.	
C13	0	Not installed. A 4.7pF capacitor could be used to reduce any potential rise time glitching when the comparator changes state.	
R1*, R2*	2	10Ω ±5% resistor (0402)	
R3	1	200Ω ±5% resistor (0402). This resistor is used to provide some lowpass noise filtering when used with C12. The value of R3 slows down the response time. R3 also provides protection for the device in case V_{CTRL} is applied without V_{CC} present.	
U1	1	MAX19794	

**Add 2 additional 10Ω resistors between the V_{CC} pins leading to C5 and C6 unless a V_{CC} power plane is used.*

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For best performance, route the ground-pin traces directly to the exposed pad underneath the package. This pad must be connected to the ground plane of the board by using multiple vias under the device to provide the best RF and thermal conduction path. Solder the exposed pad on the bottom of the device package to a PCB.

RF Ground Return Capacitors

The device requires RF ground return capacitors C10 and C11. The value of these capacitors optimize the dynamic range and frequency flatness for the RF band of interest. Some recommended values are shown in Table 7 along with the resulting performance in the *Typical Operating Characteristics* section.

Power-Supply Bypassing

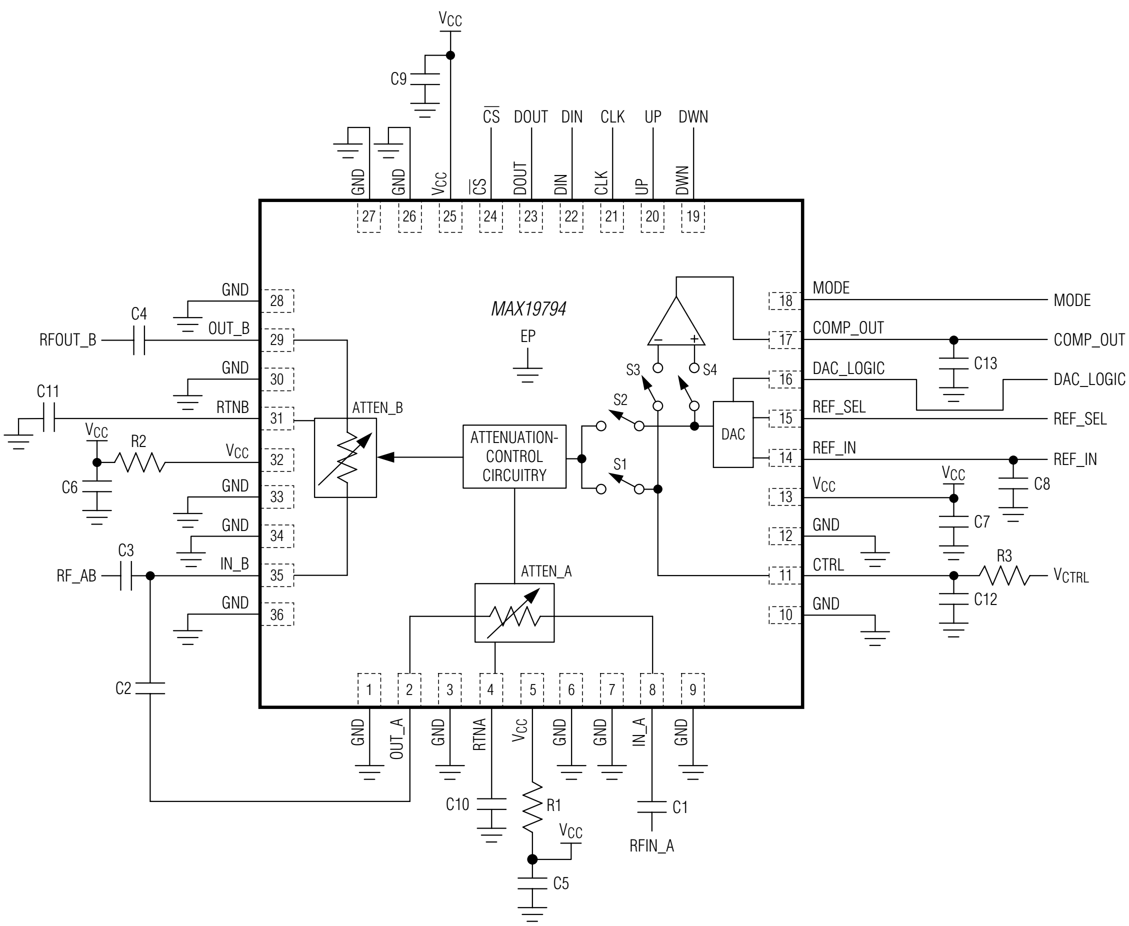
Proper voltage-supply bypassing is essential for high frequency circuit stability. Bypass each V_{CC} pin with capacitors placed as close as possible to the device. Place the smallest capacitor closest to the device. See the *Typical Application Circuit* and Table 7 for details.

Exposed Pad RF and Thermal Considerations

The exposed pad (EP) of the device's 36-pin TQFN package provides a low thermal-resistance path to the die. It is important that the PCB on which the device is mounted to conduct heat from this contact. In addition, provide the EP with a low-inductance RF ground path for the device.

The EP must be soldered to a ground plane on the PCB, either directly or through an array of plated via holes. Soldering the pad to ground is also critical for efficient heat transfer. Use a solid ground plane wherever possible.

Typical Application Circuit



NOTE: FOR ATTENUATOR A ONLY CONFIGURATION, REMOVE C3 AND MOVE C2 DIAGONALLY TO CONNECT PIN 2 TO THE OUTPUT CONNECTION RF_AB.
FOR ATTENUATOR B ONLY CONFIGURATION, REMOVE C2.
FOR CASCADED CONFIGURATION, REMOVE C3 AND USE C2 TO CONNECT OUT_A TO IN_B.

10MHz to 500MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX19794ETX+	-40°C to +100°C	36 TQFN-EP*
MAX19794ETX+T	-40°C to +100°C	36 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
36 TQFN	T3666+2	**21-0141**	**90-0049**

10MHz to 500MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/12	Initial release	—
1	5/15	Removed military reference from *Applications*	1