

HD74HCT563, HD74HCT573

Octal Transparent Latches (with 3-state outputs)

REJ03D0669-0200
(Previous ADE-205-559)
Rev.2.00
Mar 30, 2006

Description

When the latch enable (LE) input is high, the Q outputs of HD74HCT563 will follow the inversion of the D inputs and the Q outputs of HD74HCT573 will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (Data to Q, $\bar{Q}$) = 13 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: $1 \mu A$ max
- Low Quiescent Supply Current: I_{CC} (static) = $4 \mu A$ max ($T_a = 25^\circ C$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HCT573P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74HCT563FPEL HD74HCT573FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HCT563RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)
HD74HCT573TELL	TSSOP-20 pin	PTSP0020JB-A (TTP-20DAV)	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

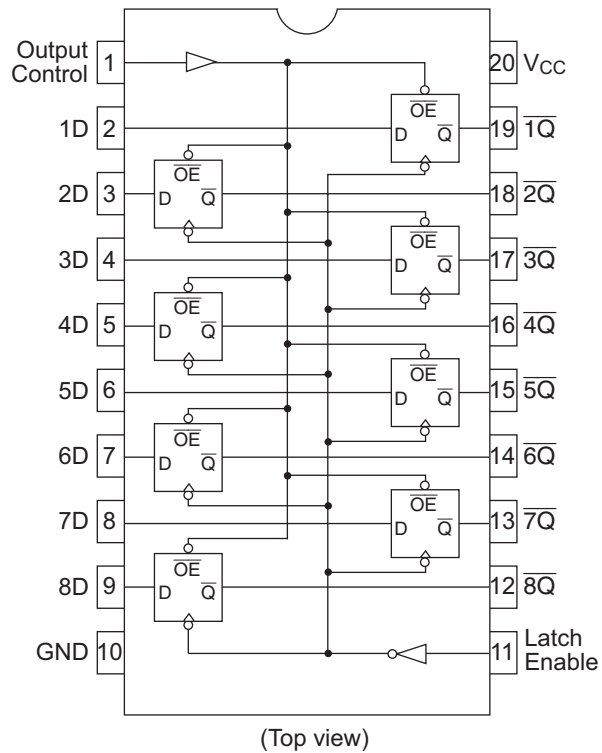
Inputs			Outputs	
Output Control	Latch Enable	Data	HD74HCT563	HD74HCT573
L	H	H	L	H
L	H	L	H	L
L	L	X	Q_0	Q_0
H	X	X	Z	Z

Q_0 : level of Q before the indicated Steady-state input conditions were established.

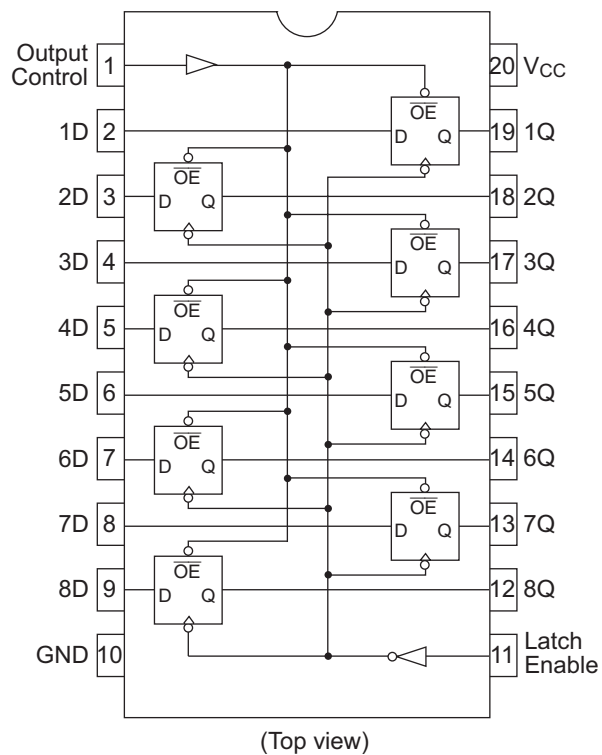
$\bar{Q}_0$: complement of Q_0 or level of $\bar{Q}$ before the indicated Steady-state input conditions were established.

Pin Arrangement

HD74HCT563

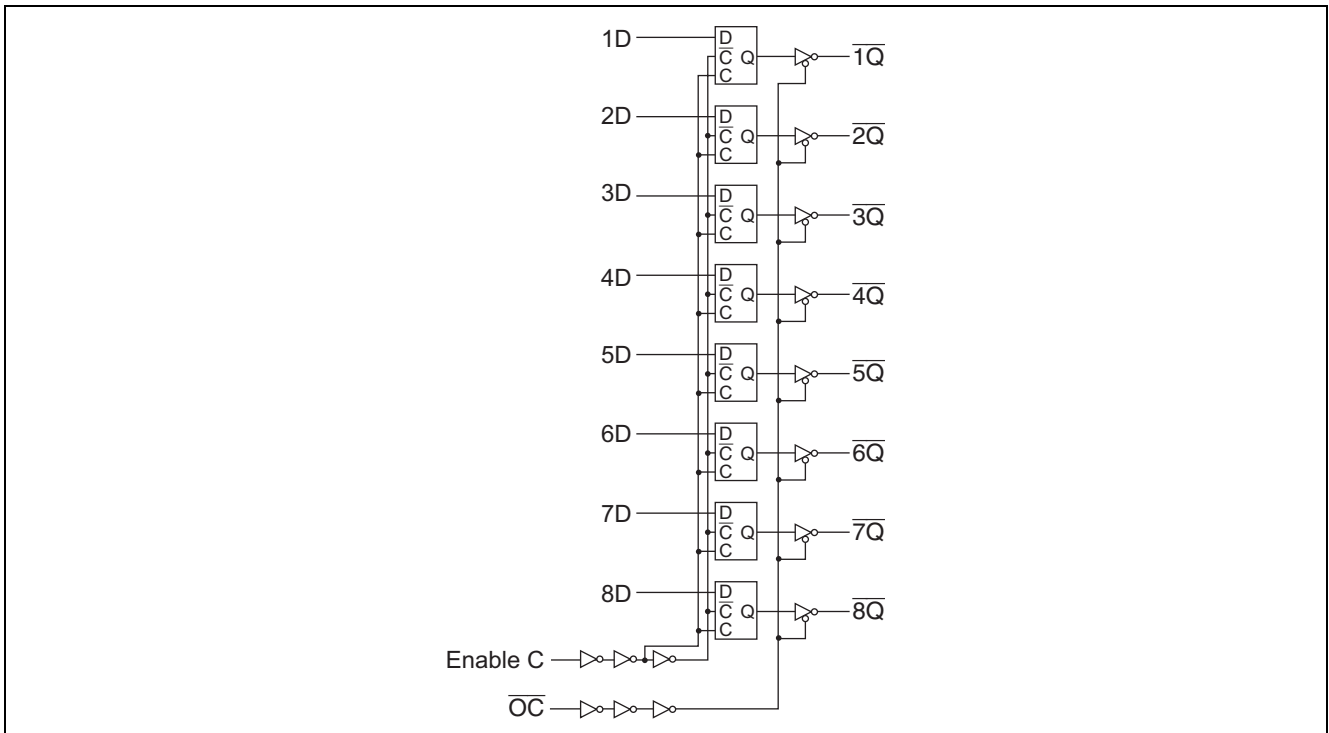


HD74HCT573

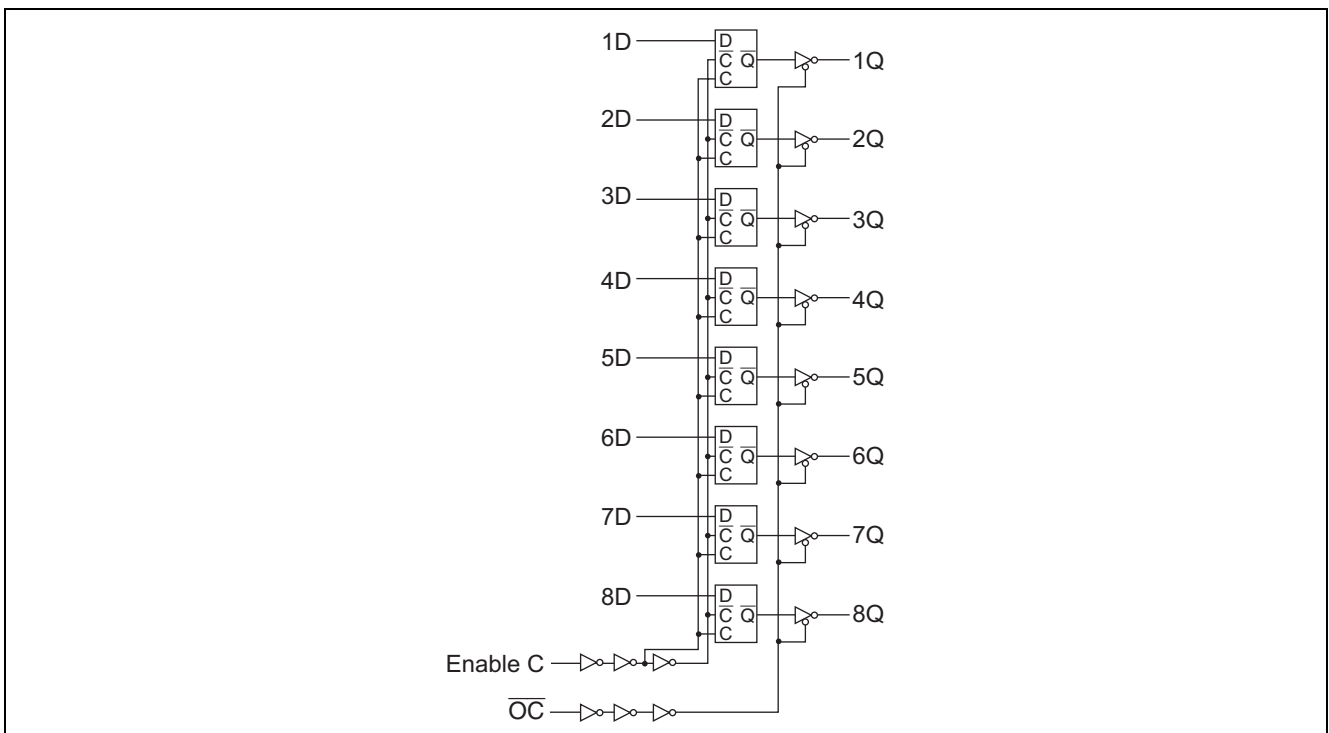


Logic Diagram

HD74HCT563



HD74HCT573



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	Tstg	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	4.5 to 5.5	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 500	ns	$V_{CC} = 4.5$ V

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

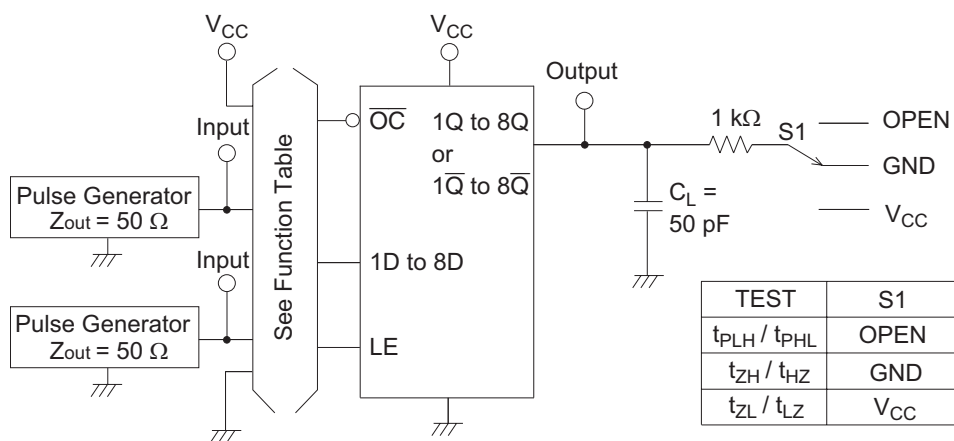
Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	—	2.0	—	V		
	V_{IL}	4.5 to 5.5	—	—	0.8	—	0.8	V		
Output voltage	V_{OH}	4.5	4.4	—	—	4.4	—	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu A$
		4.5	4.18	—	—	4.13	—			$I_{OH} = -6 \text{ mA}$
	V_{OL}	4.5	—	—	0.1	—	0.1	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu A$
		4.5	—	—	0.26	—	0.33			$I_{OL} = 6 \text{ mA}$
Off-state output current	I_{OZ}	5.5	—	—	± 0.5	—	± 5.0	μA	$V_{in} = V_{IH}$ or V_{IL} , $V_{out} = V_{CC}$ or GND	
Input current	I_{in}	5.5	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}$ or GND	
Quiescent current	I_{CC}	5.5	—	—	4.0	—	40	μA	$V_{in} = V_{CC}$ or GND, $I_{out} = 0 \mu A$	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

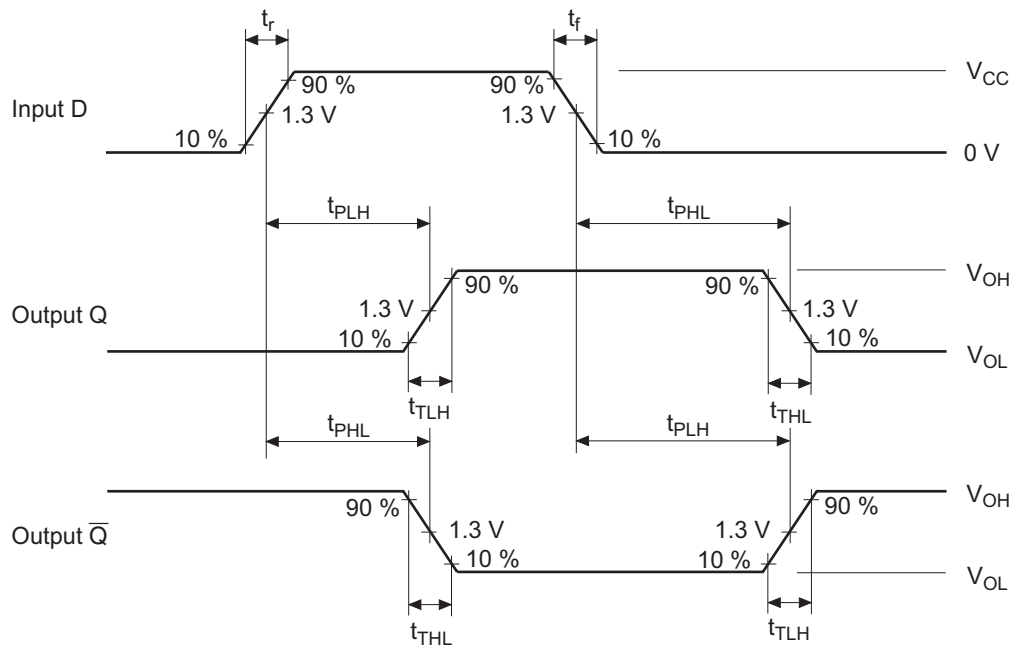
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	t _{PLH}	4.5	—	13	22	—	28	ns	Data to Q, $\overline{Q}$
	t _{PHL}	4.5	—	13	22	—	28		
	t _{PLH}	4.5	—	14	23	—	29	ns	Enable G to Q, $\overline{Q}$
	t _{PHL}	4.5	—	14	23	—	29		
Output enable time	t _{ZL}	4.5	—	14	30	—	38	ns	
	t _{ZH}	4.5	—	15	30	—	38		
Output disable time	t _{LZ}	4.5	—	16	30	—	38	ns	
	t _{HZ}	4.5	—	17	30	—	38		
Setup time	t _{su}	4.5	15	3	—	19	—	ns	
Hold time	t _h	4.5	5	-1	—	5	—	ns	
Pulse width	t _w	4.5	16	4	—	20	—	ns	
Output rise/fall time	t _{TLH}	4.5	—	4	12	—	15	ns	
	t _{THL}	4.5	—	4	12	—	15		
Input capacitance	C _{in}	—	—	5	10	—	10	pF	

Test Circuit

Note : 1. C_L includes probe and jig capacitance.

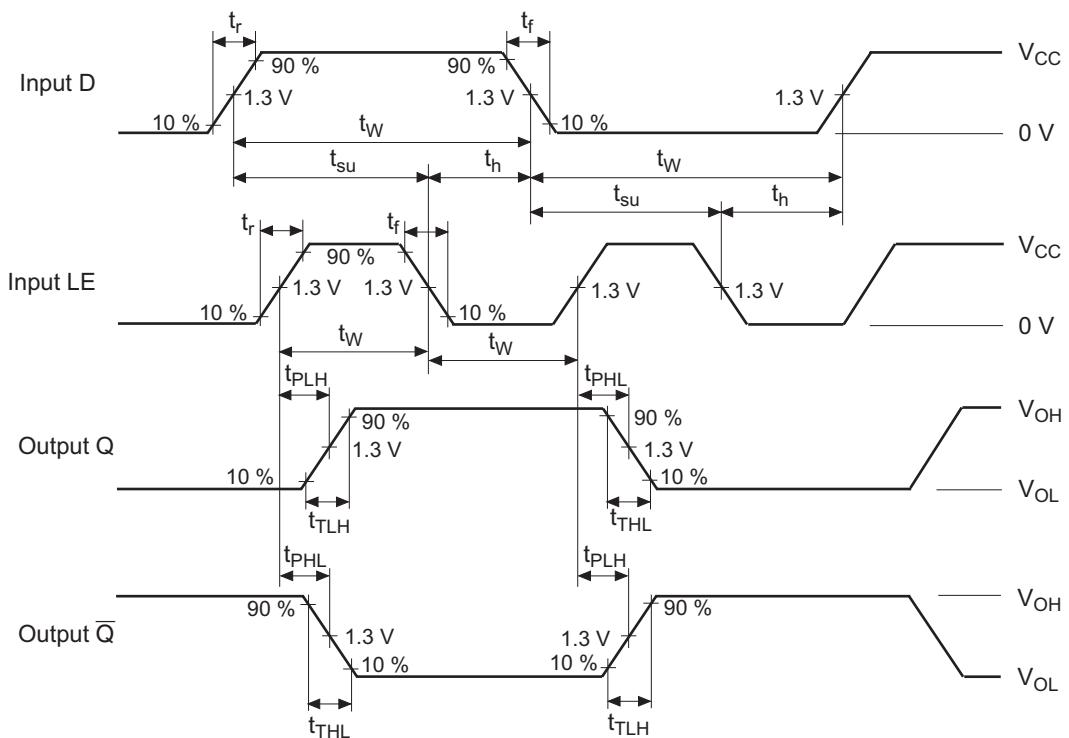
Waveforms

• Waveform – 1



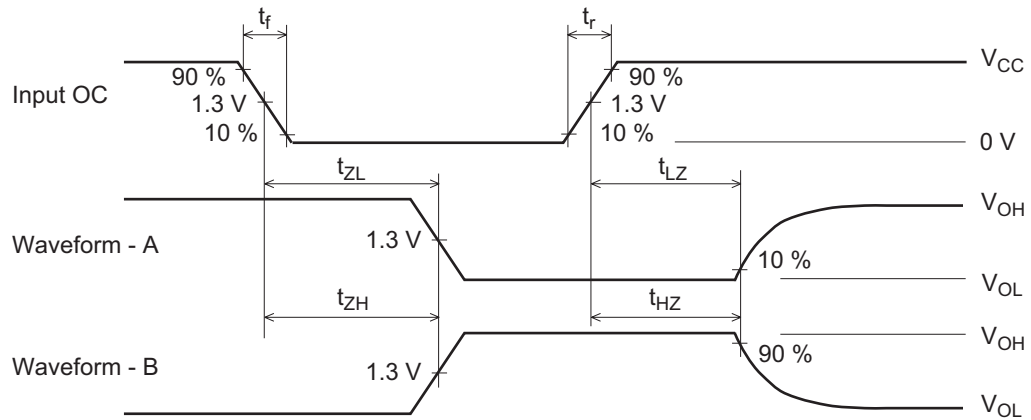
Notes : 1. Input waveform : $PRR \leq 1$ MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

• Waveform – 2



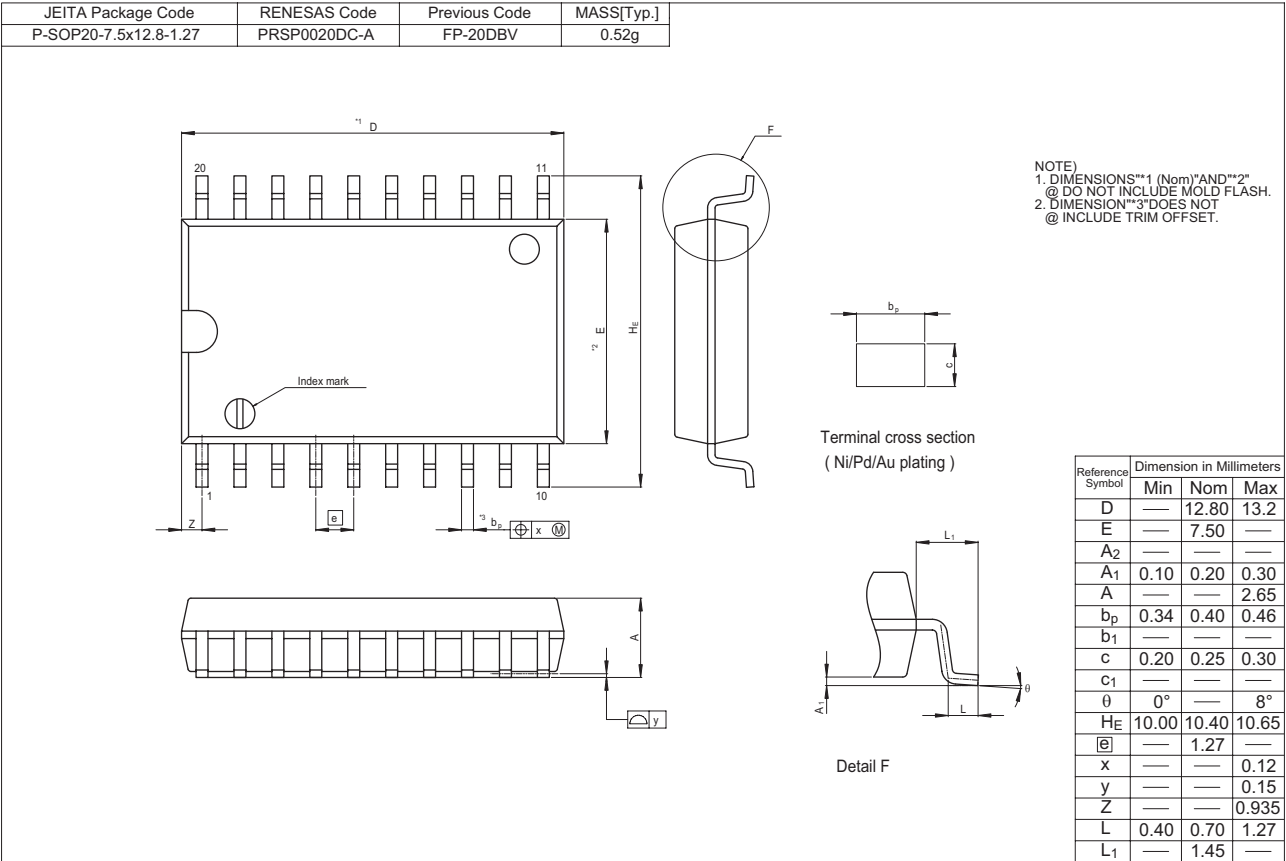
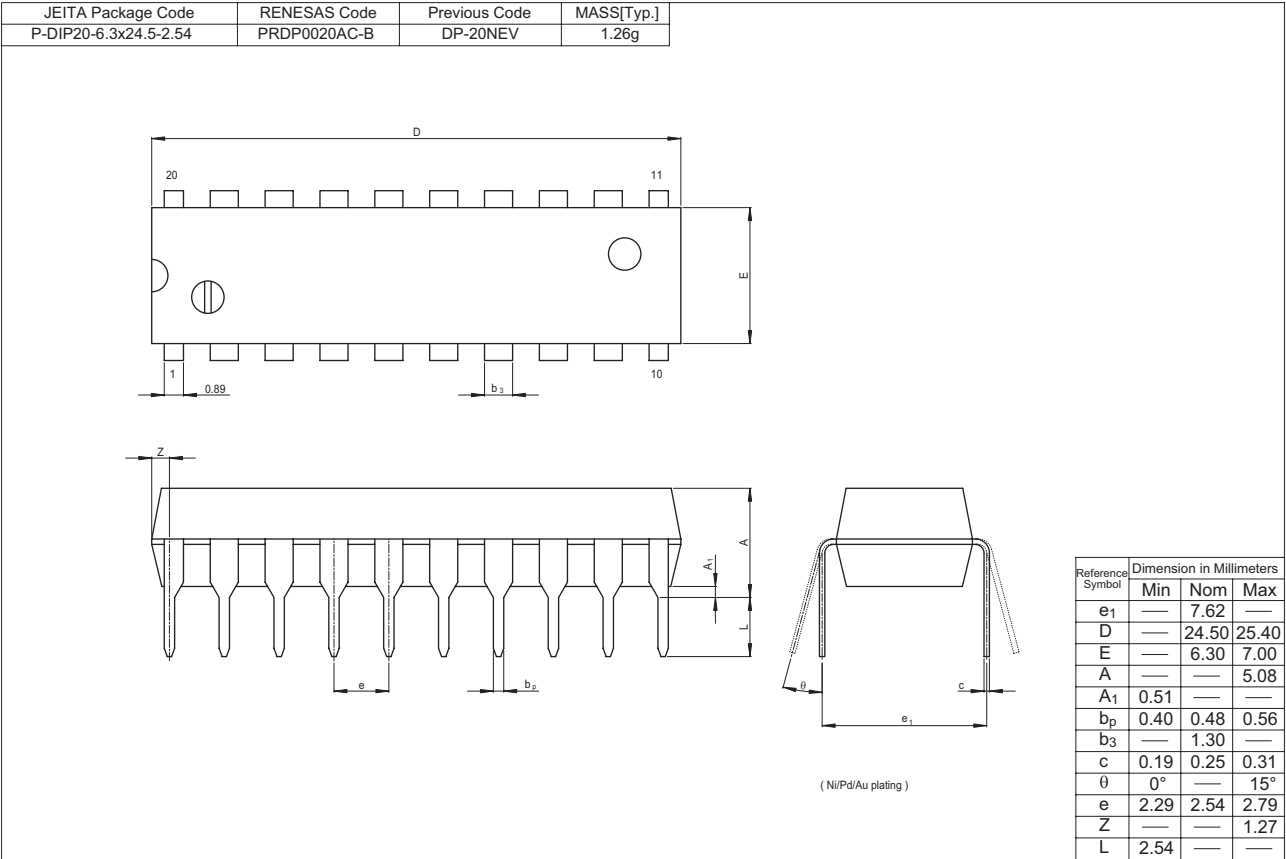
Notes : 1. Input waveform : $PRR \leq 1$ MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

• Waveform – 3



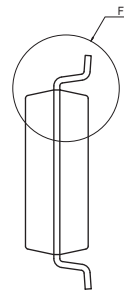
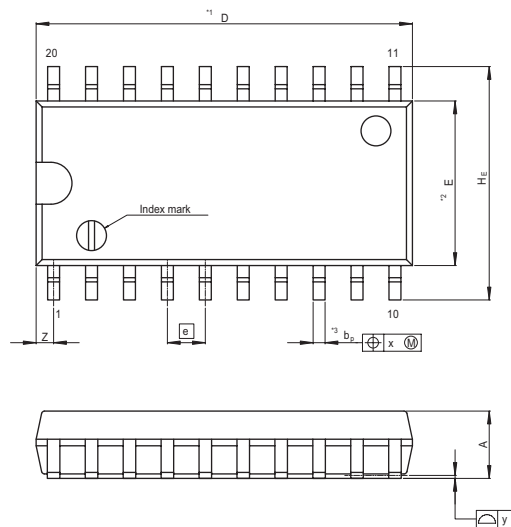
- Notes :
1. Input waveform : $PRR \leq 1 \text{ MHz}$, duty cycle 50%, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. Waveform– A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform– B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

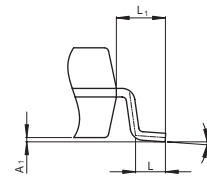
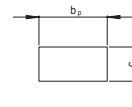


HD74HCT563, HD74HCT573

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.5x12.6-1.27	PRSP0020DD-B	FP-20DAV	0.31g



Terminal cross section
(Ni/Pd/Au plating)

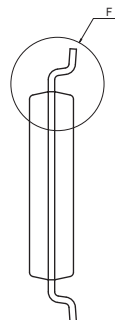
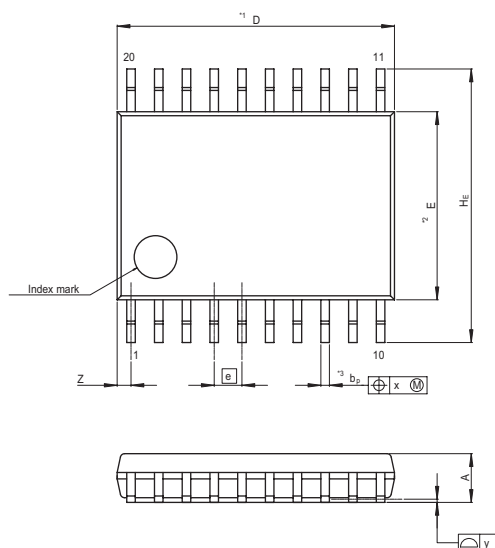


Detail F

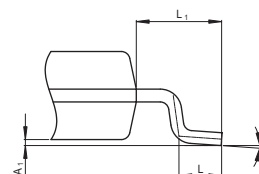
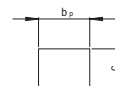
NOTE)
1. DIMENSIONS""1 (Nom)""AND""2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION""3""DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.60	13.0
E	—	5.50	—
A ₂	—	—	—
A ₁	0.00	0.10	0.20
A	—	—	2.20
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	7.50	7.80	8.00
@	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L ₁	—	1.15	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP20-4.4x6.5-0.65	PTSP0020JB-A	TTP-20DAV	0.07g



Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS""1 (Nom)""AND""2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION""3""DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.50	6.80
E	—	4.40	—
A ₂	—	—	—
A ₁	0.03	0.07	0.10
A	—	—	1.10
b _p	0.15	0.20	0.25
b ₁	—	—	—
c	0.10	0.15	0.20
c ₁	—	—	—
θ	0°	—	8°
H _E	6.20	6.40	6.60
⓪	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L ₁	—	1.0	—

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Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

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7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
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Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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