

Low Input Offset, High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

The MC33282/284 series of high performance operational amplifiers are quality fabricated with innovative bipolar and JFET design concepts. This dual and quad amplifier series incorporates JFET inputs along with a patented ZIP R TRIM™ element for input offset voltage reduction. These devices exhibit low input offset voltage, low input bias current, high gain bandwidth and high slew rate. Dual-doublet frequency compensation is incorporated to produce high quality phase/gain performance. In addition, the MC33282/284 series exhibit low input noise characteristics for JFET input amplifiers. Its all NPN output stage exhibits no deadband crossover distortion and a large output voltage swing. They also provide a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33282/284 series are specified over -40° to $+85^{\circ}\text{C}$ and are available in plastic DIP and SOIC surface mount packages.

- Low Input Offset Voltage: Trimmed to 200 μV
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 6.0 pA
- High Input Resistance: $10^{12} \Omega$
- Low Noise: 18 nV $\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Products: 35 MHz @ 100 kHz
- High Slew Rate: 15 V/ μs
- Power Bandwidth: 175 kHz
- Unity Gain Stable: w/Capacitance Loads to 300 pF
- Large Output Voltage Swing: +14.1 V/-14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Dual Supply Operation: $\pm 2.5 \text{ V}$ to $\pm 18 \text{ V}$ (Max)

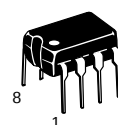
ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Dual	MC33282D	$T_A = -40^{\circ}$ to $+85^{\circ}\text{C}$	SOP-8
	MC33282P		Plastic DIP
Quad	MC33284D		SO-14
	MC33284P		Plastic DIP

MC33282 MC33284

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA



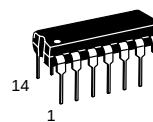
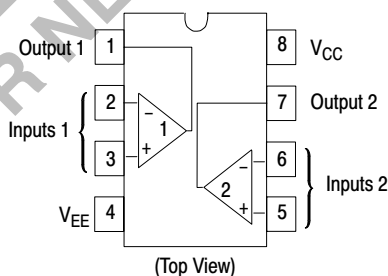
DUAL

P SUFFIX
PLASTIC PACKAGE
CASE 626



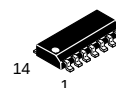
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



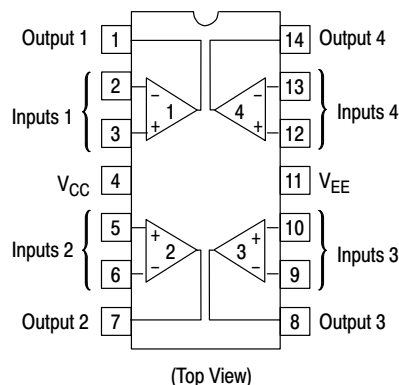
QUAD

P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	– 60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE} .
 2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Figure	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\ \Omega$, $V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	$ V_{IO} $	3	— —	0.2 —	2.0 4.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$, $V_{CM} = 0$ V, $V_O = 0$ V, $T_A = T_{low}$ to T_{high}	$ \Delta V_{IO} /\Delta T$	3	—	15	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	I_{IB}	4, 5	–200 –2.0	30 —	200 2.0	pA nA
Input Offset Current ($V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	I_{IO}		–100 –1.0	6.0 —	100 1.0	pA nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0$ mV, $V_O = 0$ V)	V_{ICR}	6	–11 —	–12 +14	— +11	V
Large Signal Voltage Gain ($V_O = \pm 10$ V, $R_L = 2.0$ k Ω) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	A_{VOL}	7	50 25	200 —	— —	V/mV
Output Voltage Swing ($V_{ID} = \pm 1.0$ V) $R_L = 2.0$ k Ω $R_L = 2.0$ k Ω $R_L = 10$ k Ω $R_L = 10$ k Ω	V_{O+} V_{O-} V_{O+} V_{O-}	8, 9, 10	13.2 — 13.7 —	+13.7 –13.9 +14.1 –14.6	— –13.2 — –14.3	V
Common Mode Rejection ($V_{in} = \pm 11$ V)	CMR	11	70	90	—	dB
Power Supply Rejection $V_{CC}/V_{EE} = +15$ V/–15 V, +5.0 V/–15 V, +15 V/–5.0 V	PSR	12	75	100	—	dB
Output Short Circuit Current ($V_{ID} = 1.0$ V, output to ground) Source Sink	I_{SC}	13, 14	15 —	+21 –27	— –15	mA
Power Supply Current ($V_O = 0$ V, per amplifier) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	I_D	15	— —	2.15 —	2.75 3.0	mA

MC33282 MC33284

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Figure	Min	Typ	Unit
Slew Rate ($V_{in} = -10\text{ V to } +10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0$)	SR	16, 28, 29	8.0	15	$\text{V}/\mu\text{s}$
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	17	20	35	MHz
AC Voltage Gain ($R_L = 2.0\text{ k}\Omega$, $V_O = 0\text{ V}$, $f = 20\text{ kHz}$)	A_{VO}	18, 21	—	1750	V/V
Unity Gain Frequency (Open Loop)	f_U		—	5.5	MHz
Gain Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	A_m	19, 20	—	15	dB
Phase Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	ϕ_m	19, 20	—	40	Degrees
Channel Separation ($f = 20\text{ Hz to } 20\text{ kHz}$)	CS	22	—	-120	dB
Power Bandwidth ($V_O = 20\text{ V}_{pp}$, $R_L = 2.0\text{ k}\Omega$, $\text{THD} \leq 1.0\%$)	BW_P		—	175	kHz
Distortion ($R_L = 2.0\text{ k}\Omega$, $f = 20\text{ Hz to } 20\text{ kHz}$, $V_O = 3.0\text{ V}_{rms}$, $A_V = +1.0$)	THD	23	—	0.003	%
Open Loop Output Impedance ($V_O = 0\text{ V}$, $f = 9.0\text{ MHz}$)	$ Z_O $	24	—	37	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)	R_{in}		—	10^{12}	Ω
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)	C_{in}		—	5.0	pF
Equivalent Input Noise Voltage ($R_S = 100\text{ }\Omega$, $f = 1.0\text{ kHz}$)	e_n	25	—	18	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	i_n		—	0.01	$\text{pA}/\sqrt{\text{Hz}}$

Figure 1. Equivalent Circuit Schematic
(Each Amplifier)

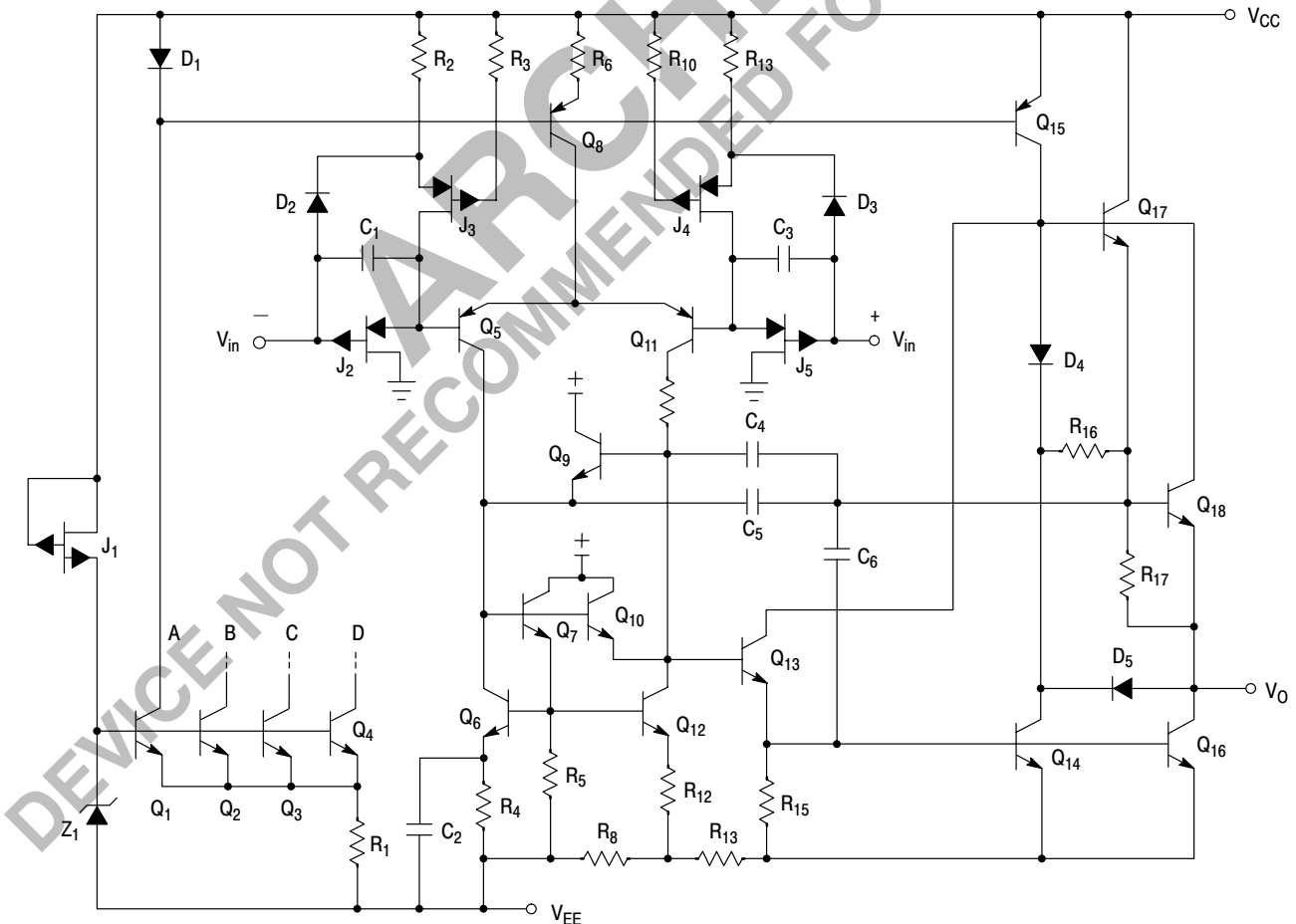


Figure 2. Maximum Power Dissipation versus Temperature

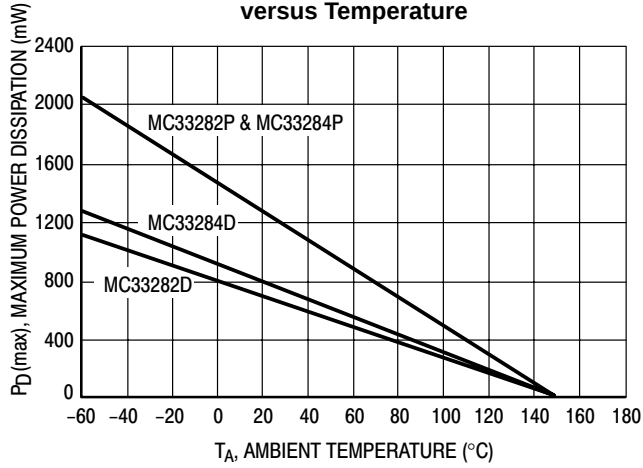


Figure 3. Input Offset Voltage versus Temperature for Typical Units

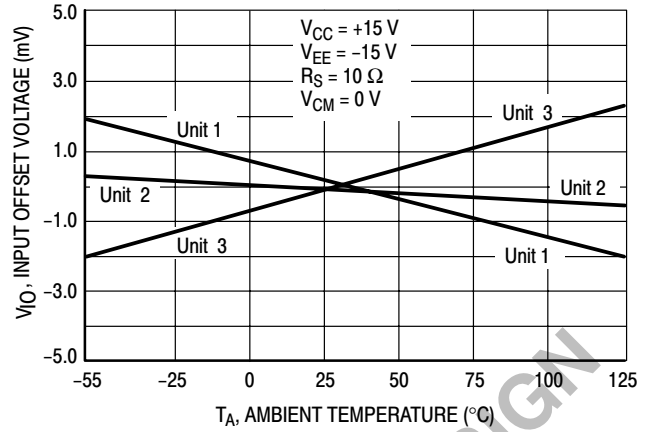


Figure 4. Input Bias Current versus Temperature

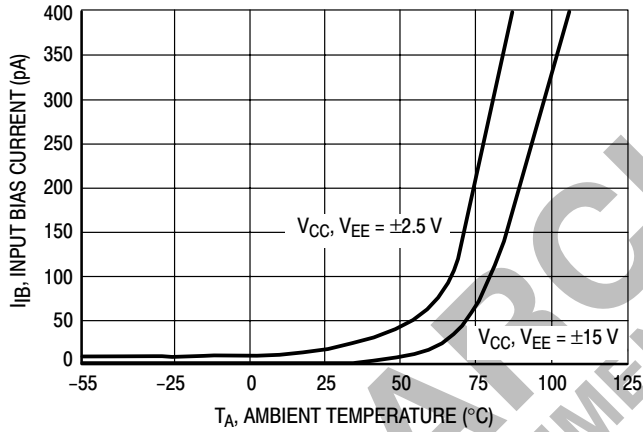


Figure 5. Input Bias Current versus Common Mode Voltage

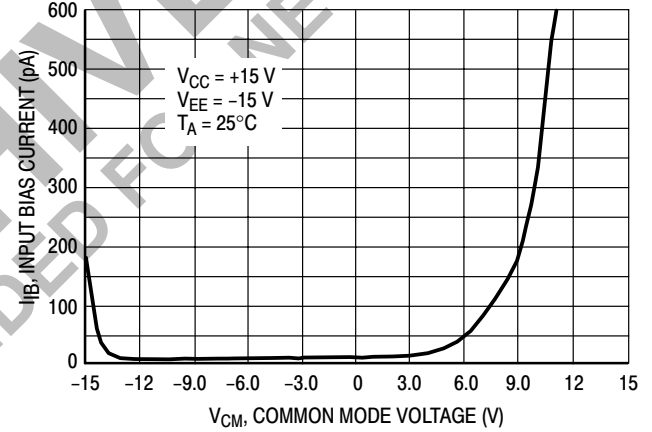


Figure 6. Input Common Mode Voltage Range versus Temperature

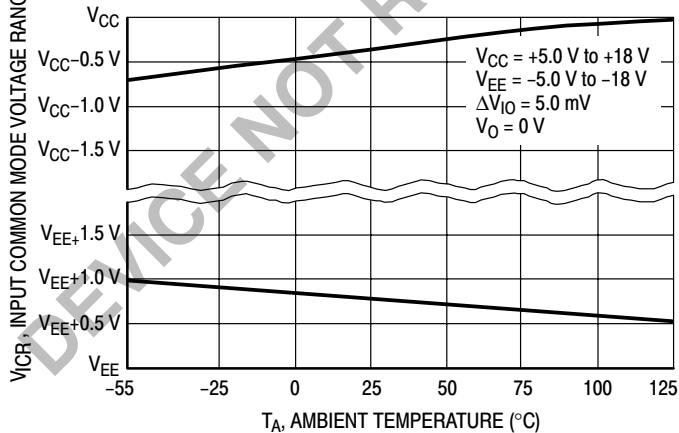


Figure 7. Open Loop Voltage Gain versus Temperature

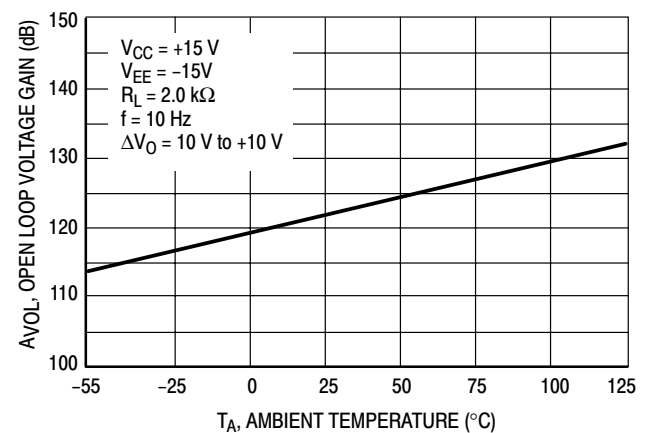


Figure 8. Output Voltage Swing versus Supply Voltage

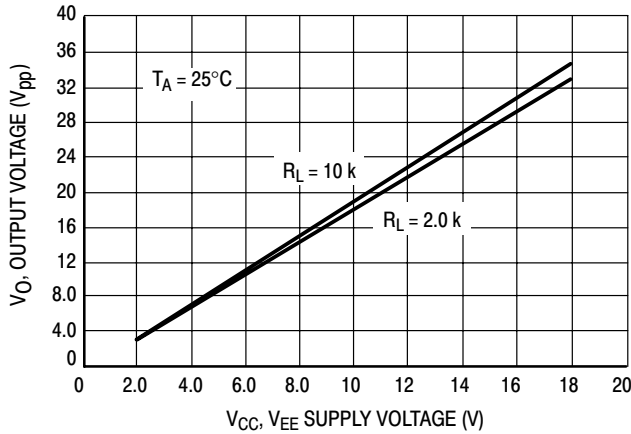


Figure 9. Output Voltage versus Frequency

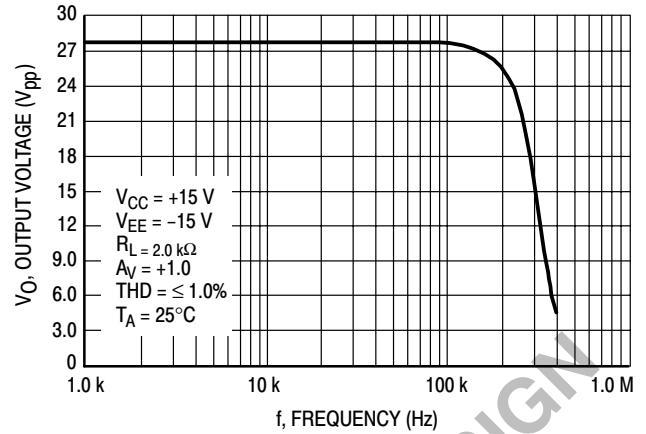


Figure 10. Output Saturation Voltage versus Load Current

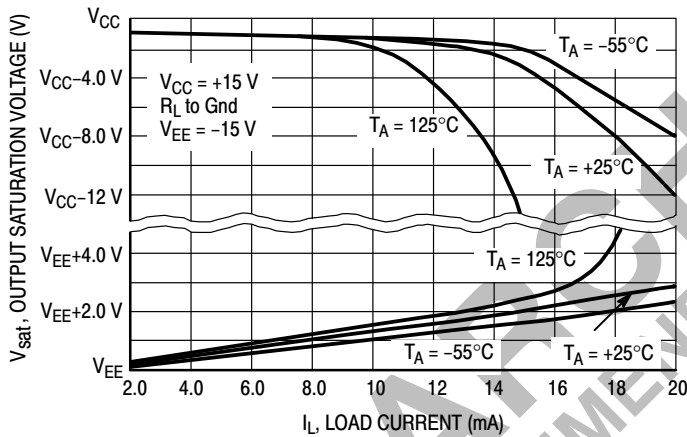


Figure 11. Common Mode Rejection versus Frequency

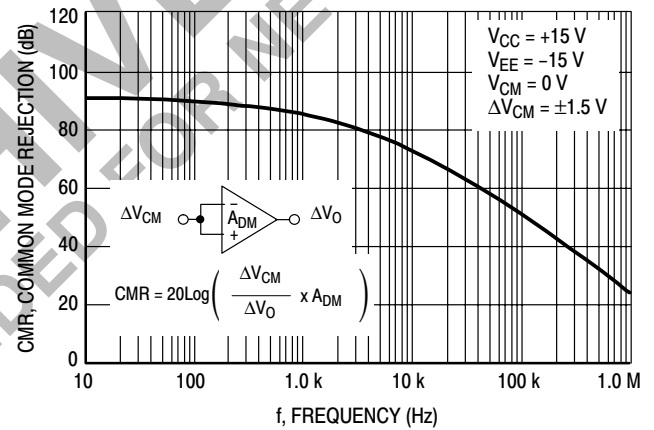


Figure 12. Positive Power Supply Rejection versus Frequency

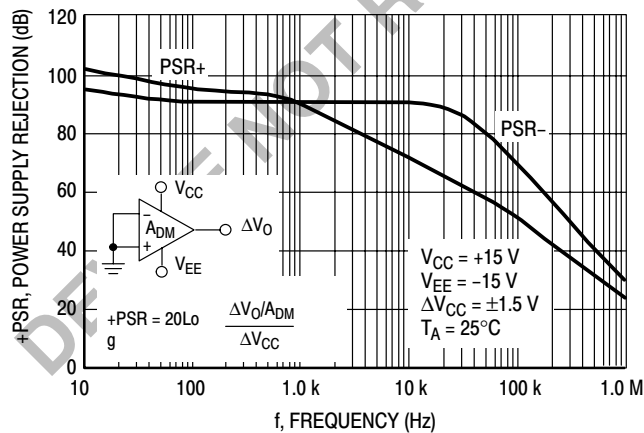


Figure 13. Output Short Circuit Source Current versus Temperature

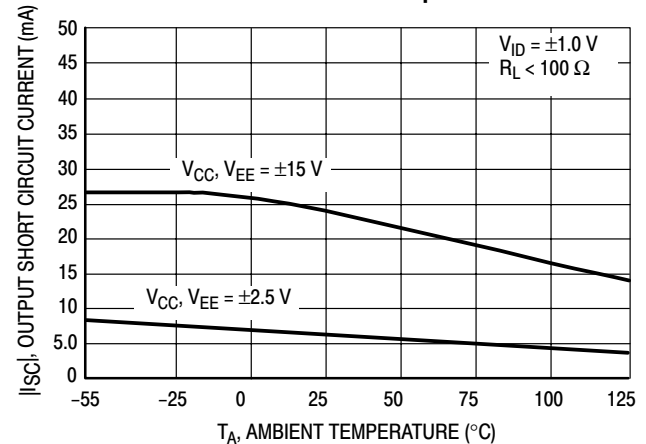


Figure 14. Output Short Circuit Sink Current versus Temperature

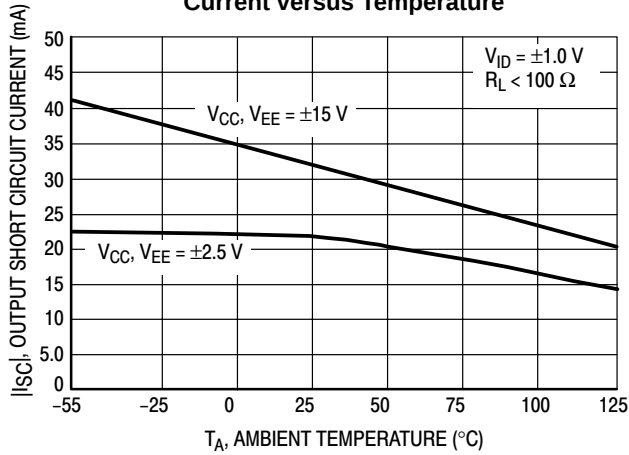


Figure 15. Power Supply Current versus Supply Voltage

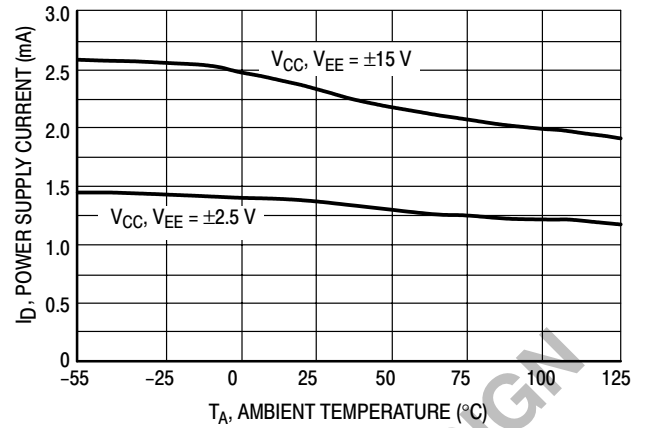


Figure 16. Slew Rate versus Temperature

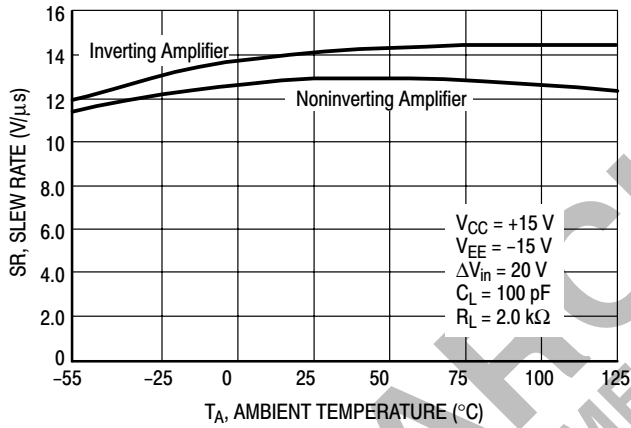


Figure 17. Gain Bandwidth Product versus Temperature

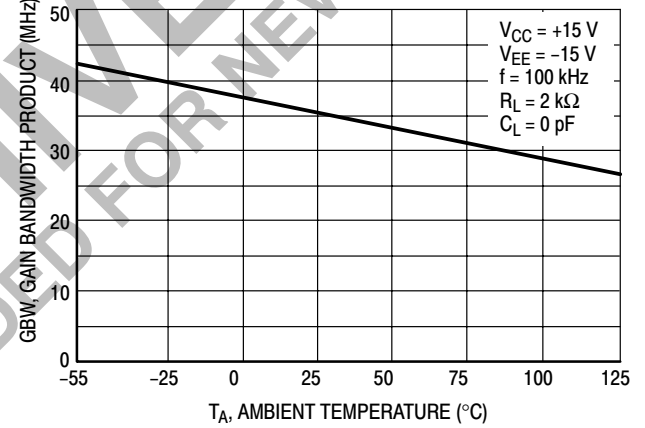


Figure 18. Gain and Phase versus Frequency

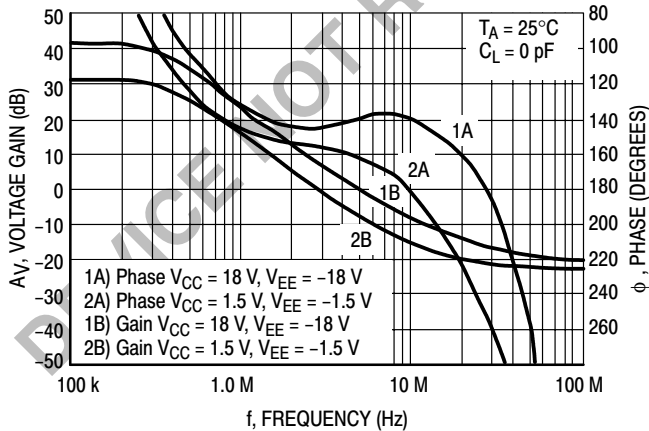


Figure 19. Phase Margin and Gain Margin versus Differential Source Resistance

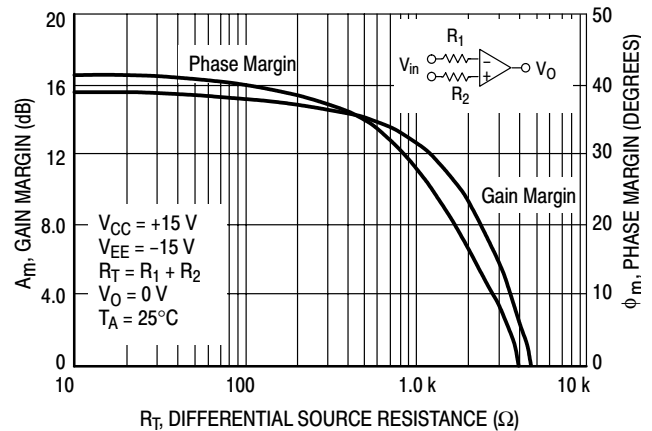


Figure 20. Open Loop Gain and Phase Margin versus Output Load Capacitance

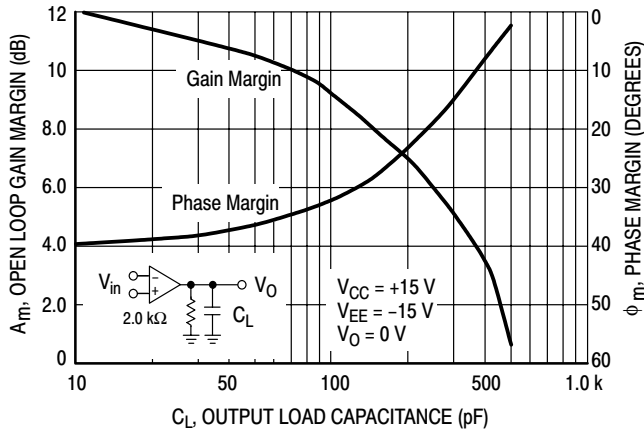


Figure 21. Gain and Phase versus Frequency

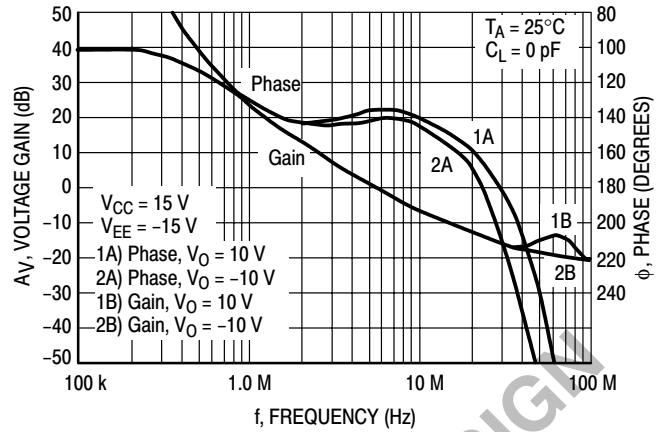


Figure 22. Channel Separation versus Frequency

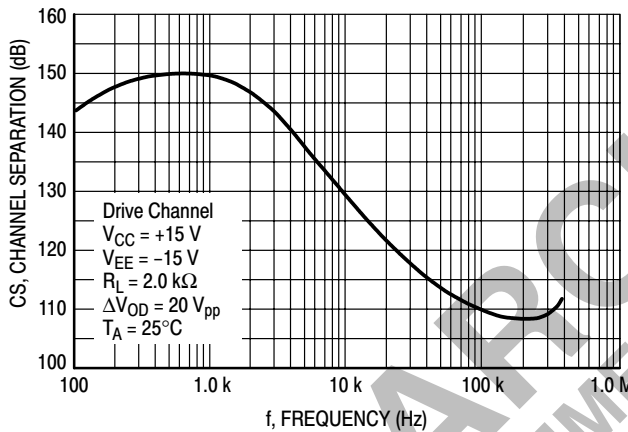


Figure 23. Total Harmonic Distortion versus Frequency

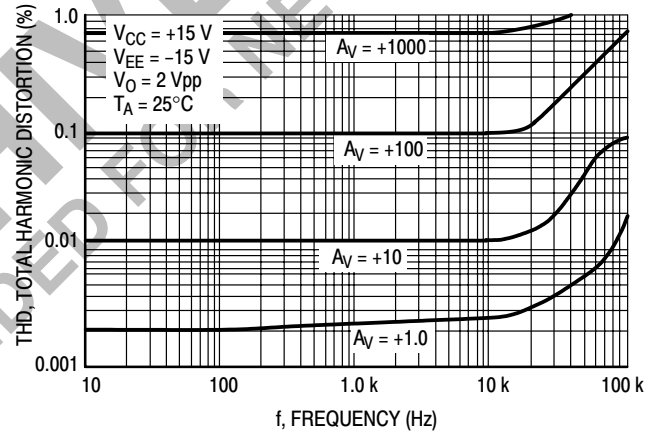


Figure 24. Output Impedance versus Frequency

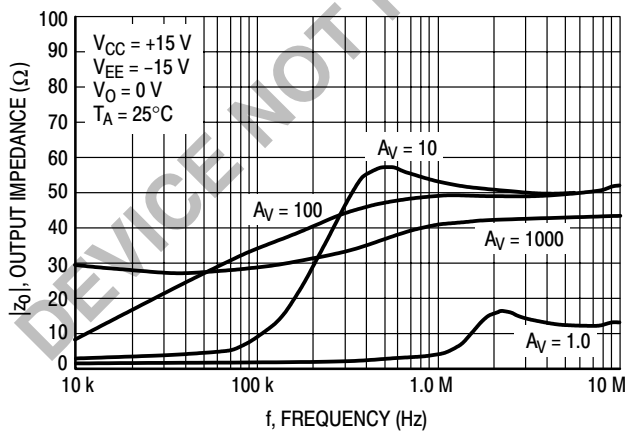


Figure 25. Input Referred Noise Voltage versus Frequency

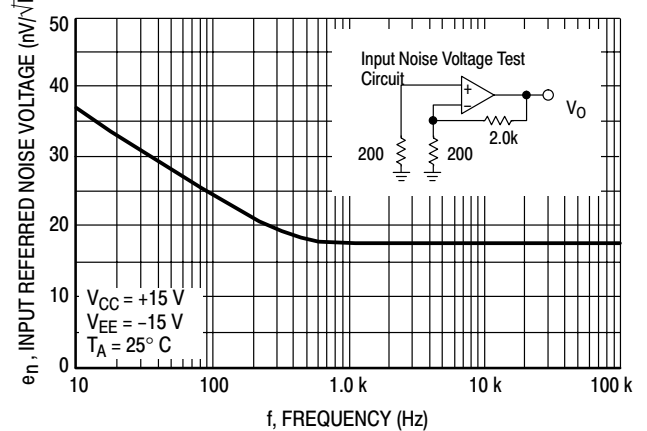


Figure 26. Percent Overshoot versus Load Capacitance

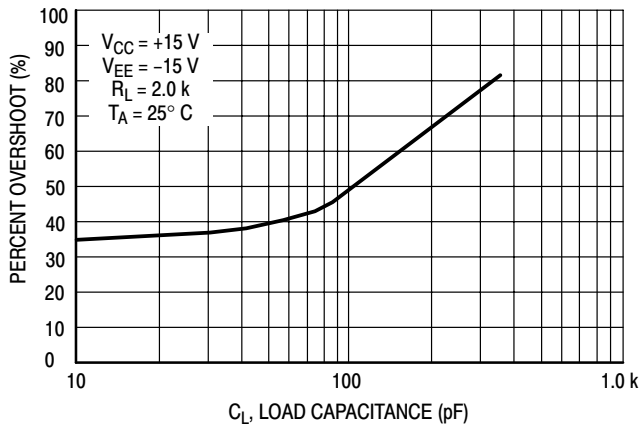


Figure 27. Noninverting Amplifier Overshoot

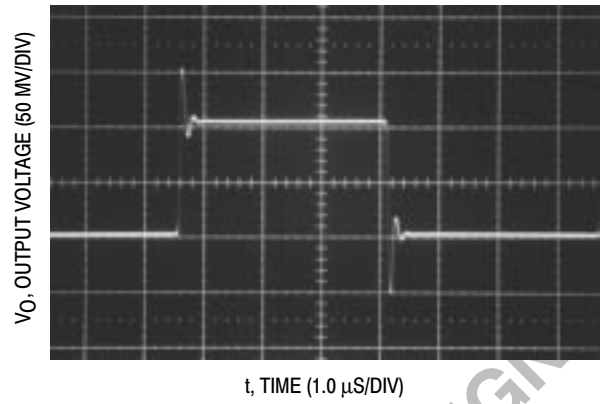


Figure 28. Noninverting Amplifier Slew Rate

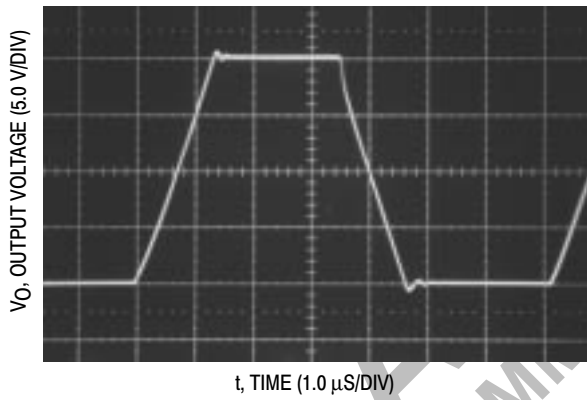
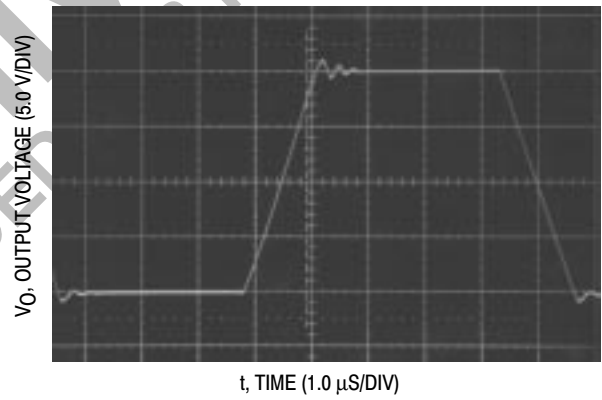
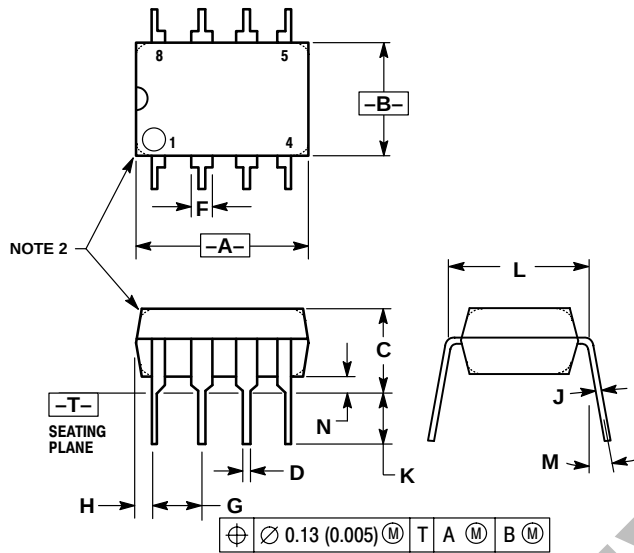


Figure 29. Inverting Amplifier Slew Rate



OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 626-05
ISSUE K

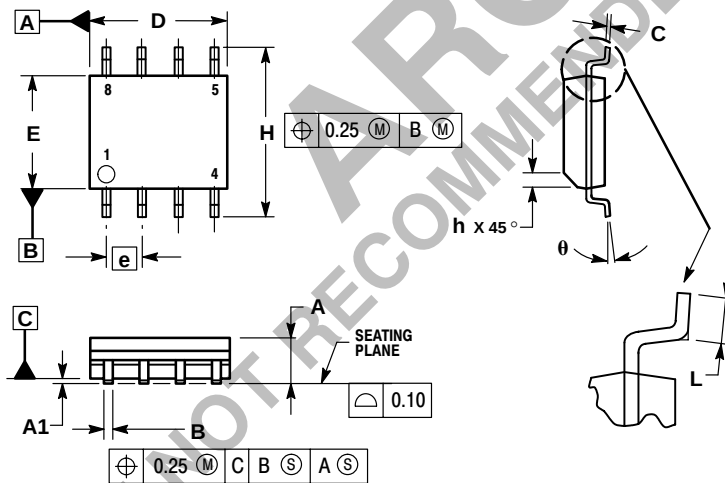


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---		10°	
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751-05
(SO-8)
ISSUE R



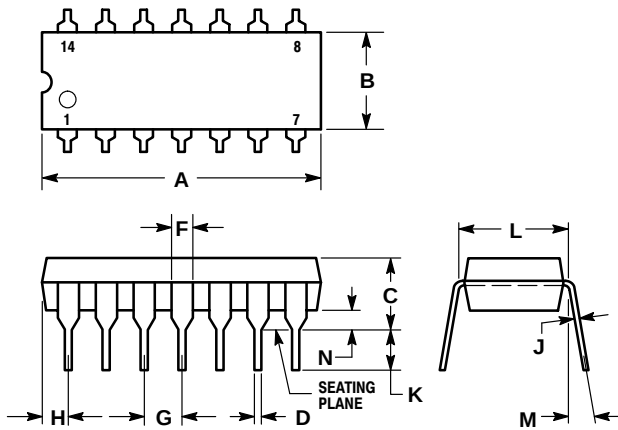
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

OUTLINE DIMENSIONS

P SUFFIX
 PLASTIC PACKAGE
 CASE 646-06
 ISSUE L

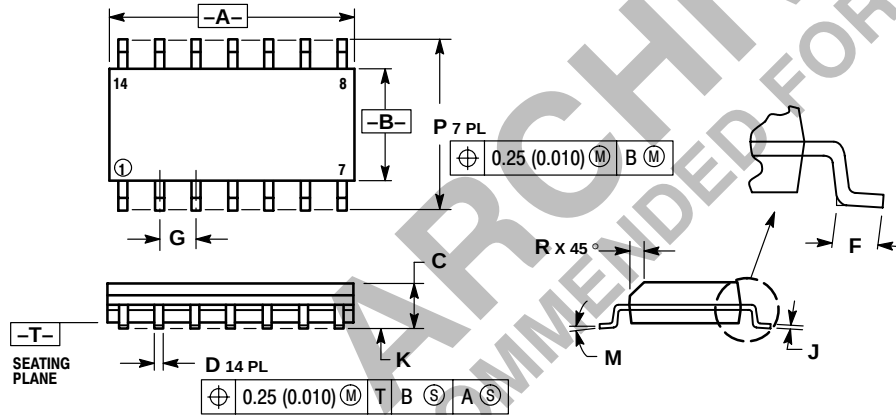


NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
 PLASTIC PACKAGE
 CASE 751A-03
 (SO-14)
 ISSUE F



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

Notes

ARCHIVE
DEVICE NOT RECOMMENDED FOR NEW DESIGN

ZIP R TRIM is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor is a trademark and  is a registered trademark of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.