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April 1st, 2010
Renesas Electronics Corporation

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

PRELIMINARY

MITSUBISHI MICROCOMPUTERS
M37733M4LXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37733M4LXXXHP is a single-chip microcomputer using the 7700 Family core. This single-chip microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the ROM, RAM, multiple-function timers, serial I/O, A-D converter, and so on.

Its strong points are the low power dissipation, the low supply voltage, and the small package.

FEATURES

- Number of basic instructions 103
- Memory size ROM 32 Kbytes
- RAM 2048 bytes
- Instruction execution time
 The fastest instruction at 12 MHz frequency 333 ns
- Single power supply 2.7–5.5 V
- Low power dissipation (At 3 V supply voltage, 12 MHz frequency)
..... 9 mW (Typ.)

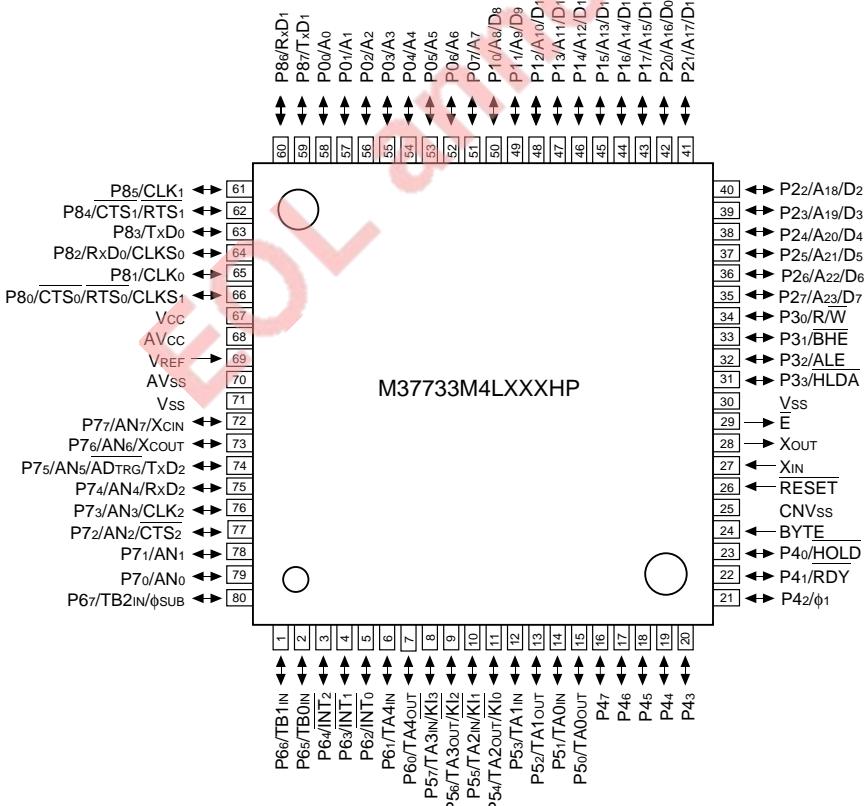
- Interrupts 19 types, 7 levels
- Multiple-function 16-bit timer 5 + 3
- Serial I/O (UART or clock synchronous) 3
- 10-bit A-D converter 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output
(ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 68
- Clock generating circuit 2 circuits built-in
- Small package 80-pin plastic molded fine-pitch QFP
(80P6D-A;0.5 mm lead pitch)

APPLICATION

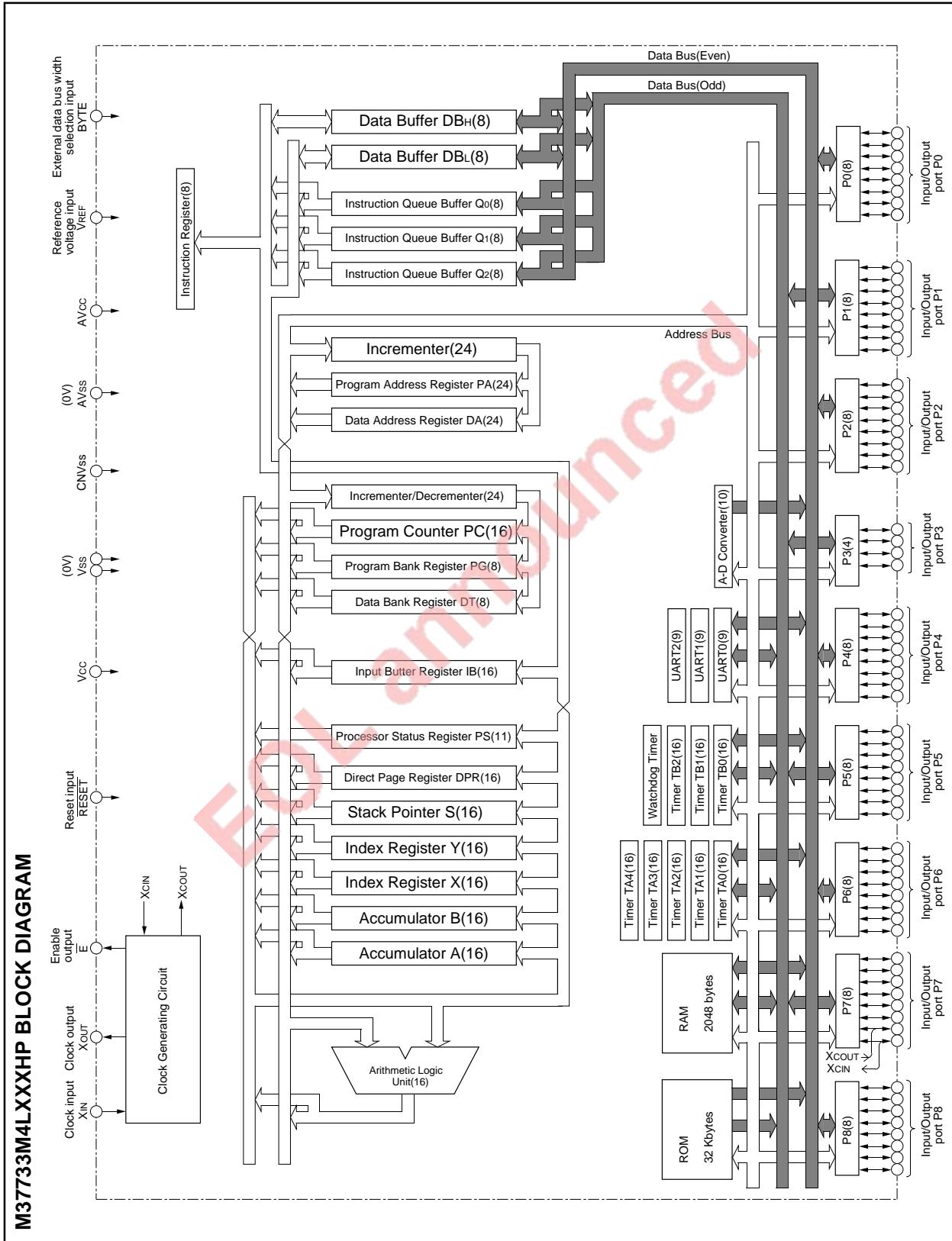
Control devices for general commercial equipment such as office automation, office equipment, personal information equipment, and so on.

Control devices for general industrial equipment such as communication equipment, and so on.

PIN CONFIGURATION (TOP VIEW)



Outline 80P6D-A



PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37733M4LXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37733M4LXXXHP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		333 ns (the fastest instruction at external clock 12 MHz frequency)
Memory size	ROM	32 Kbytes
	RAM	2048 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit X 8
	P3	4-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 3
A-D converter		10-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		2.7 – 5.5 V
Power dissipation		9 mW (at 3 V supply voltage, external clock 12 MHz frequency) 22.5 mW (at 5 V supply voltage, external clock 12 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16 Mbytes
Operating temperature range		–40 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded fine-pitch QFP (80P6D-A;0.5 mm lead pitch)

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 2.7 – 5.5 V to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
RESET	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
XIN	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
E	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. When output level of E signal is "L", data/instruction read or data write is performed.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P00 – P07	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output address (A0 – A7).
P10 – P17	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D8 – D15) is input/output or an address (A8 – A15) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A8 – A15) is output.
P20 – P27	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D0 – D7) is input/output or an address (A16 – A23) is output.
P30 – P33	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, R/W, BHE, ALE, and HLDA signals are output.
P40 – P47	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P40, P41, and P42 become HOLD and RDY input pins, and clock φ1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P42 also functions as an I/O port.
P50 – P57	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input (K10 – K13).
P60 – P67	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input (INT0 – INT2) and input pins for timers B0 to B2. P67 also functions as sub-clock φSUB output pin.
P70 – P77	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. P72 to P75 also function as I/O pins for UART2. Additionally, P76 and P77 have the function as the output pin (Xcout) and the input pin (Xcin) of the sub-clock (32 kHz) oscillation circuit, respectively. When P76 and P77 are used as the Xcout and Xcin pins, connect a resonator or an oscillator between the both.
P80 – P87	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.

BASIC FUNCTION BLOCKS

The M37733M4LXXXHP has the same functions as the M37733MHBXXXFP except for the memory allocation, the reset circuit, the ROM area modification function, and the package. Refer to the section on the M37733MHBXXXFP.

MEMORY

The memory map is shown in Figure 1. The address space has a capacity of 16 Mbytes and is allocated to addresses from 016 to FFFFFFF16. The address space is divided by 64-Kbyte unit called bank. The banks are numbered from 016 to FF16.

Built-in ROM, RAM and control registers for internal peripheral devices are assigned to bank 016.

The 32-Kbyte area from addresses 800016 to FFFF16 is the built-in ROM. Addresses FFD616 to FFFF16 are the RESET and interrupt vector addresses and contain the interrupt vectors. Refer to the section on interrupts for details.

The 2048-byte area allocated to addresses from 8016 to 87F16 is the built-in RAM. In addition to storing data, the RAM is used as stack during a subroutine call or interrupts.

Peripheral devices such as I/O ports, A-D converter, serial I/O, timer, and interrupt control registers are allocated to addresses from 016 to 7F16.

Additionally, the internal ROM area can be modified by software. Refer to the section on ROM area modification function for details.

A 256-byte direct page area can be allocated anywhere in bank 016 by using the direct page register (DPR). In the direct page addressing mode, the memory in the direct page area can be accessed with two words. Hence program steps can be reduced.

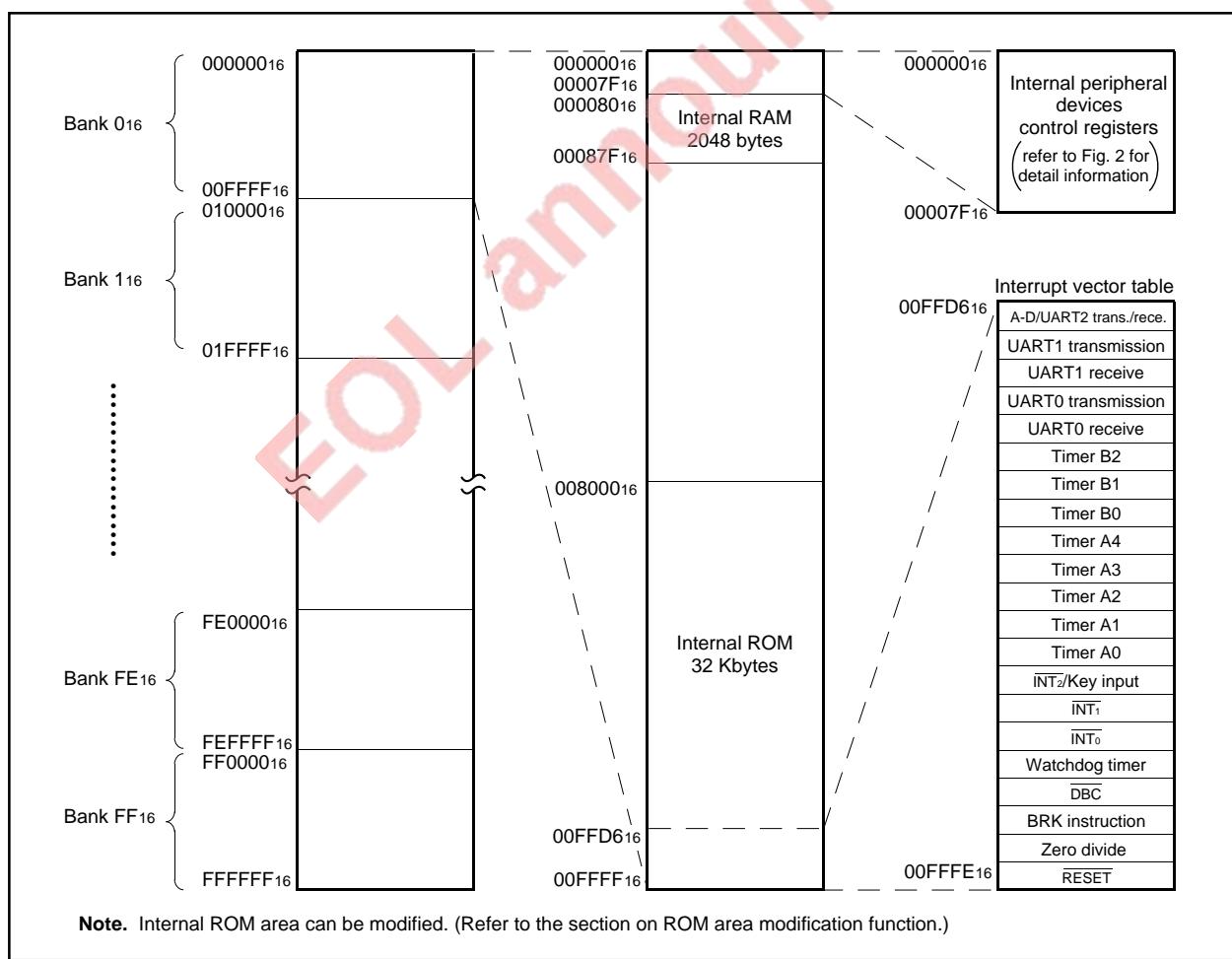


Fig. 1 Memory map

Address (Hexadecimal notation)	Address (Hexadecimal notation)
000000	
000001	
000002	Port P0 register
000003	Port P1 register
000004	Port P0 direction register
000005	Port P1 direction register
000006	Port P2 register
000007	Port P3 register
000008	Port P2 direction register
000009	Port P3 direction register
00000A	Port P4 register
00000B	Port P5 register
00000C	Port P4 direction register
00000D	Port P5 direction register
00000E	Port P6 register
00000F	Port P7 register
000010	Port P6 direction register
000011	Port P7 direction register
000012	Port P8 register
000013	
000014	Port P8 direction register
000015	
000016	
000017	
000018	
000019	
00001A	
00001B	
00001C	Reserved area (Note)
00001D	Reserved area (Note)
00001E	A-D control register 0
00001F	A-D control register 1
000020	A-D register 0
000021	
000022	A-D register 1
000023	
000024	A-D register 2
000025	
000026	A-D register 3
000027	
000028	A-D register 4
000029	
00002A	A-D register 5
00002B	
00002C	A-D register 6
00002D	
00002E	A-D register 7
00002F	
000030	UART 0 transmit/receive mode register
000031	UART 0 baud rate register
000032	UART 0 transmission buffer register
000033	
000034	UART 0 transmit/receive control register 0
000035	UART 0 transmit/receive control register 1
000036	UART 0 receive buffer register
000037	
000038	UART 1 transmit/receive mode register
000039	UART 1 baud rate register
00003A	UART 1 transmission buffer register
00003B	
00003C	UART 1 transmit/receive control register 0
00003D	UART 1 transmit/receive control register 1
00003E	UART 1 receive buffer register
00003F	
000040	Count start flag
000041	
000042	One-shot start flag
000043	
000044	Up-down flag
000045	
000046	Timer A0 register
000047	
000048	Timer A1 register
000049	
00004A	Timer A2 register
00004B	
00004C	Timer A3 register
00004D	
00004E	Timer A4 register
00004F	
000050	Timer B0 register
000051	
000052	Timer B1 register
000053	
000054	Timer B2 register
000055	
000056	Timer A0 mode register
000057	Timer A1 mode register
000058	Timer A2 mode register
000059	Timer A3 mode register
00005A	Timer A4 mode register
00005B	Timer B0 mode register
00005C	Timer B1 mode register
00005D	Timer B2 mode register
00005E	Processor mode register 0
00005F	Processor mode register 1
000060	Watchdog timer register
000061	Watchdog timer frequency selection flag
000062	Reserved area (Note)
000063	Memory allocation control register
000064	UART 2 transmit/receive mode register
000065	UART 2 baud rate register
000066	
000067	UART 2 transmission buffer register
000068	UART 2 transmit/receive control register 0
000069	UART 2 transmit/receive control register 1
00006A	UART 2 receive buffer register
00006B	
00006C	Oscillation circuit control register 0
00006D	Port function control register
00006E	Serial transmit control register
00006F	Oscillation circuit control register 1
000070	A-D/UART 2 trans./rece. interrupt control register
000071	UART 0 transmission interrupt control register
000072	UART 0 receive interrupt control register
000073	UART 1 transmission interrupt control register
000074	UART 1 receive interrupt control register
000075	Timer A0 interrupt control register
000076	Timer A1 interrupt control register
000077	Timer A2 interrupt control register
000078	Timer A3 interrupt control register
000079	Timer A4 interrupt control register
00007A	Timer B0 interrupt control register
00007B	Timer B1 interrupt control register
00007C	Timer B2 interrupt control register
00007D	INT ₀ interrupt control register
00007E	INT ₁ interrupt control register
00007F	INT ₂ /Key input interrupt control register

Note. Do not write to this address.

Fig. 2 Location of internal peripheral devices and interrupt control registers

PRELIMINARY

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MITSUBISHI MICROCOMPUTERS

M37733M4LXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

RESET CIRCUIT

The microcomputer is released from the reset state when the RESET pin is returned to "H" level after holding it at "L" level with the power source voltage at 2.7 – 5.5 V. Program execution starts at the address formed by setting address A₂₃ – A₁₆ to 00₁₆, A₁₅ – A₈ to the contents of address FFFF₁₆, and A₇ – A₀ to the contents of address FFFE₁₆. Figure 3 shows an example of a reset circuit. When the stabilized clock is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.55 V or less when the power source voltage reaches 2.7 V. When a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from "L" to "H" after the main-clock oscillation is fully stabilized.

The status of the internal registers during reset is the same as the M37733MHBXXXFP's.

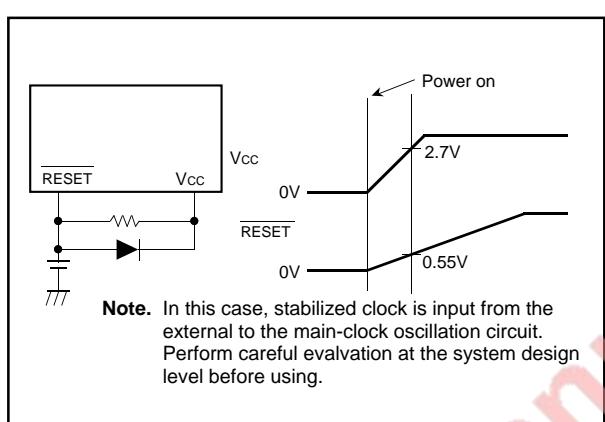


Fig. 3 Example of a reset circuit

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MITSUBISHI MICROCOMPUTERS

M37733M4LXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

ROM AREA MODIFICATION FUNCTION

The internal ROM size and its address area of the M37733M4LXXXHP can be modified by the memory allocation control register's bit 0 shown in Figure 4.

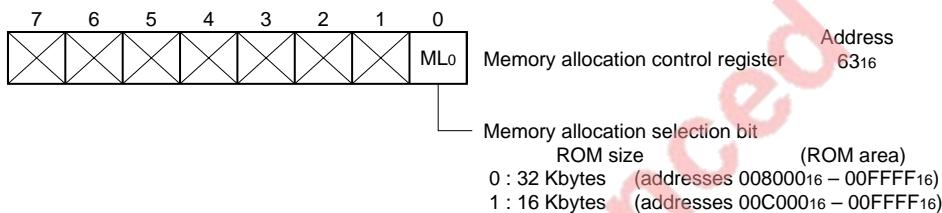
Figure 6 shows the memory allocation in which the internal ROM size and its address area are modified.

Make sure to write data in the memory allocation control register as the flow shown in Figure 5.

This ROM area modification function is valid in memory expansion mode and single-chip mode.

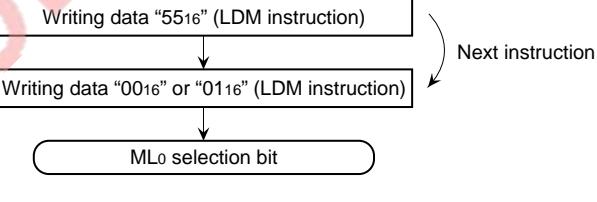
When ordering a mask ROM, Mitsubishi Electric corp. produces the mask ROM using the data within 32 Kbytes (addresses 008000₁₆ – 00FFFF₁₆). It is regardless of the selected ROM size (refer to MASK ROM ORDER CONFIRMATION FORM.) Therefore, program "FF₁₆" to the addresses out of the selected ROM area in the EPROM which you tender when ordering a mask ROM.

Address 00FFFF₁₆ of this microcomputer corresponds to the lowest address of the EPROM which you tender.



Note. Write to the memory allocation control register as the flow shown in Figure 5.

Fig. 4 Bit configuration of memory allocation control register



- How to write in memory allocation control register

Fig. 5 How to write in memory allocation control register

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MITSUBISHI MICROCOMPUTERS

M37733M4LXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

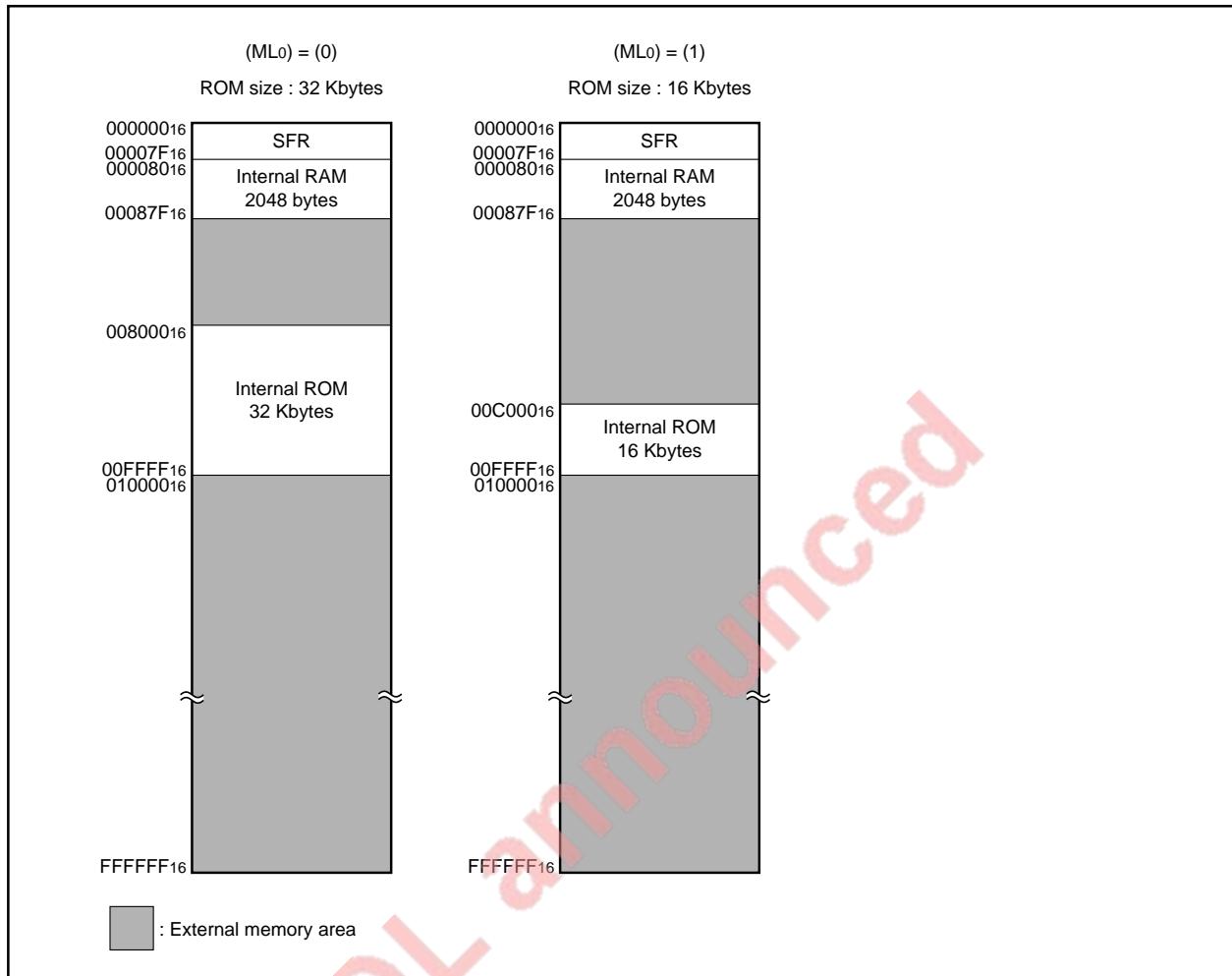


Fig. 6 Memory allocation (modification of internal ROM area by memory allocation selection bit)

ADDRESSING MODES

The M37733M4LXXXHP has 28 powerful addressing modes. Refer to the SINGLE-CHIP 16-BIT MICROCOMPUTERS DATA BOOK for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37733M4LXXXHP has 103 machine instructions. Refer to the SINGLE-CHIP 16-BIT MICROCOMPUTERS DATA BOOK for details.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M37733M4LXXXHP mask ROM order confirmation form
- (2) 80P6D mark specification form
- (3) ROM data (EPROM 3 sets)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Power source voltage		−0.3 to +7	V
A _{Vcc}	Analog power source voltage		−0.3 to +7	V
V _i	Input voltage RESET, CNV _{ss} , BYTE		−0.3 to +12	V
V _i	Input voltage P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₇ , P ₅₀ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇ , V _{REF} , X _{IN}		−0.3 to V _{cc} + 0.3	V
V _o	Output voltage P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₇ , P ₅₀ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇ , X _{OUT} , \bar{E}		−0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	T _a = 25 °C	200	mW
T _{opr}	Operating temperature		−40 to +85	°C
T _{stg}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (V_{cc} = 2.7 – 5.5 V, T_a = −40 to +85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{cc}	Power source voltage f(X _{IN}) : Operating	2.7		5.5	V
	f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz	2.7		5.5	
A _{Vcc}	Analog power source voltage		V _{cc}		V
V _{ss}	Power source voltage		0		V
A _{Vss}	Analog power source voltage		0		V
V _{iH}	High-level input voltage P ₀₀ – P ₀₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₇ , P ₅₀ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇ , X _{IN} , RESET, CNV _{ss} , BYTE, X _{CIN} (Note 3)	0.8 V _{cc}		V _{cc}	V
V _{iH}	High-level input voltage P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ (in single-chip mode)	0.8 V _{cc}		V _{cc}	V
V _{iH}	High-level input voltage P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ (in memory expansion mode and microprocessor mode)	0.5 V _{cc}		V _{cc}	V
V _{iL}	Low-level input voltage P ₀₀ – P ₀₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₇ , P ₅₀ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇ , X _{IN} , RESET, CNV _{ss} , BYTE, X _{CIN} (Note 3)	0		0.2V _{cc}	V
V _{iL}	Low-level input voltage P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ (in single-chip mode)	0		0.2V _{cc}	V
V _{iL}	Low-level input voltage P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ (in memory expansion mode and microprocessor mode)	0		0.16V _{cc}	V
I _{OH(peak)}	High-level peak output current P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₇ , P ₅₀ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇			−10	mA
I _{OH(avg)}	High-level average output current P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₇ , P ₅₀ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇			−5	mA
I _{OL(peak)}	Low-level peak output current P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₃ , P ₅₄ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇			10	mA
I _{OL(peak)}	Low-level peak output current P ₄₄ – P ₄₇ , P ₅₀ – P ₅₃			16	mA
I _{OL(avg)}	Low-level average output current P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₃ , P ₅₄ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇			5	mA
I _{OL(avg)}	Low-level average output current P ₄₄ – P ₄₇ , P ₅₀ – P ₅₃			12	mA
f(X _{IN})	Main-clock oscillation frequency (Note 4)			12	MHz
f(X _{CIN})	Sub-clock oscillation frequency		32.768	50	kHz

Notes 1. Average output current is the average value of a 100 ms interval.

2. The sum of I_{OL(peak)} for ports P₀, P₁, P₂, P₃, and P₈ must be 80 mA or less,
the sum of I_{OH(peak)} for ports P₀, P₁, P₂, P₃, and P₈ must be 80 mA or less,
the sum of I_{OL(peak)} for ports P₄, P₅, P₆, and P₇ must be 100 mA or less, and
the sum of I_{OH(peak)} for ports P₄, P₅, P₆, and P₇ must be 80 mA or less.
3. Limits V_{iH} and V_{iL} for X_{CIN} are applied when the sub clock external input selection bit = "1".
4. The maximum value of f(X_{IN}) = 6 MHz when the main clock division selection bit = "1".

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, V_{SS} = 0 V, T_A = -40 to +85 °C, f(XIN) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V _{OH}	High-level output voltage P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₃ , P ₄₀ – P ₄₇ , P ₅₀ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇	V _{CC} = 5 V, I _{OH} = -10 mA	3			V	
		V _{CC} = 3 V, I _{OH} = -1 mA	2.5				
V _{OH}	High-level output voltage P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₃	V _{CC} = 5 V, I _{OH} = -400 μA	4.7			V	
V _{OH}	High-level output voltage P ₃₀ – P ₃₂	V _{CC} = 5 V, I _{OH} = -10 mA	3.1			V	
		V _{CC} = 5 V, I _{OH} = -400 μA	4.8				
		V _{CC} = 3 V, I _{OH} = -1 mA	2.6				
		V _{CC} = 5 V, I _{OH} = -10 mA	3.4				
V _{OL}	Low-level output voltage P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₃ , P ₄₀ – P ₄₃ , P ₅₄ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇	V _{CC} = 5 V, I _{OL} = 10 mA			2	V	
		V _{CC} = 3 V, I _{OL} = 1 mA			0.5		
		V _{CC} = 5 V, I _{OL} = 16 mA			1.8		
V _{OL}	Low-level output voltage P ₄₄ – P ₄₇ , P ₅₀ – P ₅₃	V _{CC} = 3 V, I _{OL} = 10 mA			1.5	V	
		V _{CC} = 5 V, I _{OL} = 2 mA			0.45		
V _{OL}	Low-level output voltage P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₃	V _{CC} = 5 V, I _{OL} = 10 mA			1.9	V	
		V _{CC} = 5 V, I _{OL} = 2 mA			0.43		
		V _{CC} = 3 V, I _{OL} = 1 mA			0.4		
V _{OL}	Low-level output voltage P ₃₀ – P ₃₂	V _{CC} = 5 V, I _{OL} = 10 mA			1.6	V	
		V _{CC} = 5 V, I _{OL} = 2 mA			0.4		
		V _{CC} = 3 V, I _{OL} = 1 mA			0.4		
V _{T+} – V _{T-}	Hysteresis HOLD, RDY, TA0IN – TA4IN, TB0IN – TB2IN, INT ₀ – INT ₂ , AD _{TRG} , CTS ₀ , CTS ₁ , CTS ₂ , CLK ₀ , CLK ₁ , CLK ₂ , K ₁₀ – K ₁₃	V _{CC} = 5 V	0.4		1	V	
		V _{CC} = 3 V	0.1		0.7		
		V _{CC} = 5 V	0.2		0.5		
V _{T+} – V _{T-}	Hysteresis RESET	V _{CC} = 3 V	0.1		0.4	V	
		V _{CC} = 5 V	0.06		0.26		
V _{T+} – V _{T-}	Hysteresis XIN	V _{CC} = 5 V	0.1		0.4	V	
		V _{CC} = 3 V	0.06		0.26		
V _{T+} – V _{T-}	Hysteresis XCIN (When external clock is input)	V _{CC} = 5 V	0.1		0.4	V	
		V _{CC} = 3 V	0.06		0.26		
I _{IH}	High-level input current P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₇ , P ₅₀ – P ₅₇ , P ₆₀ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇ , XIN, RESET, CNVss, BYTE	V _{CC} = 5 V, V _I = 5 V			5	μA	
		V _{CC} = 3 V, V _I = 3 V			4		
I _{IL}	Low-level input current P ₀₀ – P ₀₇ , P ₁₀ – P ₁₇ , P ₂₀ – P ₂₇ , P ₃₀ – P ₃₃ , P ₄₀ – P ₄₇ , P ₅₀ – P ₅₃ , P ₆₀ , P ₆₁ , P ₆₅ – P ₆₇ , P ₇₀ – P ₇₇ , P ₈₀ – P ₈₇ , XIN, RESET, CNVss, BYTE	V _{CC} = 5 V, V _I = 0 V			-5	μA	
		V _{CC} = 3 V, V _I = 0 V			-4		
I _{IL}	Low-level input current P ₅₄ – P ₅₇ , P ₆₂ – P ₆₄	V _I = 0 V, without a pull-up transistor	V _{CC} = 5 V		-5	μA	
		V _{CC} = 3 V			-4		
		V _I = 0 V, with a pull-up transistor	V _{CC} = 5 V	-0.25	-0.5	-1.0	mA
		V _{CC} = 3 V	-0.08	-0.18	-0.35		
V _{RAM}	RAM hold voltage	When clock is stopped.	2			V	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5$ V, $V_{SS} = 0$ V, $T_a = -40$ to $+85$ °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
I _{CC}	Power source current	When single-chip mode, output pins are open, and other pins are V_{SS} .	V _{CC} = 5 V, $f(X_{IN}) = 12$ MHz (square waveform), $(f(f_2) = 6$ MHz), $f(X_{CIN}) = 32.768$ kHz, in operating (Note 1)		4.5	9	mA
			V _{CC} = 3 V, $f(X_{IN}) = 12$ MHz (square waveform), $(f(f_2) = 6$ MHz), $f(X_{CIN}) = 32.768$ kHz, in operating (Note 1)		3	6	mA
			V _{CC} = 3 V, $f(X_{IN}) = 12$ MHz (square waveform), $(f(f_2) = 0.75$ MHz), $f(X_{CIN})$: Stopped, in operating		0.4	0.8	mA
			V _{CC} = 3 V, $f(X_{IN}) = 12$ MHz (square waveform), $f(X_{CIN}) = 32.768$ kHz, when a WIT instruction is executed (Note 2)		6	12	μA
			V _{CC} = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN}) = 32.768$ kHz, in operating (Note 3)		30	60	μA
			V _{CC} = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN}) = 32.768$ kHz, when a WIT instruction is executed (Note 4)		3	6	μA
			T _a = 25 °C, when clock is stopped			1	μA
			T _a = 85 °C, when clock is stopped			20	μA

Notes

1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
4. This applies when the X_{OUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1".

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5$ V, $V_{SS} = AV_{SS} = 0$ V, $T_a = -40$ to $+85$ °C, $f(X_{IN}) = 12$ MHz, unless otherwise noted (Note))

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V _{REF} = V _{CC}			10	Bits
—	Absolute accuracy	V _{REF} = V _{CC}			± 3	LSB
R _{LADDER}	Ladder resistance	V _{REF} = V _{CC}	10		25	kΩ
t _{CONV}	Conversion time		19.6			μs
V _{REF}	Reference voltage		2.7		V _{CC}	V
V _{IA}	Analog input voltage		0		V _{REF}	V

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 6$ MHz.

TIMING REQUIREMENTS ($V_{CC} = 2.7 - 5.5$ V, $V_{SS} = 0$ V, $T_a = -40$ to $+85$ °C, $f(XIN) = 12$ MHz, unless otherwise noted (Note 1))

Notes 1. This applies when the main clock division selection bit = "0" and $f(f_2) = 6$ MHz.

2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 1)	83		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 2)	33		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 2)	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Notes 1. When the main clock division selection bit = "1", the minimum value of $t_c = 166$ ns.

2. When the main clock division selection bit = "1", values of $t_{w(H)} / t_c$ and $t_{w(L)} / t_c$ must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P0D-E)}$	Port P0 input setup time	200		ns
$t_{su(P1D-E)}$	Port P1 input setup time	200		ns
$t_{su(P2D-E)}$	Port P2 input setup time	200		ns
$t_{su(P3D-E)}$	Port P3 input setup time	200		ns
$t_{su(P4D-E)}$	Port P4 input setup time	200		ns
$t_{su(P5D-E)}$	Port P5 input setup time	200		ns
$t_{su(P6D-E)}$	Port P6 input setup time	200		ns
$t_{su(P7D-E)}$	Port P7 input setup time	200		ns
$t_{su(P8D-E)}$	Port P8 input setup time	200		ns
$t_{h(E-P0D)}$	Port P0 input hold time	0		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		ns
$t_{h(E-P3D)}$	Port P3 input hold time	0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(D-E)}$	Data input setup time	80		ns
$t_{su(RDY-φ1)}$	RDY input setup time	80		ns
$t_{su(HOLD-φ1)}$	HOLD input setup time	80		ns
$t_{h(E-D)}$	Data input hold time	0		ns
$t_{h(φ1-RDY)}$	RDY input hold time	0		ns
$t_{h(φ1-HOLD)}$	HOLD input hold time	0		ns

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

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Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	250		ns
tw(TAH)	TAiIN input high-level pulse width	125		ns
tw(TAL)	TAiIN input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time (Note)	666		ns
tw(TAH)	TAiIN input high-level pulse width (Note)	333		ns
tw(TAL)	TAiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on f(XIN). Refer to "DATA FORMULAS".

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time (Note)	666		ns
tw(TAH)	TAiIN input high-level pulse width	166		ns
tw(TAL)	TAiIN input low-level pulse width	166		ns

Note. Limits change depending on f(XIN). Refer to "DATA FORMULAS".

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high-level pulse width	166		ns
tw(TAL)	TAiIN input low-level pulse width	166		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	3333		ns
tw(UPH)	TAiOUT input high-level pulse width	1666		ns
tw(UPL)	TAiOUT input low-level pulse width	1666		ns
tsu(UP-TIN)	TAiOUT input setup time	666		ns
th(TIN-UP)	TAiOUT input hold time	666		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAjIN input cycle time	2000		ns
tsu(TAjIN-TAjout)	TAjIN input setup time	500		ns
tsu(TAjout-TAjIN)	TAjOUT input setup time	500		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TB)	TBiN input cycle time (one edge count)	250		ns
tw(TBH)	TBiN input high-level pulse width (one edge count)	125		ns
tw(TBL)	TBiN input low-level pulse width (one edge count)	125		ns
tc(TB)	TBiN input cycle time (both edges count)	500		ns
tw(TBH)	TBiN input high-level pulse width (both edges count)	250		ns
tw(TBL)	TBiN input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TB)	TBiN input cycle time (Note)	666		ns
tw(TBH)	TBiN input high-level pulse width (Note)	333		ns
tw(TBL)	TBiN input low-level pulse width (Note)	333		ns

Note. Limits change depending on f(Xin). Refer to "DATA FORMULAS".

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TB)	TBiN input cycle time (Note)	666		ns
tw(TBH)	TBiN input high-level pulse width (Note)	333		ns
tw(TBL)	TBiN input low-level pulse width (Note)	333		ns

Note. Limits change depending on f(Xin). Refer to "DATA FORMULAS".

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(AD)	ADTRG input cycle time (minimum allowable trigger)	1333		ns
tw(ADL)	ADTRG input low-level pulse width	166		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	333		ns
tw(CKH)	CLKi input high-level pulse width	166		ns
tw(CKL)	CLKi input low-level pulse width	166		ns
td(C-Q)	TxDi output delay time		100	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	65		ns
th(C-D)	RxDi input hold time	75		ns

External interrupt INTi input, key input interrupt Kli input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tw(INH)	INTi input high-level pulse width	250		ns
tw(INL)	INTi input low-level pulse width	250		ns
tw(KIL)	Kli input low-level pulse width	250		ns

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Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
tw(TAH)	TAiIN input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
tw(TAL)	TAiIN input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
tw(TBH)	TBiIN input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
tw(TBL)	TBiIN input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXFP".

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

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SWITCHING CHARACTERISTICS

($V_{CC} = 2.7 - 5.5$ V, $V_{SS} = 0$ V, $T_a = -40$ to $+85^\circ\text{C}$, $f(X_{IN}) = 12$ MHz, unless otherwise noted (Note))

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$td(E-P0Q)$	Port P0 data output delay time	Fig. 7		300	ns
$td(E-P1Q)$	Port P1 data output delay time			300	ns
$td(E-P2Q)$	Port P2 data output delay time			300	ns
$td(E-P3Q)$	Port P3 data output delay time			300	ns
$td(E-P4Q)$	Port P4 data output delay time			300	ns
$td(E-P5Q)$	Port P5 data output delay time			300	ns
$td(E-P6Q)$	Port P6 data output delay time			300	ns
$td(E-P7Q)$	Port P7 data output delay time			300	ns
$td(E-P8Q)$	Port P8 data output delay time			300	ns

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 6$ MHz.

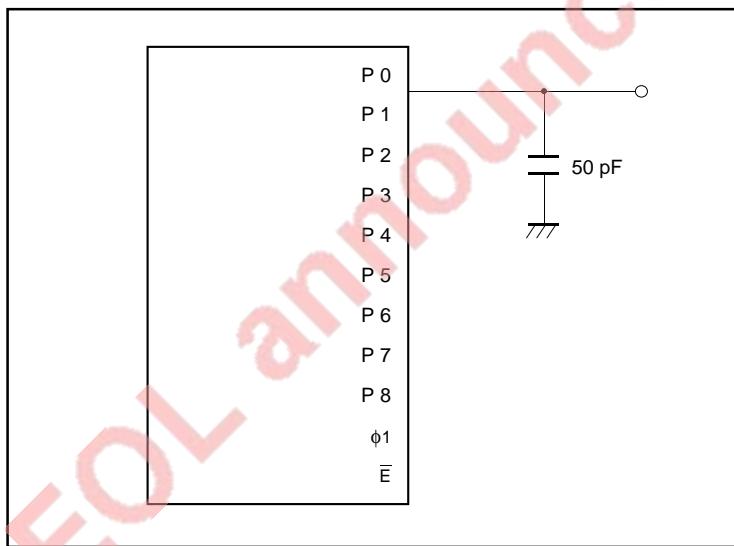


Fig. 7 Measuring circuit for ports P0 – P8 and ϕ_1

Memory expansion mode and microprocessor mode

($V_{CC} = 2.7 - 5.5$ V, $V_{SS} = 0$ V, $T_a = -40$ to $+85^\circ$ C, $f(X_{IN}) = 12$ MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit
				Min.	Max.	
td(An-E)	Address output delay time	No wait Wait 1 Wait 0	Wait mode	20		ns
td(A-E)	Address output delay time	No wait Wait 1 Wait 0		182		ns
th(E-An)	Address hold time			20		ns
tw(ALE)	ALE pulse width	No wait Wait 1 Wait 0	Wait mode	162		ns
tsu(A-ALE)	Address output set up time	No wait Wait 1 Wait 0		40		ns
th(ALE-A)	Address hold time	No wait Wait 1 Wait 0		123		ns
td(ALE-E)	ALE output delay time	No wait Wait 1 Wait 0	Wait mode	10		ns
td(E-DQ)	Data output delay time			93		ns
th(E-DQ)	Data hold time			9		ns
tw(EL)	\bar{E} pulse width	No wait Wait 1 Wait 0	Wait mode	40		ns
tpxz(E-DZ)	Floating start delay time			4		ns
tpzx(E-DZ)	Floating release delay time			40		ns
td(BHE-E)	\bar{BHE} output delay time	No wait Wait 1 Wait 0	Wait mode	90		ns
td(R/W-E)	R/\bar{W} output delay time	No wait Wait 1 Wait 0		40		ns
th(E-BHE)	\bar{BHE} hold time			131		ns
th(E-R/W)	R/W hold time		Wait mode	298		ns
td(E- ϕ 1)	ϕ 1 output delay time			10		ns
td(ϕ 1-HLDA)	HLDA output delay time			53		ns
			Wait mode	20		ns
				182		ns
				20		ns
			Wait mode	182		ns
				33		ns
				33		ns
			Wait mode	0	30	ns
					120	ns

Fig. 7

Notes 1. This applies when the main clock division selection bit = "0" and $f(f_2) = 6$ MHz.

2. No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

Bus timing data formulas (V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, T_A = –40 to +85 °C, f(X_{IN}) = 12 MHz (Max., Note 1), unless otherwise noted)

Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
td(An-E)	Address output delay time	No wait	1×10^9	– 63	ns
		Wait 1	$2 \cdot f(f_2)$		
		Wait 0	3×10^9 $2 \cdot f(f_2)$	– 68	
td(A-E)	Address output delay time	No wait	1×10^9 $2 \cdot f(f_2)$	– 63	ns
		Wait 1	3×10^9 $2 \cdot f(f_2)$	– 88	
		Wait 0	2×10^9 $2 \cdot f(f_2)$	– 88	
th(E-An)	Address hold time		1×10^9 $2 \cdot f(f_2)$	– 43	ns
tw(ALE)	ALE pulse width	No wait	1×10^9	– 43	ns
		Wait 1	$2 \cdot f(f_2)$		
		Wait 0	2×10^9 $2 \cdot f(f_2)$	– 43	
tsu(A-ALE)	Address output set up time	No wait	1×10^9	– 73	ns
		Wait 1	$2 \cdot f(f_2)$		
		Wait 0	2×10^9 $2 \cdot f(f_2)$	– 73	
th(ALE-A)	Address hold time	No wait	9		ns
		Wait 1			
		Wait 0	1×10^9 $2 \cdot f(f_2)$	– 43	
td(ALE-E)	ALE output delay time	No wait	4		ns
		Wait 1			
		Wait 0	1×10^9 $2 \cdot f(f_2)$	– 43	
td(E-DQ)	Data output delay time			90	ns
th(E-DQ)	Data hold time		1×10^9 $2 \cdot f(f_2)$	– 43	ns
tw(EL)	E pulse width	No wait	2×10^9 $2 \cdot f(f_2)$	– 35	ns
		Wait 1	4×10^9 $2 \cdot f(f_2)$	– 35	
		Wait 0	2×10^9 $2 \cdot f(f_2)$	– 35	
tpxz(E-DZ)	Floating start delay time			10	ns
tpzx(E-DZ)	Floating release delay time		1×10^9 $2 \cdot f(f_2)$	– 30	ns
td(BHE-E)	BHE output delay time	No wait	1×10^9 $2 \cdot f(f_2)$	– 63	ns
		Wait 1			
		Wait 0	3×10^9 $2 \cdot f(f_2)$	– 68	
td(R/W-E)	R/W output delay time	No wait	1×10^9 $2 \cdot f(f_2)$	– 63	ns
		Wait 1			
		Wait 0	3×10^9 $2 \cdot f(f_2)$	– 68	
th(E-BHE)	BHE hold time		1×10^9 $2 \cdot f(f_2)$	– 50	ns
th(E-R/W)	R/W hold time		1×10^9 $2 \cdot f(f_2)$	– 50	ns
td(E-φ1)	φ1 output delay time		0	30	ns

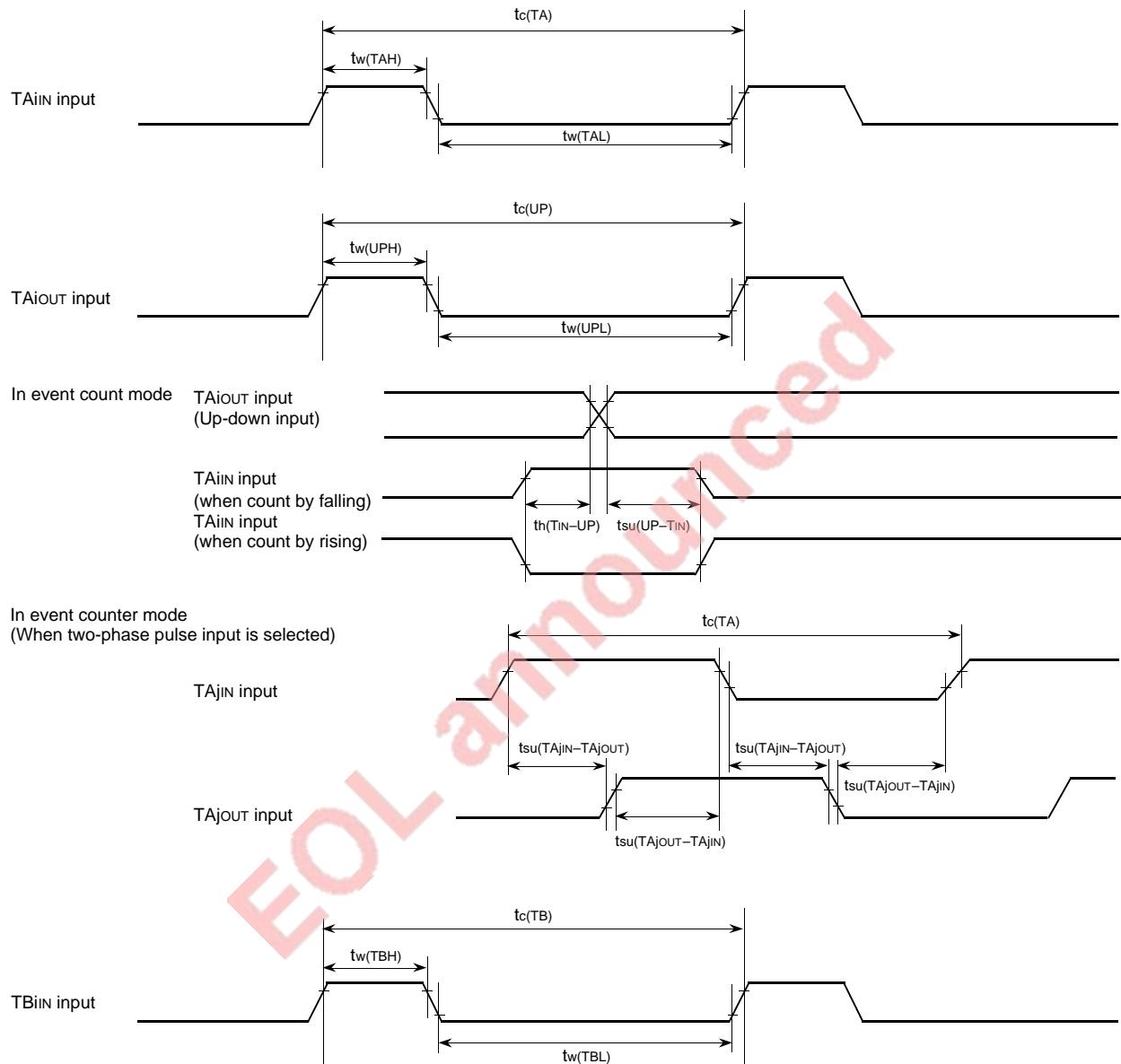
Notes 1. This applies when the main-clock division selection bit = "0".

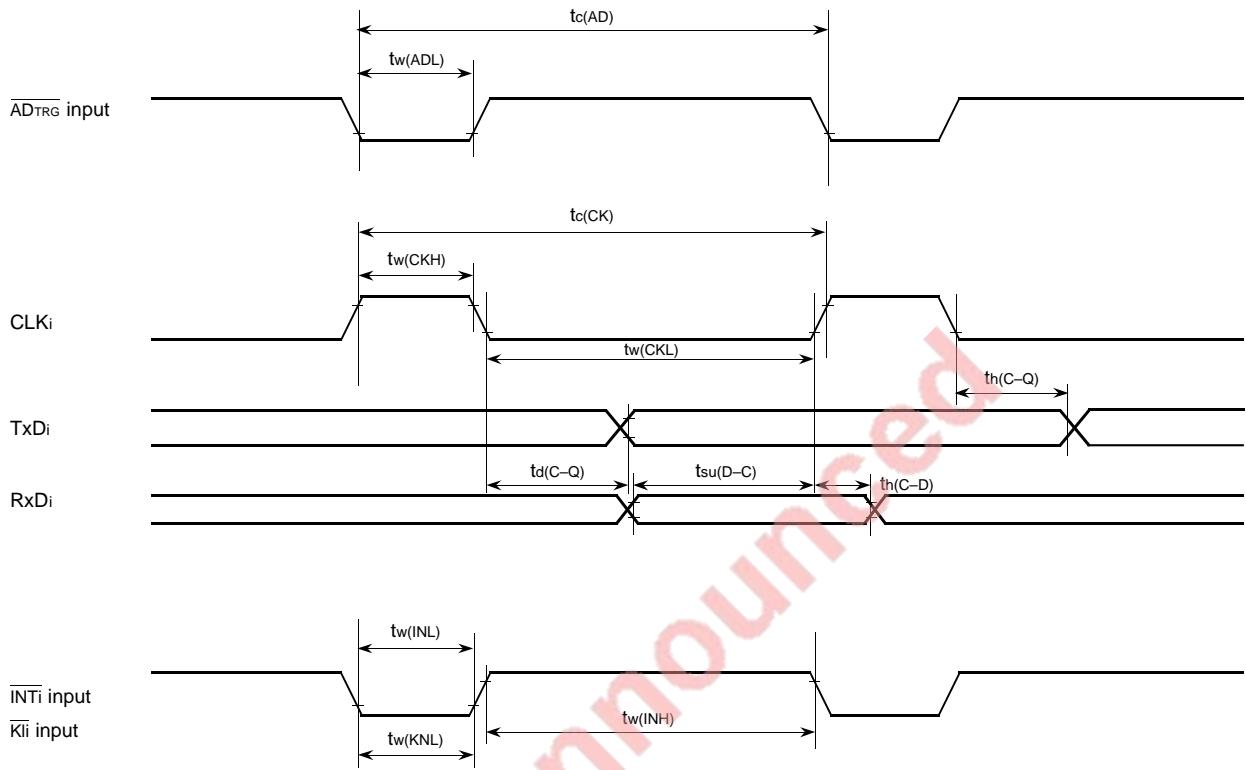
2. f(f₂) represents the clock f₂ frequency.

For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXFP".

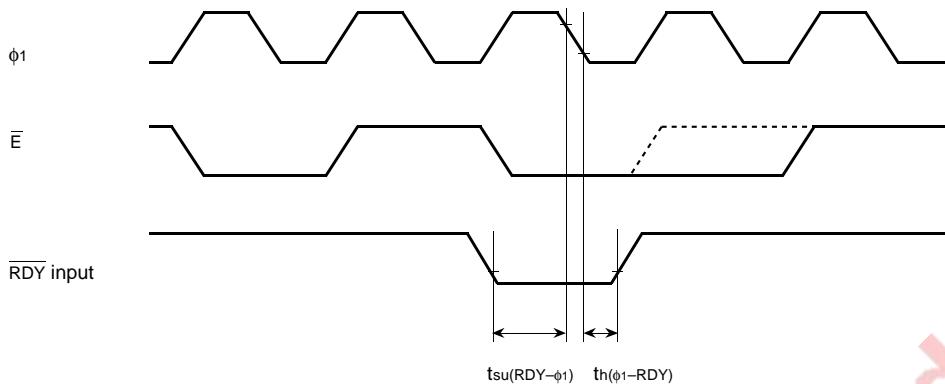
TIMING DIAGRAM



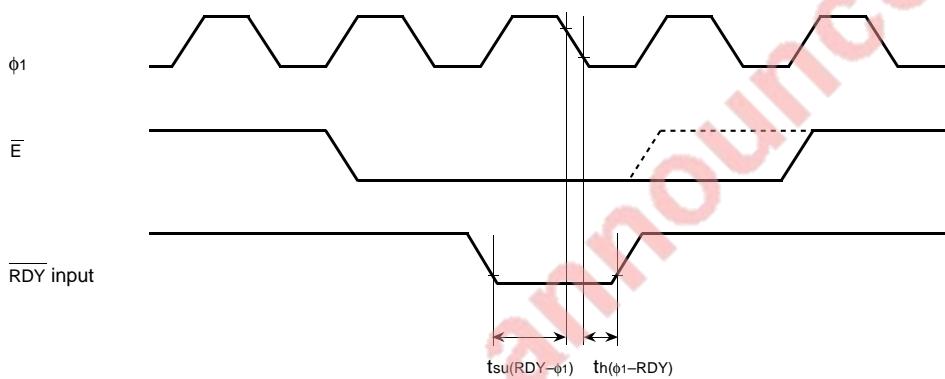




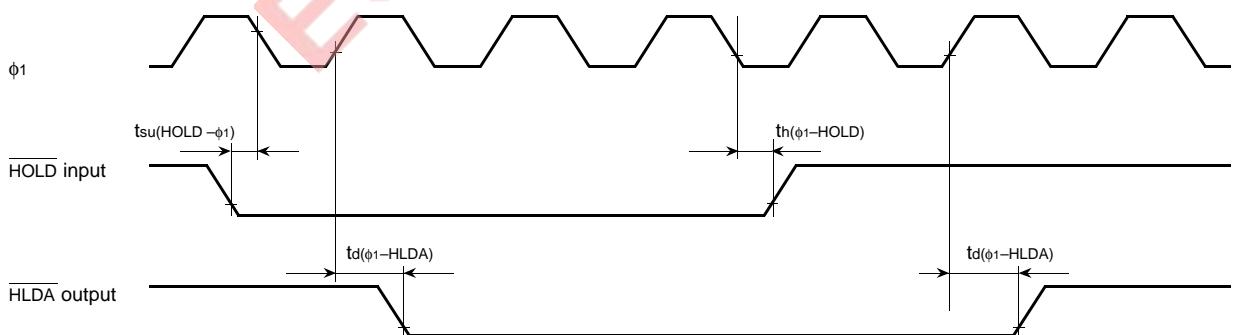
Memory expansion mode and microprocessor mode
(When wait bit = "1")



(When wait bit = "0")



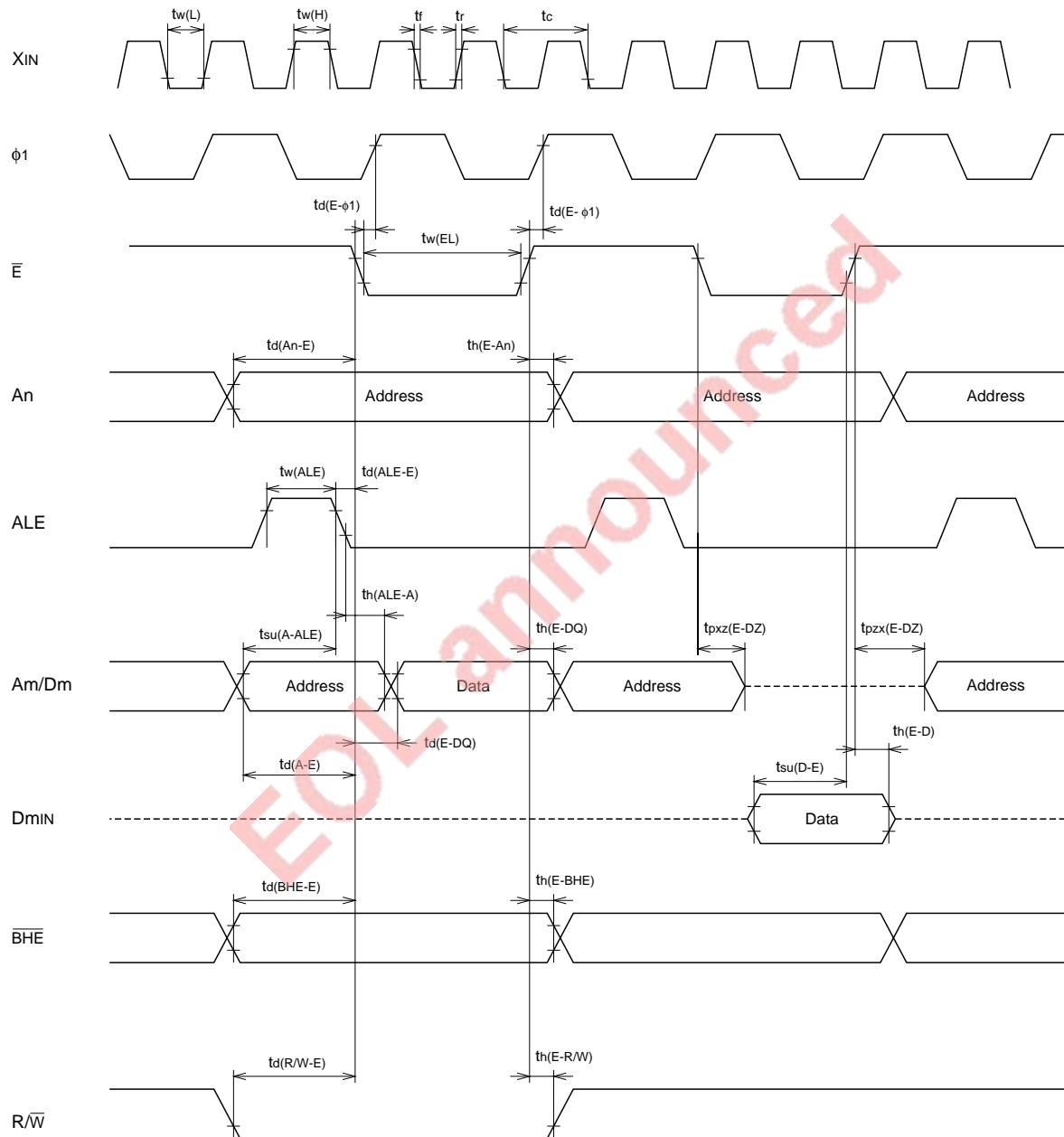
(When wait bit = "1" or "0" in common)



Test conditions

- $V_{CC} = 2.7 - 5.5$ V
- Input timing voltage : $V_{IL} = 0.2$ V_{CC} , $V_{IH} = 0.8$ V_{CC}
- Output timing voltage : $V_{OL} = 0.8$ V, $V_{OH} = 2.0$ V

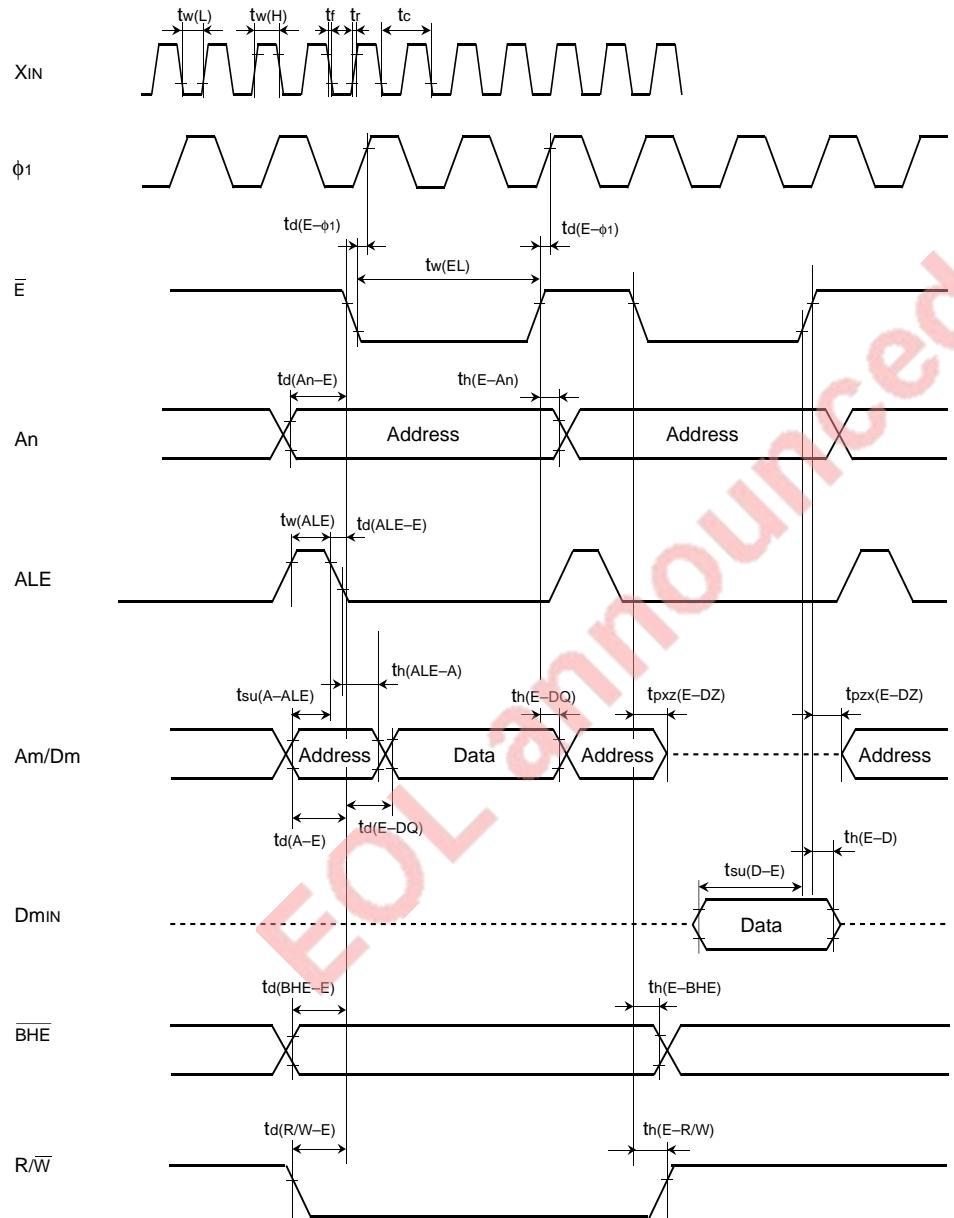
Memory expansion mode and microprocessor mode
(No wait : When wait bit = "1")



Test conditions

- $V_{CC} = 2.7 - 5.5$ V
- Output timing voltage : $V_{OL} = 0.8$ V, $V_{OH} = 2.0$ V
- Data input DMIN : $V_{IL} = 0.16$ V_{CC} , $V_{IH} = 0.5$ V_{CC}

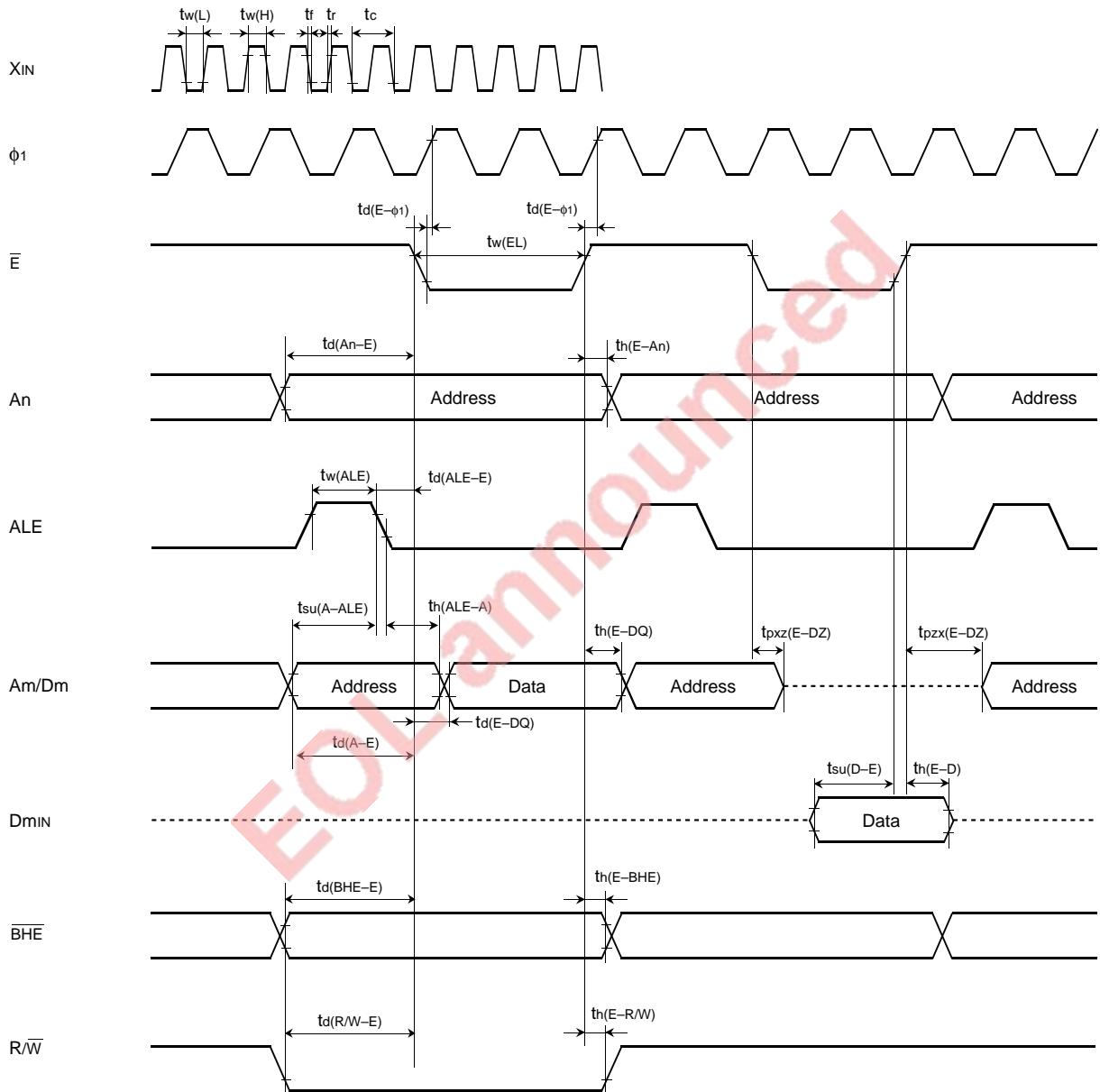
Memory expansion mode and microprocessor mode
(Wait 1 : The external area is accessed when wait bit = "0" and wait selection bit = "1".)



Test conditions

- $V_{CC} = 2.7 - 5.5$ V
- Output timing voltage : $V_{OL} = 0.8$ V, $V_{OH} = 2.0$ V
- Data input D_{MIN} : $V_{IL} = 0.16$ V_{CC} , $V_{IH} = 0.5$ V_{CC}

Memory expansion mode and microprocessor mode
(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



Test conditions

- $V_{CC} = 2.7 - 5.5$ V
- Output timing voltage : $V_{OL} = 0.8$ V, $V_{OH} = 2.0$ V
- Data input D_{MIN} : $V_{IL} = 0.16$ V_{CC} , $V_{IH} = 0.5$ V_{CC}

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

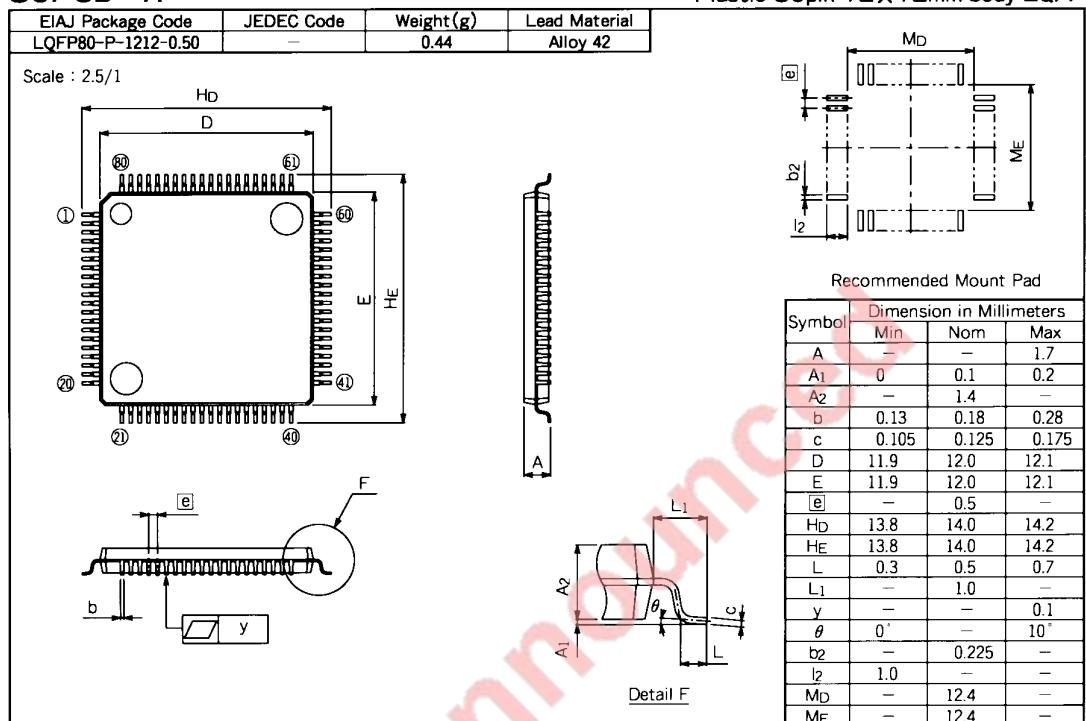
MITSUBISHI MICROCOMPUTERS

M37733M4LXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

PACKAGE OUTLINE

80P6D-A



7700 FAMILY MASK ROM ORDER CONFIRMATION FORM
SINGLE-CHIP 16-BIT MICROCOMPUTER
M37733M4LXXXHP
MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked **※**

※ Customer	Company name	TEL ()	Responsible officer Issuance signatures	Supervisor
	Date issued	Date:		

※1. Confirmation

Specify the name of the product being ordered.

Three sets of EPROMs are required for each pattern (Check in the appropriate box).

If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based on this data.

We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data.

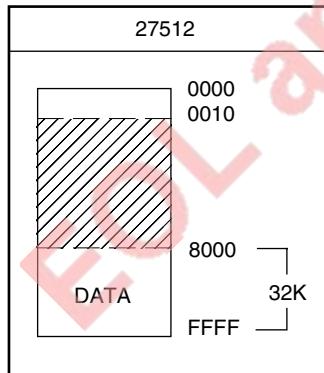
Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas

--	--	--	--

(hexadecimal notation)

EPROM Type :



- (1) Set "FF16" in the shaded area.
- (2) Address 016 to 1016 are the area for storing the data on model designation and options. This area must be written with the data shown below.

Details for option data are given next in the section describing the STP instruction option.

Address and data are written in hexadecimal notation.

	Address	Address	Address
4D	0	4C	8
33	1	FF	9
37	2	FF	A
37	3	FF	B
33	4	FF	C
33	5	FF	D
4D	6	FF	E
34	7	FF	F

※2. STP instruction option

One of the following sets of data should be written to the option data address (1016) of the EPROM you have ordered.

Check in the appropriate box.

<input type="checkbox"/> STP instruction enable	0116	Address 1016
<input type="checkbox"/> STP instruction disable	0016	Address 1016

※3. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6D Mark Specification Form (for M37733M4LXXXHP) and attach to the Mask ROM Order Confirmation Form.

※4. Comments

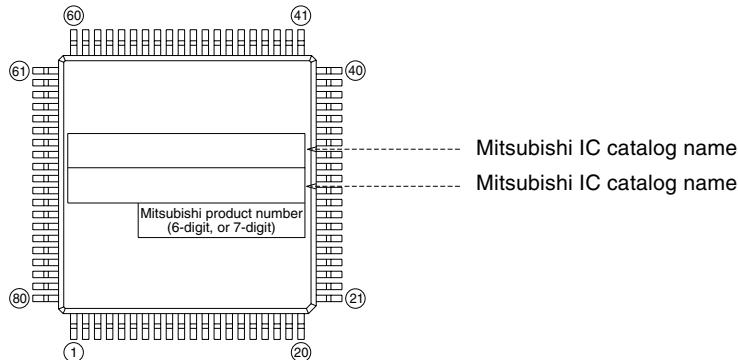
80P6S (80-PIN QFP) MARK SPECIFICATION FORM

80P6D, 80P6Q (80-PIN Fine-pitch QFP)

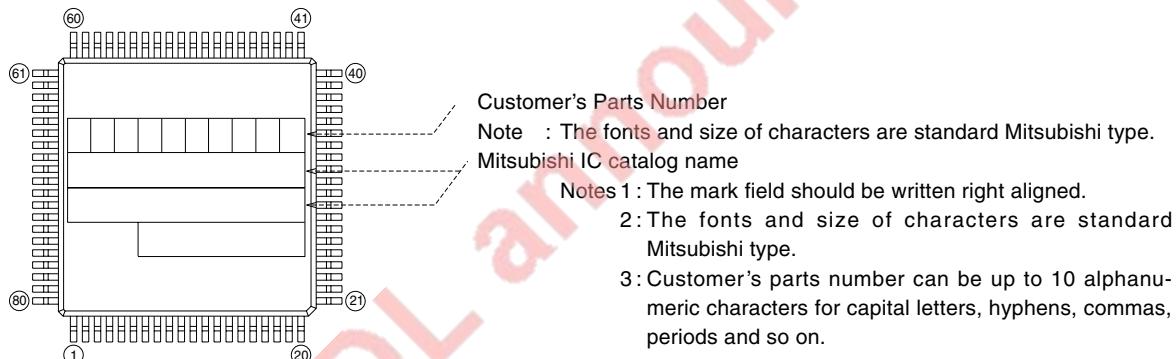
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

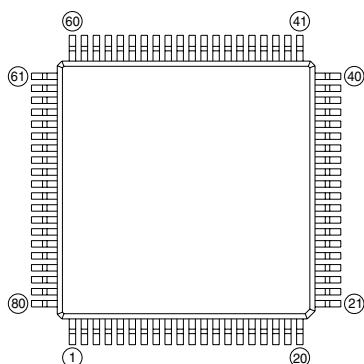
A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi IC Catalog Name



C. Special Mark Required



Notes 1 : If Special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible. Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.

2 : If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.

For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37733M4LXXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

EOL announced

Renesas Technology Corp.

Nippon Bldg., 6-2, Otemachi 2-chome, Chiyoda-ku, Tokyo, 100-0004 Japan

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- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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REVISION DESCRIPTION LIST

M37733M4LXXXHP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	970604
1.01	<p>The following are added:</p> <ul style="list-style-type: none">•MASK ROM ORDER CONFIRMATION FORM•MARK SPECIFICATION FORM	980526