

4 Ω , 360 MHz, Dual SPST Analog Switches

DESCRIPTION

The DG3537, DG3538, DG3539, DG3540 are dual SPST analog switches which operate from 1.8 V to 5.5 V single rail power supply. They are design for audio, video, and USB switching applications.

The devices have 4 Ω on-resistance and 360 MHz 3 dB bandwidth. 0.2 Ω on-resistance matching and 1 Ω flatness make the device high linearity. The devices are 1.6 V logic compatible within the full operation voltage range.

These switches are built on a sub-micron high density process that brings low power consumption and low voltage performance.

The switches are packaged in MICRO FOOT chip scale package of 3 x 3 bump array.

As a committed partner to the community and environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For MICRO FOOT analog switch products manufactured with tin/silver/copper (SnAgCu) device termination, the lead (Pb)-free "E1" suffix is being used as a designator.

FEATURES

- 1.8 V to 5.5 V operation
- 3 Ω at 2.7 V R_{ON}
- 360 MHz - 3 dB bandwidth
- ESD method 3015.7 > 2 kV
- Latch-up current 0.300 mA (JESD 78)
- 1.6 V logic compatible

BENEFITS

- Space saving MICRO FOOT[®] package
- High linearity
- Low power consumption
- High bandwidth
- Full rail Signal swing range

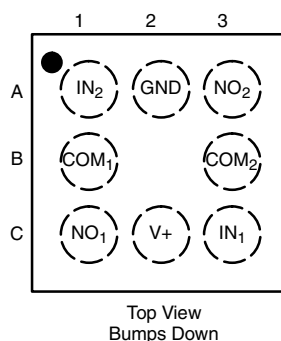
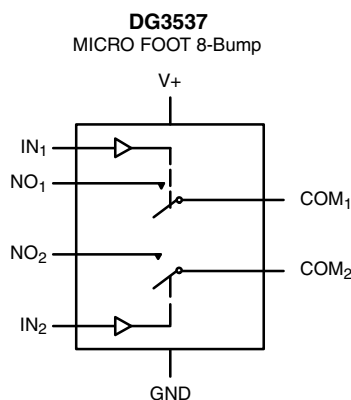
APPLICATIONS

- Cellular phones
- MP3
- Media players
- Modems
- Hard drives
- PCMCIA

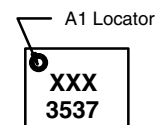


RoHS
COMPLIANT

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

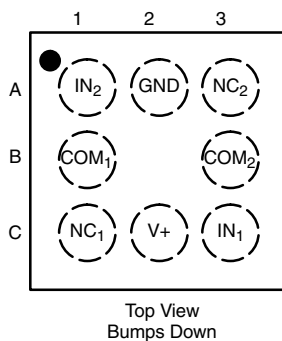
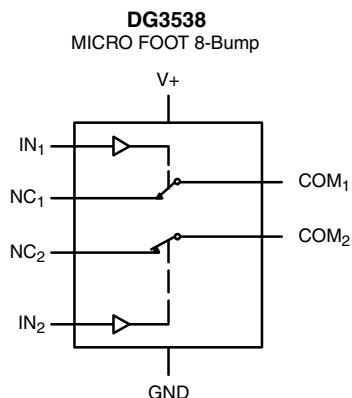


Device Marking



3537 = Device Marking
xxx = Data/Lot Traceability Code

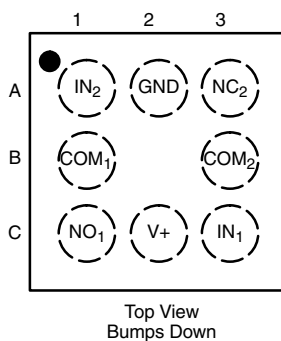
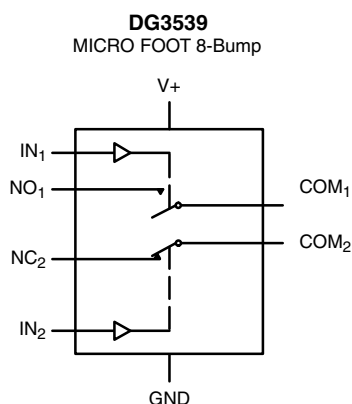
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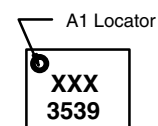
Device Marking



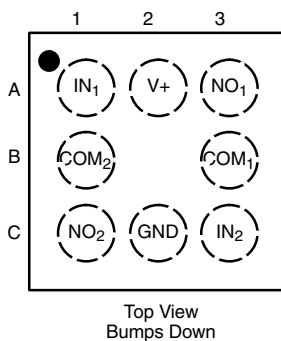
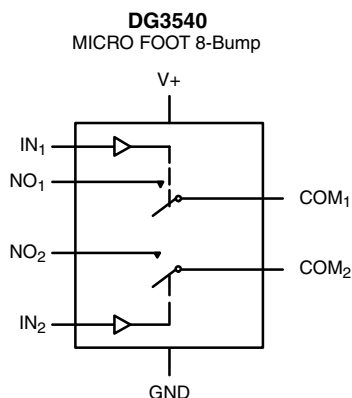
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xxx = Data/Lot Traceability Code



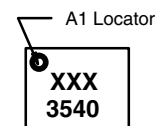
Device Marking



3539 = Device Marking
xxx = Data/Lot Traceability Code



Device Marking



3540 = Device Marking
xxx = Data/Lot Traceability Code

TRUTH TABLE

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp. Range	Package	Part Number
- 40 °C to 85 °C	MICRO FOOT: 8 Bump (3 x 3, 0.5 mm Pitch, 238 µm Bump Height)	DG3537DB-T5-E1 DG3538DB-T5-E1 DG3539DB-T5-E1 DG3540DB-T1-E1

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Limit	Unit
Reference V+ to GND	- 0.3 to + 6	V
IN, COM, NC, NO ^a	- 0.3 to (V+ + 0.3 V)	
Continuous Current (NO, NC, COM)	± 100	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)	± 200	
Storage Temperature	(D Suffix)	°C
Package Solder Reflow Conditions ^b	IR/Convection	
ESD per Method 3015.7	> 2	kV
Power Dissipation (Packages) ^c	MICRO FOOT: 8 Bump (3 x 3 mm) ^d	mW

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. Refer to IPC/JEDEC (J-STD-020B)
c. All bumps welded or soldered to PC Board.
d. Derate 5.0 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.7 to 3.6 V, V _{IN} = 0.5 V or 1.4 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance ^d	R _{ON}	V+ = 2.7 V, V _{COM} = 0.2/1.5 V I _{NO} , I _{NC} = 10 mA	Room Full		3	4 4.3	Ω
R _{ON} Flatness ^d	R _{ON} Flatness		Room		0.75	1.2	
On-Resistance Match Between Channels ^d	ΔR _{DS(on)}		Room			0.25	
Switch Off Leakage Current ^f	I _{NO(off)} I _{NC(off)}	V+ = 3.6 V, V _{NO} , V _{NC} = 0.3 V/3.3 V, V _{COM} = 3.3 V/0.3 V	Room Full	- 2 - 20		2 20	nA
	I _{COM(off)}		Room Full	- 2 - 20		2 20	
Channel-On Leakage Current ^f	I _{COM(on)}	V+ = 3.6 V, V _{NO} , V _{NC} = V _{COM} = 0.3 V/3.3 V	Room Full	- 2 - 20		2 20	
Digital Control							
Input High Voltage ^d	V _{INH}		Full	1.4			V
Input Low Voltage	V _{INL}		Full			0.5	
Input Capacitance	C _{in}		Full		8		pF
Input Current ^f	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	1		1	μA

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.7 to 3.6 V, VIN = 0.5 V or 1.4 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Dynamic Characteristics							
Turn-On Time	tON	V+ = 2.7 V, VNO or VNC = 1.5 V RL = 300 Ω, CL = 35 pF	Room Full		16	46 48	ns
Turn-Off Time	tOFF		Room Full		7	37 39	
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 2 V, RGEN = 0 Ω	Room		1		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		- 78.5		dB
Crosstalk ^d	XTALK		Room		- 113		
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 10 MHz	Room		- 58		
Crosstalk ^d	XTALK		Room		- 66		
Off Capacitance ^d	CNO/NC(off)	VIN = 0 or V+, f = 1 MHz	Room		8		pF
	CCOM(off)		Room		14		
Channel-On Capacitance ^d	CNO/NC(on)		Room		27		
	CCOM(on)		Room		27		
Power Supply							
Power Supply Current	I+	VIN = 0 or V+	Room Full		0.001	1.0 1.0	μA



SPECIFICATIONS (V+ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 4.2 to 5.5 V, VIN = 0.8 V or 2.0 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Analog Switch							
Analog Signal Range ^d	VNO, VNC, VCOM		Full	0		V+	V
On-Resistance ^d	RON	V+ = 4.2 V, VCOM = 0.5/3.5 V INO, INC = 10 mA	Room Full		2.6	3.5 3.7	Ω
rON Flatness ^d	RON Flatness		Room		0.8	1.2	
On-Resistance Match Between Channels ^d	ΔRDS(on)		Room			0.2	
Switch Off Leakage Current	INO(off) INC(off)	V+ = 5.5 V, VNO, VNC = 1.0 V/4.5 V, VCOM = 4.5 V/1.0 V	Room Full	- 2 - 20		2 20	nA
	ICOM(off)		Room Full	- 2 - 20		2 20	
Channel-On Leakage Current	ICOM(on)	V+ = 5.5 V, VNO, VNC = VCOM = 1.0 V/4.5 V	Room Full	- 2 - 20		2 20	
Digital Control							
Input High Voltage ^d	VINH		Full	2.0			V
Input Low Voltage	VINL		Full			0.8	
Input Capacitance	Cin		Full		8		pF
Input Current	IINL or IINH	VIN = 0 or V+	Full	1		1	μA
Dynamic Characteristics							
Turn-On Time	tON	V+ = 4.2 V, VNO or VNC = 3.0 V RL = 300 Ω, CL = 35 pF	Room Full		11	41 43	ns
Turn-Off Time	tOFF		Room Full		7	37 39	
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 2 V, RGEN = 0 Ω	Room		1		pC
Off Capacitance ^d	CNO/NC(off)	VIN = 0 or V+, f = 1 MHz	Room		8		pF
	CCOM(off)		Room		14		
Channel-On Capacitance ^d	CNO/NC(on)		Room		28		
	CCOM(on)		Room		28		
Power Supply							
Power Supply Current	I+	VIN = 0 or V+	Room Full		0.001	1.0 1.0	μA

Notes:

a. Room = 25 °C, Full = as determined by the operating suffix.

b. Typical values are for design aid only, not guaranteed nor subject to production testing.

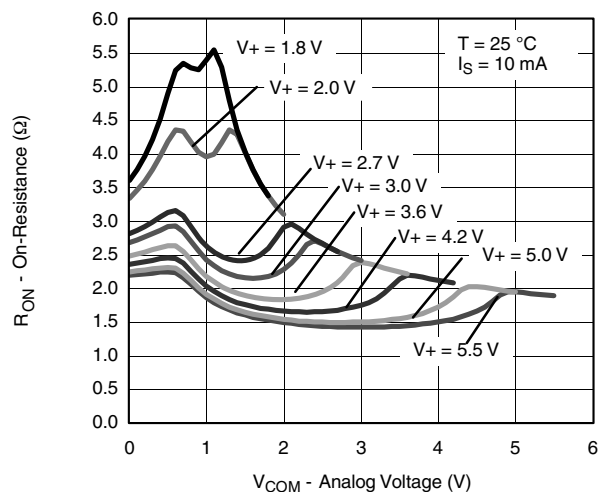
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

d. Guarantee by design, nor subjected to production test.

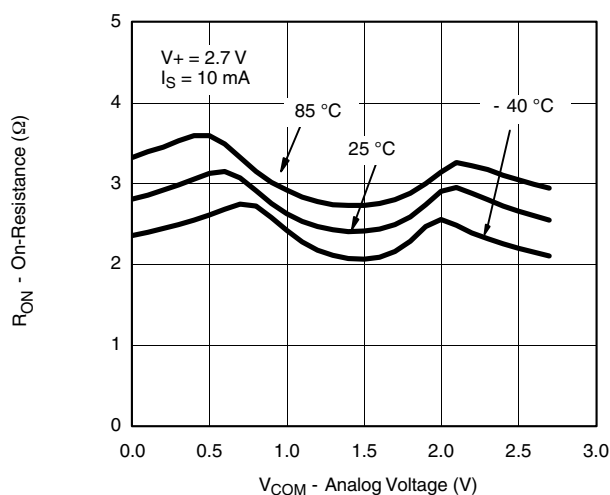
e. V_{IN} = input voltage to perform proper function.

f. Guaranteed by 5 V leakage testing, not production tested.

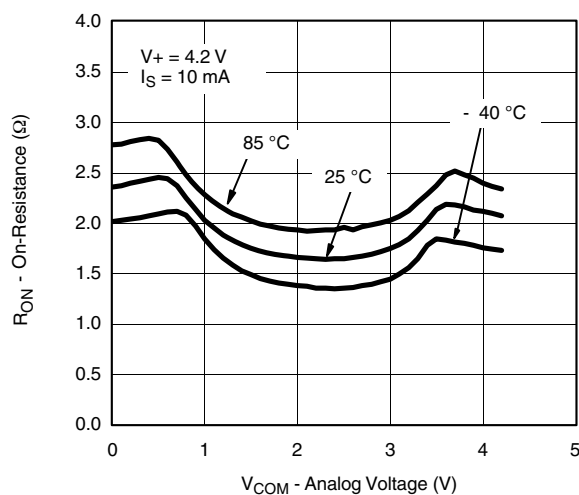
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



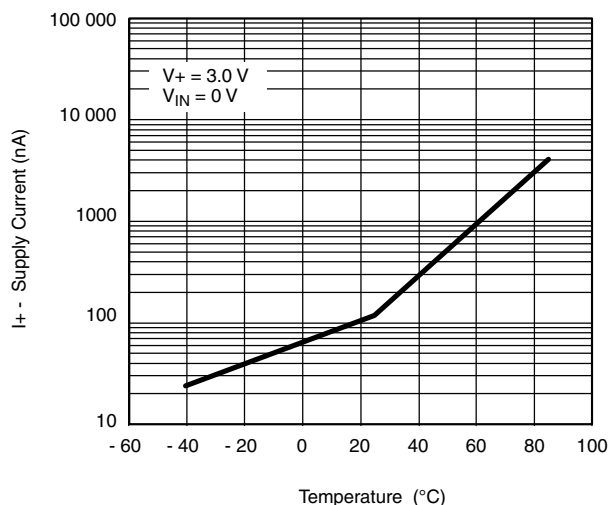
R_{ON} vs. V_{COM} and Supply Voltage



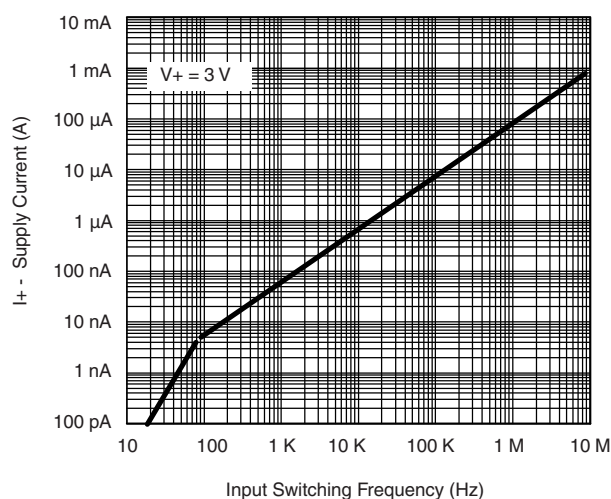
R_{ON} vs. Analog Voltage and Temperature



R_{ON} vs. Analog Voltage and Temperature

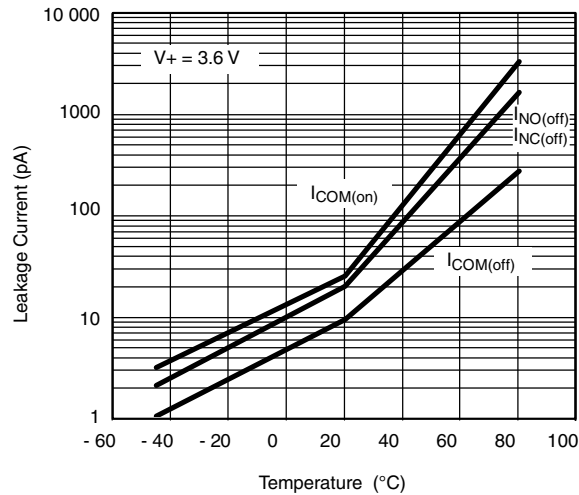


Supply Current vs. Temperature

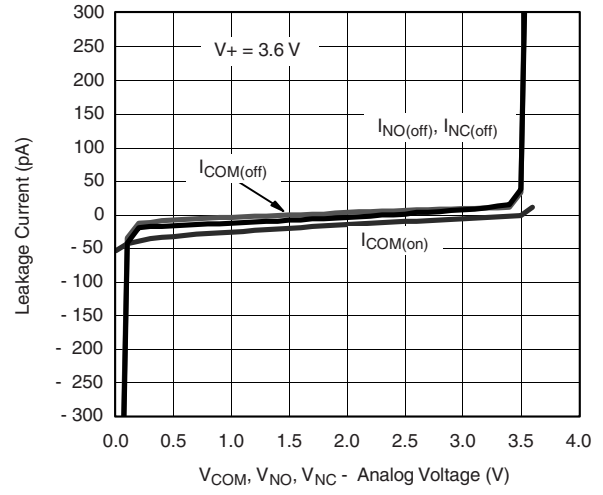


Supply Current vs. Input Switching Frequency

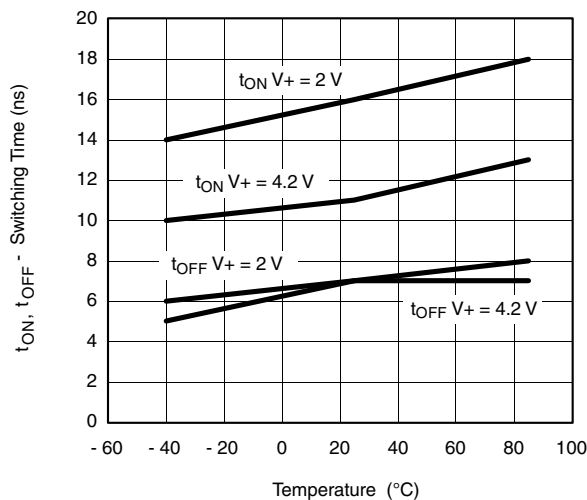
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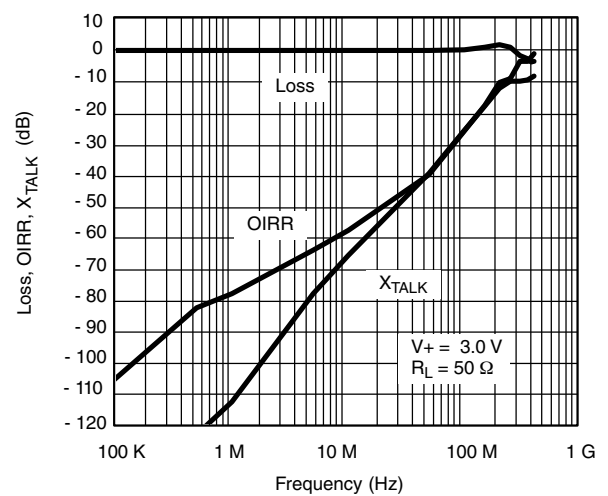
Leakage Current vs. Temperature



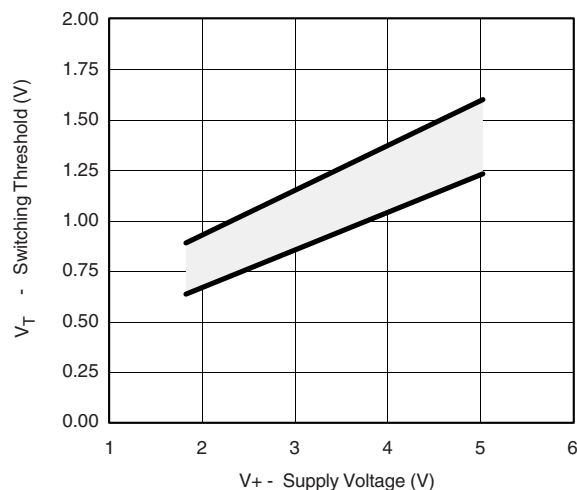
Leakage vs. Analog Voltage



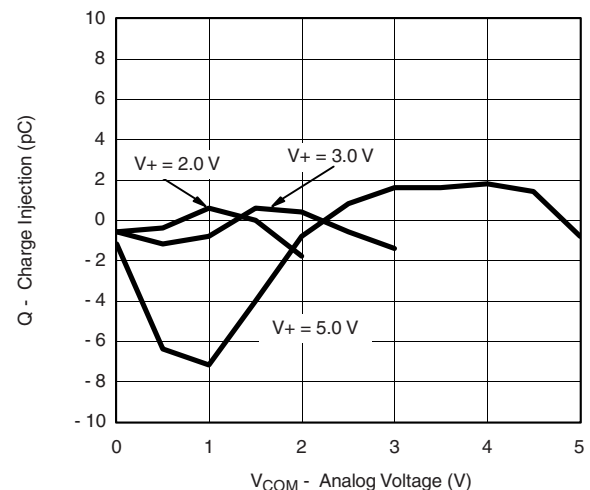
Switching Time vs. Temperature



Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

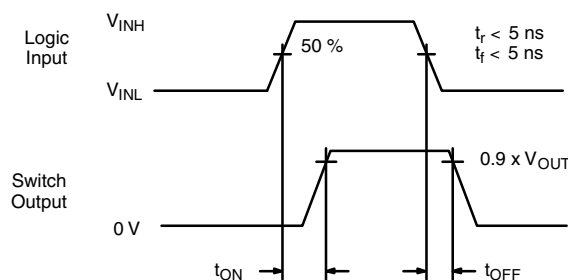
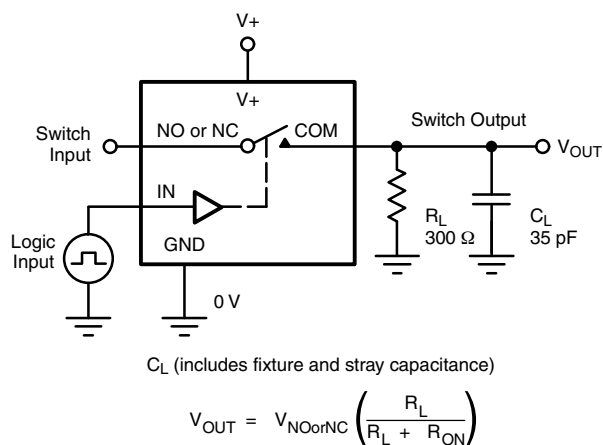


Switching Threshold vs. Supply Voltage



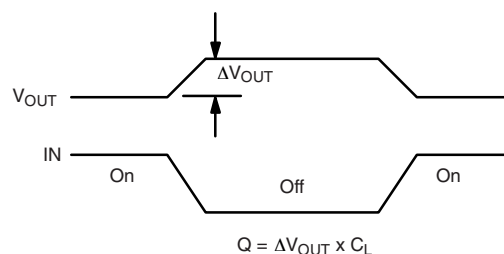
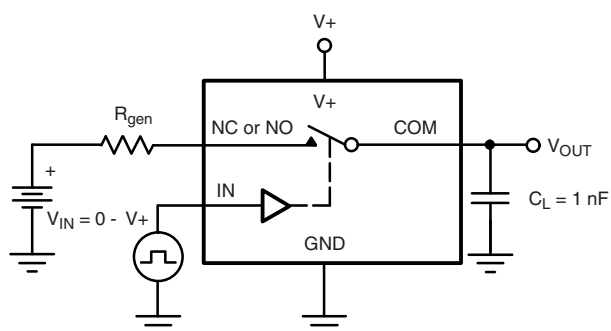
Charge Injection vs. Analog Voltage

TEST CIRCUITS



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 2. Charge Injection

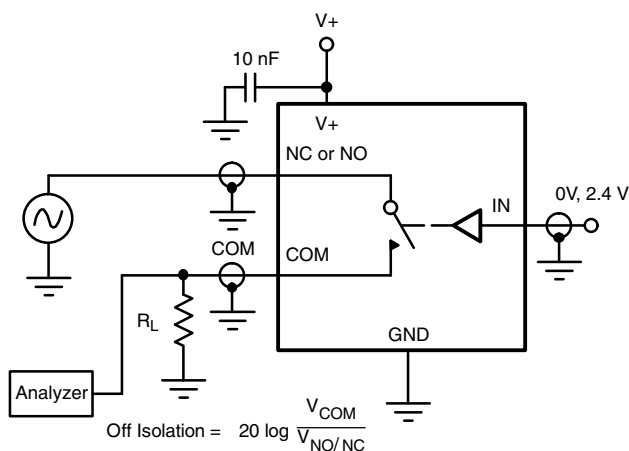


Figure 3. Off-Isolation

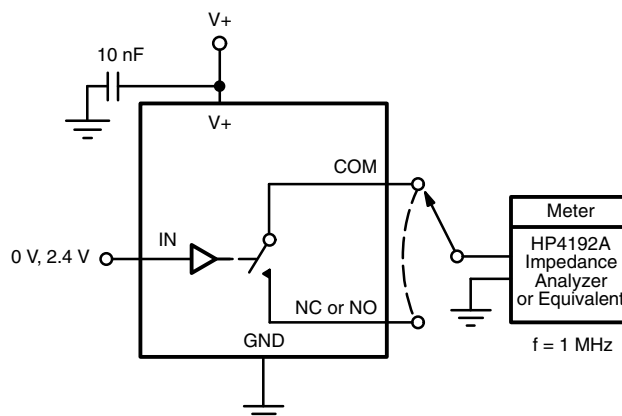
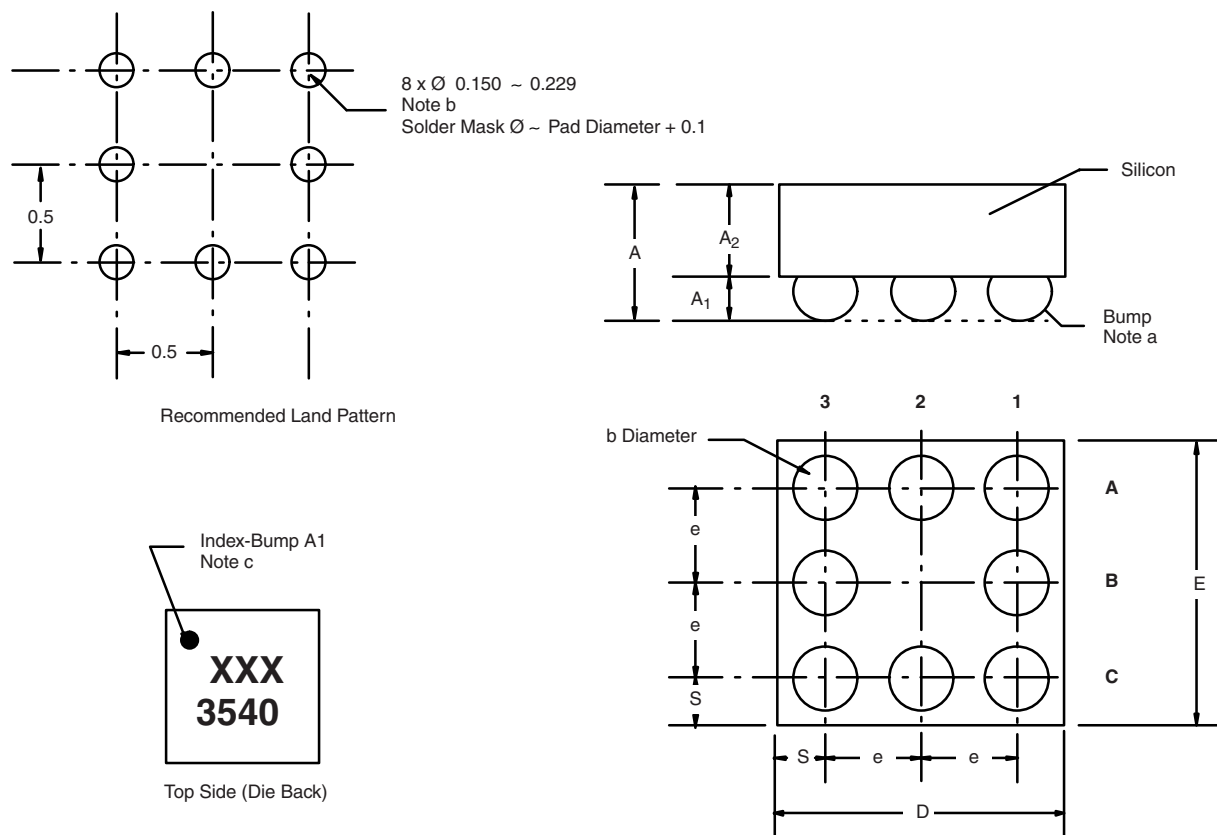


Figure 4. Channel Off/On Capacitance

PACKAGE OUTLINE

MICRO FOOT: 8 BUMP (3 x 3, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes (Unless Otherwise Specified):

- a. Bump is Lead (Pb)-free Sn/Ag/Cu.
- b. Non-solder mask defined copper landing pad.
- c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

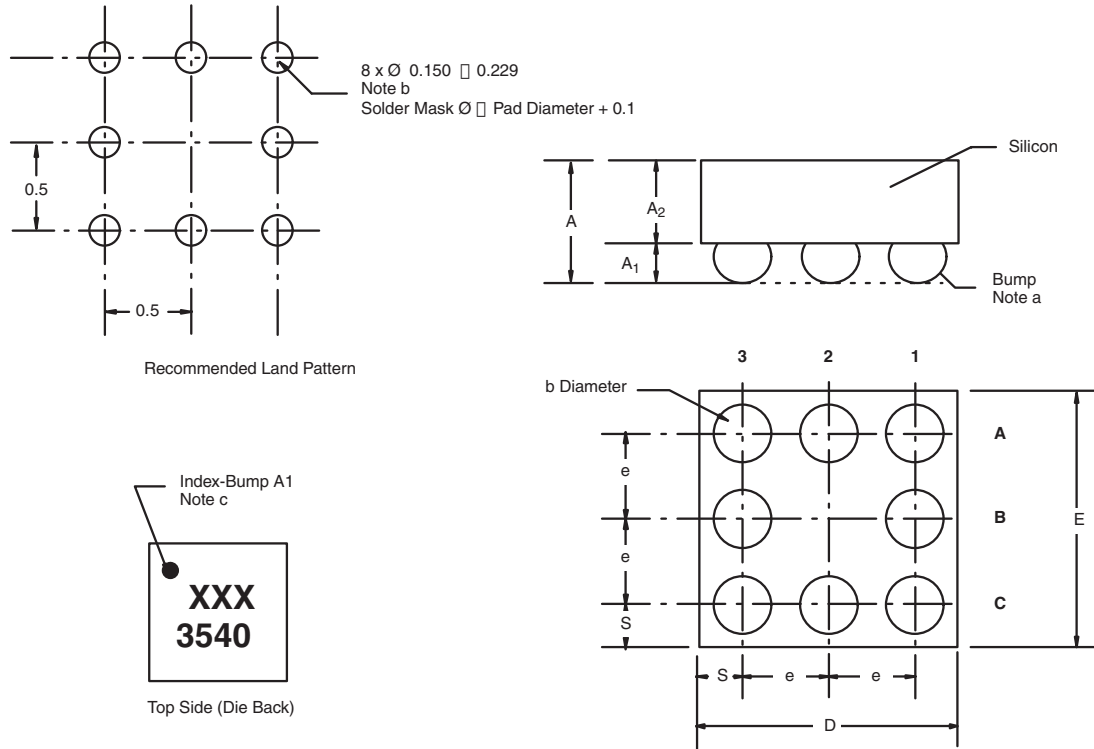
Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.688	0.753	0.0271	0.0296
A ₁	0.218	0.258	0.0086	0.0102
A ₂	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.480	1.520	0.0583	0.0598
E	1.480	1.520	0.0583	0.0598
e	0.5 BASIC		0.0197 BASIC	
S	0.230	0.270	0.0091	0.0106

Notes:

- a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73320.

MICRO FOOT: 8-BUMP (3 mm x 3 mm, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes

(unless otherwise specified)

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ECN: S11-1065-Rev. A, 13-Jun-11
 DWG: 6002



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