Features

- DSL Triple Outputs (Independantly Regulated)
- Input Voltage Range: 36V to 75V
- 1500VDC Isolation
- On/Off Control
- Current Limit
- Short Circuit Protection (All Outputs)
- Fixed Frequency Operation
- Over-Temperature Shutdown
- Under-Voltage Lockout
- Space Saving Package: 1.9 sq. in. PCB Area (suffix N)
- Solderable Copper Case
- Safety Approvals: UL60950 CSA 22.2 950 VDE EN60950

Description

The PT4840 Excalibur™ power modules are a series of isolated triple-output DC/DC converters that operate from a standard (–48V) central office supply. Rated for up to 65W, these regulators are appropriate for powering both analog and mixed-signal circuitry. A typical application is a chip-set for an ADSL/DSL line card.

The output voltage combinations offered by the PT4840 series provide power for a low-voltage processor core, the associated digital circuitry, and analog support circuitry.

The PT4840 series incorporates many features to simplify system integration. These include a flexible On/Off control, over-temperature protection, and an input under-voltage lock-out. All outputs are current limited and short-circuit protected. In addition, the low-voltage outputs for processor core and digital circuitry meet the power-up and power-down sequencing requirements of popular DSP ICs.

The PT4840 series is housed in a space-saving solderable case. The module requires no external heat sink and can occupy as little as 1.97 in² of PCB area.

Ordering Information

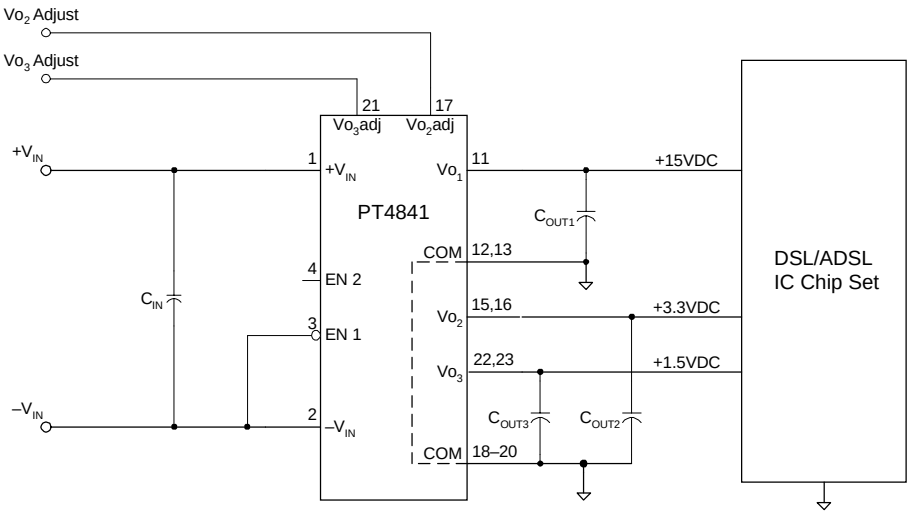
PT4841❑ = +15/+3.3/+1.5V (65W)
PT4842❑ = +12/+3.3/+1.8V (62W)

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	**N**	(EKD)
Horizontal	**A**	(EKA)
SMD	**C**	(EKC)

(Reference the applicable package code drawing for the dimensions and PC layout)

Typical Application



C_{in} = Optional
C_{out} = Optional; See specifications
EN1 & EN2 pins: See On/Off Enable Logic

Environmental Specifications

Characteristics	Symbols	Conditions		Min	Typ	Max	Units
Operating Temperature Range	T_a	Over V_{in} Range		–40	—	85 (i)	°C
Over-Temperature Protection	OTP	Case temperature		100	—	—	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module pins or case		—	—	215 (ii)	°C
Storage Temperature	T_s	—		–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted		—	500	—	G's
Mechanical Vibration		Mil-STD-883D Method 2007.2 20-2000 Hz	Suffix N Suffix A, C	— —	10 (iii) 20 (iii)	— —	G's
Weight	—	Vertical/Horizontal		—	90	—	grams
Flammability	—	Meets UL 94V-O					

Notes: *(i) See SOA curves or consult factory for appropriate derating.*
(ii) During solder reflow of SMD package version do not elevate the module case, pins, or internal component temperatures above a peak of 215°C. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products," (SLTA051).
(iii) Only the case pins on through-hole pin configurations (N & A) must be soldered. For more information see the applicable package outline drawing.

Pin Configuration

Pin	Function
1	+Vin
2	–Vin
3	EN 1
4	EN 2
5	TEMP
6	Do Not Connect
7	Do Not Connect
8	Pin Not Present
9	Pin Not Present

Pin	Function
10	Pin Not Present
11	$+Vo_1$
12	COM
13	COM
14	Pin Not Present
15	$+Vo_2$
16	$+Vo_2$
17	Vo_2 adjust

Pin	Function
18	COM
19	COM
20	COM
21	Vo_3 adjust
22	$+Vo_3$
23	$+Vo_3$
24	Pin Not Present
25	Do Not Connect
26	Do Not Connect

Note: Shaded functions indicate those pins that are at primary-side potential.

On/Off Enable Logic

Pin 3	Pin 4	Output Status
1	×	Off
0	1	On
×	0	Off

Notes:
Logic 1 =Open collector
Logic 0 = –Vin (pin 2) potential

For positive Enable function, connect pin 3 to pin 2 and use pin 4.

For negative Enable function, leave pin 4 open and use pin 3.

Pin Descriptions

+Vin: The positive input supply for the module with respect to –Vin. When powering the module from a –48V telecom central office supply, this input is connected to the primary system ground.

–Vin: The negative input supply for the module, and the 0VDC reference for the EN 1, EN 2, and TEMP inputs. When powering the module from a +48V supply, this input is connected to the 48V(Return).

EN 1: The negative logic input that activates the module output. This pin is referenced to $–V_{in}$. A low-level voltage at this pin enables the module's outputs, and a high impedance impedance disables the module's outputs. If not used, the pin must be connected to $–V_{in}$.

EN 2: The positive logic input that activates the module output. This pin is referenced to $–V_{in}$. A high impedance at this pin enables the module's outputs. If not used, the pin should be left open circuit.

TEMP: This pin produces an output signal that tracks a temperature that is approximately the module's metal case. The output voltage is referenced to –Vin and rises approximately 10mV/°C from an intital value of 0.1VDC at –40°C. The signal is available whenever the module is supplied with a valid input voltage, and is independant of the enable logic status. (**Note:** *A load impedance of less than 1MΩ will adversly affect the module's over-temperature shutdown threshold. Use a high-impedance input when monitoring this signal.)*

Vo_1: The highest regulated output voltage, which is referenced to the COM node. The output may be used to power analog support circuitry.

Vo_2: The regulated output that is designed to power logic or I/O circuitry. It is referenced to the COM node.

Vo_3: The low-voltage regulated output that provides power for a micro, processor, ASIC, or DSP core, and is referenced to the COM node.

COM: The secondary return reference for the module's three regulated output voltages. It is DC isolated from the input supply pins.

Vo_2 Adjust: Using a single resistor, this pin allows Vo_2 to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

Vo_3 Adjust: Using a single resistor, this pin allows Vo_3 to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

PT4841 Electrical Specifications

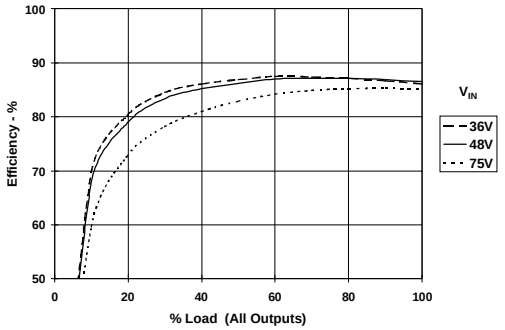
(Unless otherwise stated, the operating conditions are:- T_a =25°C, V_{in} =48V, and Io_n =0.5Io_nmax)

Characteristics	Symbols	Conditions		PT4841 Min	PT4841 Typ	PT4841 Max	Units
Output Power	P_o	Each output:	Vo_1 (15V)	—	—	41 (1)	W
			Vo_2 (3.3V)	—	—	20 (1)	
			Vo_3 (1.5V)	—	—	10.5 (1)	
		Total (all three outputs)		—	—	65 (1)	W
Output Current	I_o		Io_1 (15V)	0	—	2.7	A
			Io_2 (3.3V)	0	—	6 (2)	
			Io_3 (1.5V)	0	—	7 (2)	
		Maximum (Io_2 + Io_3)		—	—	11 (2)	A
Input Voltage Range	V_{in}			36	—	75	V
Set-Point Voltage	V_o		Vo_1	—	15.2	—	V
			Vo_2	—	3.3	—	
			Vo_3	—	1.5	—	
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1	—	±0.5	—	%V_o
			Vo_2/Vo_3	—	±0.8	—	
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	0.1	0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	0.2	0.5	%V_o
Cross Regulation	Reg_{cross}	Any one output vs. other outputs		—	—	1.0	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a≤+85°C	Vo_1	15	—	15.75 (3)	V
			Vo_2	3.2	—	3.4 (3)	
			Vo_3	1.45	—	1.55 (3)	
Efficiency	η	P_o =$P_o$max		—	85	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n	Co_1/Co_2/Co_3 =10µF	Vo_1	—	50	100 (4)	mV_{pp}
			Vo_2	—	20	50 (4)	
			Vo_3	—	20	50 (4)	
Transient Response	t_{tr}	0.1A/µs load step, 50% to 75% $I_o$max		—	30	—	µSec
	V_{os}	V_o over/undershoot		—	5	—	%V_o
Output Adjust Range	$V_o$adj		Vo_2 / Vo_3	±10	—	—	%V_o
Current Limit Threshold	I_{LIM}		Io_1	—	4	—	A
			Io_2 + Io_3	—	16	—	
Over Current Shutdown Delay	t_{sd}	Time period prior to latched shutdown		—	200 (5)	—	ms
Switching Frequency	f_s	Over V_{in} and I_o ranges		450	500	550	kHz
Under Voltage Lockout	V_{on}	V_{in} increasing		—	34	—	V
	V_{off}	V_{in} decreasing		—	32	—	
Enable Control (pins 2 & 3)		Referenced to –V_{in} (pin 2)					
High-Level Input Voltage	V_{IH}			4.0	—	70 (6)	V
Low-Level Input Voltage	V_{IL}			–0.2	—	0.8 (6)	
Low-Level Input Current	I_{IL}	V_{in} =75V		—	0.16	0.25	mA
Standby Input Current	I_{in} standby	pins 2 & 4 connected		—	8	10 (3)	mA
Internal Input Capacitance	C_{int}			—	2	—	µF
External Output Capacitance	Co_1			0	—	330 (7)	µF
	Co_2			0	—	5,000 (7)	
	Co_3			0	—	10,000 (7)	
Temperature Sense	V_{temp}	Output voltage at temperatures:-	–40°C	—	0.1 (8)	—	V
			100°C	—	1.5 (8)	—	
Primary/Secondary Isolation	V_{iso}			1500	—	—	V
	C_{iso}			—	1500	—	pF
	R_{iso}			10	—	—	MΩ

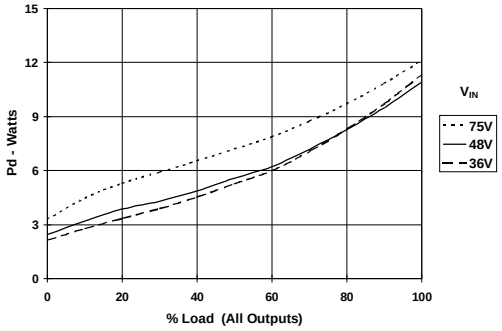
Notes: *(1) The sum total power delivered from all three regulated outputs, Vo_1, Vo_2, and Vo_3, cannot exceed 65 watts.*
(2) The sum-total current from outputs Vo_2, and Vo_3 cannot exceed 11ADC.
(3) Limits are guaranteed by design.
(4) The ripple and noise is measured with a 10µF tantalum capacitor across each output.
(5) After latched shutdown, the module may be reset cycling the input power.
(6) The Enable inputs (pins 3 & 4) have internal pull-ups. Leaving pin 4 open-circuit and connecting pin 3 to –V_{in} allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 5.1V.
(7) Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. For more information refer to the application note regarding capacitor selection.
(8) Voltage output at "TEMP" pin is defined by the equation:- V_{TEMP} = 0.5 + 0.01·T, where T is the sensed temperature in degrees centigrade. See pin descriptions for more information.

PT4841 Performance Characteristics (See Note A)

Efficiency vs Output Power

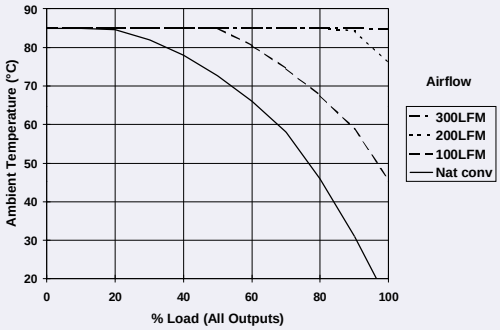


Power Dissipation vs Output Power

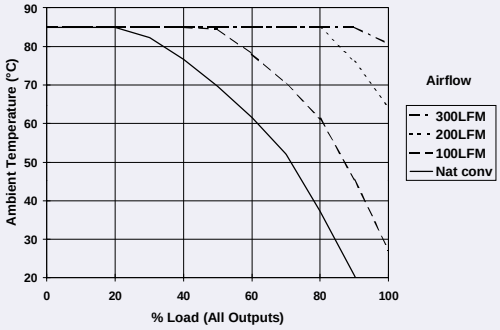


PT4841 Safe Operating Areas (See Note B)

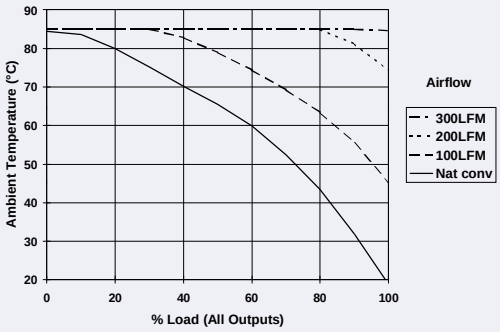
PT4841 SOA vs Output Load @V_{in} =48V



PT4841 SOA vs Output Load @V_{in} =36V



PT4841 SOA vs Output Load @V_{in} =60V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

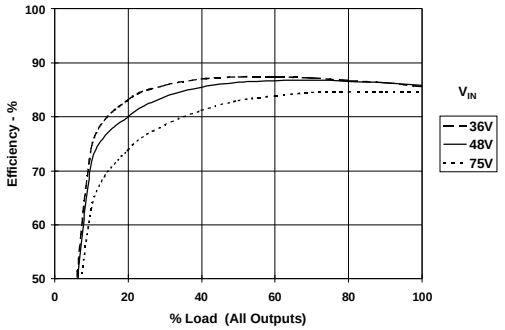
PT4842 Specifications (Unless otherwise stated, the operating conditions are:- T_a =25°C, V_{in} =48V, and Io_n =0.5Io_nmax)

Characteristics	Symbols	Conditions		PT4842 Min	Typ	Max	Units
Output Power	P_o	Each output:	Vo_1 (12V)	—	—	32.4 (1)	
			Vo_2 (3.3V)	—	—	20 (1)	W
			Vo_3 (1.8V)	—	—	12.6 (1)	
		Total (all three outputs)		—	—	62 (1)	W
Output Current	I_o		Io_1 (12V)	0	—	2.7	A
			Io_2 (3.3V)	0	—	6 (2)	A
			Io_3 (1.8V)	0	—	7 (2)	
		Maximum (Io_2 + Io_3)		—	—	11 (2)	A
Current Limit Threshold	I_{LIM}		Io_1	—	4	—	A
			Io_2 + Io_3	—	16	—	
Over Current Shutdown Delay (3)	t_{sd}	Time period prior to latched shutdown		—	200	—	ms
Input Voltage Range	V_{in}			36	—	75	V
Under Voltage Lockout	V_{on}	V_{in} increasing		—	34	—	V
	V_{off}	V_{in} decreasing		—	32	—	
Internal Input Capacitance	C_{int}			—	2	—	µF
Output Voltage	V_o		Vo_1 (12V)	11.64	12.0	12.36	
			Vo_2 (3.3V)	3.2	3.3	3.4	V
			Vo_3 (1.5V)	1.74	1.8	1.86	
Output Adjust Range	$V_o$adj		Vo_2 / Vo_3	±10	—	—	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	0.1	1.0	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	0.2	1.0	%V_o
Cross Regulation	Reg_{cross}	Any one output vs. other outputs		—	—	1.0	%V_o
V_o Ripple/Noise (4) (0 to 20MHz bandwidth)	V_n	C_{out} =10µF tantalum capacitor	Vo_1 (12V)	—	45	100	
			Vo_2 (3.3V)	—	20	50	mV_{pp}
			Vo_3 (1.5V)	—	20	50	
Transient Response (5)	t_{tr}	25% load step		—	30	—	µSec
	V_{os}	V_o over/undershoot		—	5	—	%V_o
Efficiency	η	P_o =$P_o$max		—	84	—	%
Switching Frequency	f_s	Over V_{in} and I_o ranges		450	500	550	kHz
On/Off Control	On	Referenced to –V_{in}	Logic '0'	0	—	0.8	
	Off		Logic '1'	2.4	—	75 (6)	V
			Open cct. voltage		3	5	
	I_{stby}	Input current in 'Off' state		—	9	15	mA
Primary/Secondary Isolation	V_{iso}			1500	—	—	V
	C_{iso}			—	1500	—	pF
	R_{iso}			10	—	—	MΩ
Temperature Sense (7)	V_{temp}	Output voltage at temperatures:-	–40°C	—	0.1	—	V
			100°C	—	1.5	—	
External Output Capacitance (8)	C_{out}		C_o1	0	—	330	
			C_o2	0	—	5,000	µF
			C_o3	0	—	10,000	

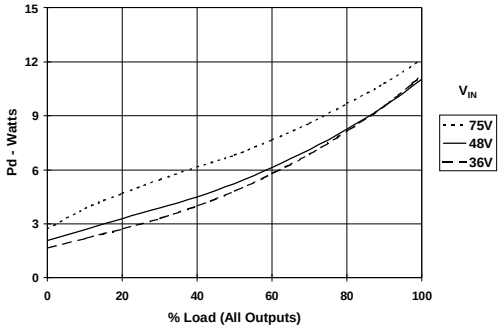
Notes: *(1) The sum total power delivered from all three regulated outputs, Vo_1, Vo_2, and Vo_3, cannot exceed 62 watts.*
(2) The sum-total current from outputs Vo_2, and Vo_3 cannot exceed 11ADC.
(3) After latched shutdown, the module may be reset by cycling the input power.
(4) The ripple and noise is measured with a 10µF tantalum capacitor across each output.
(5) The transient response is measured with a 25% load step from I_o =0.5$I_o$max, and di/dt =0.2A/µs.
(6) Pins 3 & 4 are diode protected and can be connected to +V_{in}.
(7) Voltage output at "TEMP" pin is defined by the equation:- V_{TEMP} = 0.5 + 0.01·T, where T is the sensed temperature in degrees centigrade. See pin descriptions for more information.
(8) Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. For more information, refer to the application note regarding capacitor selection.

PT4842 Performance Characteristics (See Note A)

Efficiency vs Output Power

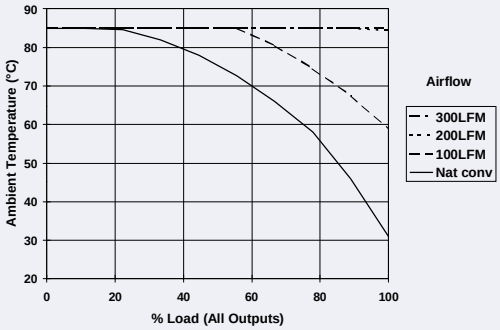


Power Dissipation vs Output Power

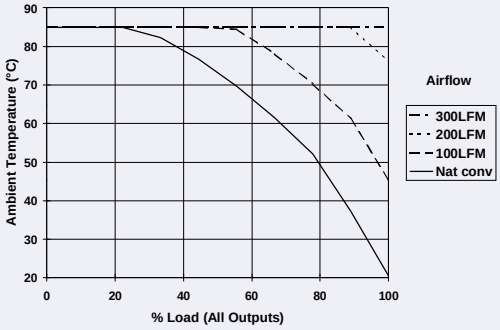


PT4842 Safe Operating Areas (See Note B)

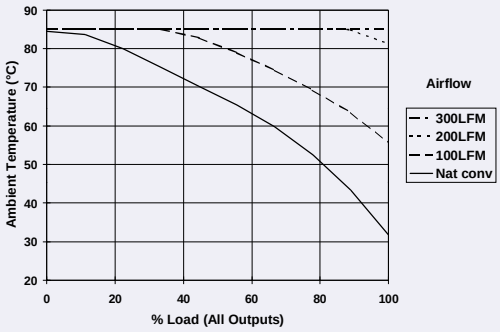
PT4842 SOA vs Output Load @V_{in} =48V



PT4842 SOA vs Output Load @V_{in} =36V



PT4842 SOA vs Output Load @V_{in} =60V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

Operating Features of the PT4840 Triple-Output DC/DC Converters

Over-Current Protection

The current limit function of the PT4840 series of triple-output DC/DC converters is divided into two zones. These are the high-voltage output Vo_1, and the two low-voltage outputs (combined) Vo_2/Vo_3.

A load fault applied to Vo_1 will cause this output voltage to drop. A drop in Vo_1 (to less than 10V) will also cause outputs Vo_2 and Vo_3 to simultaneously turn off. Load faults applied to either Vo_2 or Vo_3 will cause both these outputs to drop, but in this case Vo_1 will be unaffected.

Each protection zone incorporates a latch-off time-out period of approximately 200ms. A transient or momentary fault lasting less than this period will allow the prompt recovery of all affected outputs. Faults applied for longer than this period will cause the affected zone to latch off. Faults applied to Vo_2 or Vo_3 results in the latch off of both these outputs; Vo_1 being unaffected, whereas the latch off of Vo_1 will shut down all three outputs. Recovery from a latched shutdown condition requires the removal and corresponding re-application of input power to the converter.

Over-Temperature Protection

The PT4840 DC/DC converter series have an internal temperature sensor, which monitors the temperature of the module's metal case. If the case temperature exceeds a nominal 110°C the converter will shut down. The converter will automatically restart when the sensed temperature returns to about 100°C. The analog voltage generated by the sensor is also made available at the 'TEMP' output (pin 5), and can be monitored by the host system for diagnostic purposes. Consult the 'Pin Descriptions' section of the data sheet for more information on this feature.

Under-Voltage Lock-Out

The Under-Voltage Lock-Out (UVLO) circuit prevents operation of the converter whenever the input voltage to the module is insufficient to maintain output regulation. The UVLO has approximately 2V of hysterisis. This is to prevent oscillation with a slowly changing input voltage. Below the UVLO threshold the module is off and the enable control inputs, EN1 and EN2 are inoperative.

Primary-Secondary Isolation

The PT4840 series of DC/DC converters incorporate electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are production tested to a withstand voltage of 1500VDC. The isolation complies with UL60950 and EN60950, and the requirements for operational isolation. This allows the converter to be configured for either a positive or negative input voltage source.

The regulation control circuitry for these modules is located on the secondary (output) side of the isolation barrier. Control signals are passed between the primary and secondary sides of the converter via a proprietory magnetic coupling scheme. This eliminates the use of opto-couplers. The data sheet 'Pin Descriptions' and 'Pin-Out Information' provides guidance as to which reference (primary or secondary) that must be used for each of the external control signals.

Input Current Limiting

The converter is not internally fused. For safety and overall system protection, the maximum input current to the converter must be limited. Active or passive current limiting can be used. Passive current limiting can be a fast acting fuse. A 125-V fuse, rated no more than 10A, is recommended. Active current limiting can be implemented with a current limited "Hot-Swap" controller.

Using the On/Off Enable Controls on the PT4840 Series of Triple Output DC/DC Converters

The PT4840 (48V input) series of 65-W, triple-output DC/DC converters incorporate two output enable controls. EN1 (pin 3) is the *Negative Enable* input, and EN2 (pin 4) is the *Positive Enable* input. Both inputs are electrically referenced to -V_{in} (pin 2) on the primary or input side of the converter. A pull-up resistor is not required, but may be added if desired. Voltages of up to 70V can be safely applied to the either of the *Enable* pins.

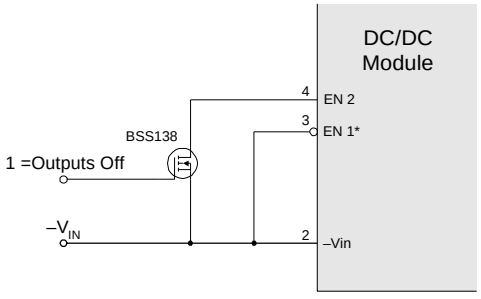
Automatic (UVLO) Power-Up

Connecting EN1 (pin 3) to -V_{in} (pin 2) and leaving EN2 (pin 4) open-circuit configures the converter for automatic power up. (See data sheet "Typical Application"). The converter control circuitry incorporates an "Under Voltage Lockout" (UVLO) function, which disables the converter until the minimum specified input voltage is present at ±V_{in}. (See data sheet Specifications). The UVLO circuitry ensures a clean transition during power-up and power-down, allowing the converter to tolerate a slow-rising input voltage. For most applications EN1 and EN2, can be configured for automatic power-up.

Positive Output Enable (Negative Inhibit)

To configure the converter for a positive enable function, connect EN1 (pin 3) to -V_{in} (pin 2), and apply the system On/Off control signal to EN2 (pin 4). In this configuration, a low-level input voltage (-V_{in} potential) applied to pin 4 disables the converter outputs. Figure 1 is an example of this configuration.

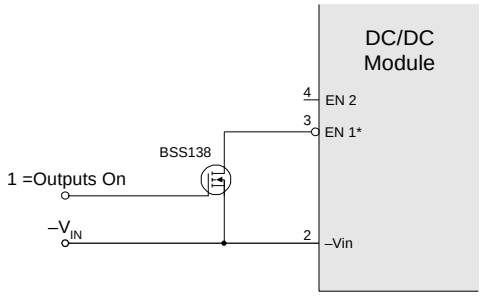
Figure 1; Positive Enable Configuration



Negative Output Enable (Positive Inhibit)

To configure the converter for a negative enable function, EN2 (pin 4) is left open circuit, and the system On/Off control signal is applied to EN1 (pin 3). A low-level input voltage (-V_{in} potential) must then be applied to pin 3 in order to enable the outputs of the converter. An example of this configuration is detailed in Figure 2. *Note: The converter will only produce and output voltage if a valid input voltage is applied to ±V_{in}.*

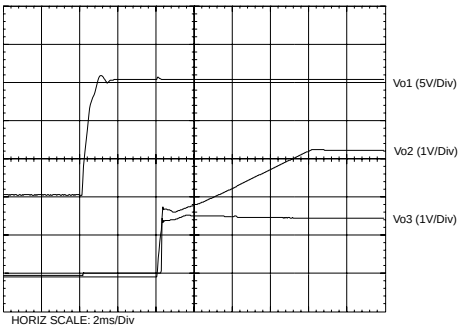
Figure 2; Negative Enable Configuration



On/Off Output Voltage Sequencing

The Vo_2 and Vo_3 low-voltage outputs from the PT4840 series of DC/DC converters are internally sequenced to meet the power-up requirements of popular microprocessor and DSP chipsets. Figure 3 shows the waveforms from a PT4841 after power is applied to the input of the converter. During power-up, the Vo_1 reaches its output regulation voltage first, followed the Vo_2 and Vo_3 voltages. The Vo_2 and Vo_3 voltage waveforms typically track within 0.4V prior to Vo_2 reaching regulation. The waveforms were measured with resistive loads of 2A, 3A, and 3A, at Vo1, Vo2, and Vo3 respectively. The input source voltage was 48-VDC. The converter typically produces a fully regulated output within 25ms.

Figure 3; Vo_1, Vo_2, Vo_3 Power-Up Sequence



During turn-off, all outputs drop rapidly due to the discharging effect of actively switched rectifiers. The voltage at Vo_2 remains higher than Vo_3 during this period. The discharge time is typically 100µs, but will vary with the amount of external load capacitance.

PT4840 Input/ Output Filter Capacitance Selection for Excalibur™ Triple-Ouput DC/DC Converters

General Requirements

The capacitors on the input bus are optional but may be required to insure dynamic response to load transients. The suggested capacitors on the input bus include ceramic noise attenuation components. The PT4840 series has an internal 1µH input inductor. This inductor provides an effective input differential noise filter when 1µF ceramic capacitors are connected across the input terminals. This low impedance filter has an attenuation factor of typically 15dB.

The output capacitors are all optional and may be used to optimize dynamic and transient load performance. The maximum capacitance allowed for each bus is given in the electrical specification table on p.3.

Input Capacitors

The input capacitors are all optional. The 33µF/100V electrolytic capacitor should have a minimum ripple current 400mA. Ripple current and <350mΩ equivalent series resistance (ESR) are the major considerations along with temperature when selecting electrolytic capacitors. The ceramic capacitors, each 1µF (3×0.33µF), X7R type, have a wide temperature range and are suggested for noise reduction. The module's internal inductor and the external ceramic capacitors form an excellent differential noise filter. Additional filter components, L_1 and L_2, will reject common-mode input noise (*See Figure 1*). A common-mode choke can also be used to reduce common-mode noise levels. These optional filter components may be required to meet FCC Class A limits for conducted emissions.

Optional Output Capacitors; Vo_1 (Table 1)

The ESR of the 330µF output capacitor for Vo_1 (+15V) must be ≥40mΩ. Electrolytic capacitors have minimal effect on ripple at frequencies greater than 200kHz but excellent low-frequency transient response. At the ripple frequency, ceramic decoupling capacitors improve the response to fast transients and reduce any high-frequency noise components during higher current excursions.

The preferred capacitor part numbers are identified in the Table 1. The table identifies vendors with acceptable ESR and ripple current (rms) ratings. The suggested minimum quantities for Vo_1 are identified. Tantalum capacitors, rated 30V or greater with an equivalent ESR of ≥40mΩ, are also recommended for Vo_1.

Optional Output Capacitors; Vo_2 & Vo_3 (Table 2)

The combined ESR of the output capacitors selected for Vo_2 and Vo_3 (lower bus voltages) must be ≥10mΩ. Low ESR electrolytic capacitors have minimal effect on ripple at frequencies greater than 200kHz but excellent low-frequency transient response. Above the ripple frequency, ceramic decoupling capacitors improve the response to fast transients and reduce any high-frequency noise components during higher current excursions. The preferred lower ESR type capacitor part numbers for Vo_2 and Vo_3 are identified in Table 2. The table identifies vendors with acceptable ESR and ripple current (rms) ratings. The tantalum and Oscon® type capacitors have both low ESR and stable characteristics. These are recommended for Vo_2 and Vo_3 in applications where the temperature range extends below 0°C.

Capacitors from other vendors may also be suitable. The specifications in both tables provide guidance for the selection of alternative parts. The ripple current (rms) rating and ESR (Equivalent Series Resistance at 100kHz) are the critical parameters necessary to insure both optimum regulator and long term capacitor life cycles.

Figure 1; Optional Capacitor and FIlter Components

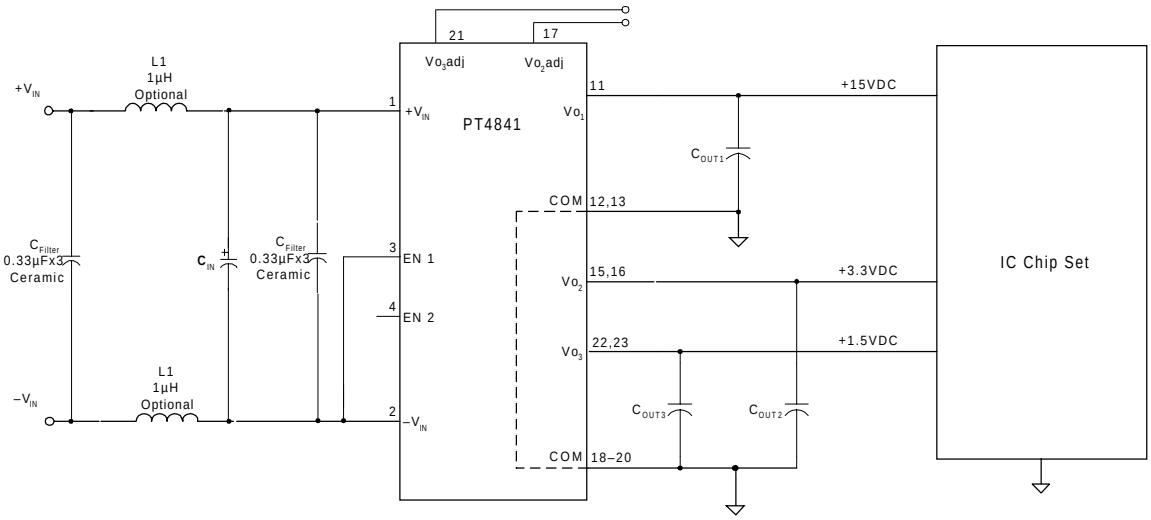


Table 1; Output Capacitors for Vo_1 *(See Note A)*

Capacitor Vendor/ Component Series	Capacitor Characteristics, High Voltage Bus Selection (≥12V)					Quantity	
	Working Voltage	Value (µF)	(ESR) Equivalent Series Resistance	Max Ripple Current @85°C (Irms)	Physical Size (mm)	Vo_1 (≥12V)	Vendor Number
Panasonic							
FC (Surface Mount)	25V	220	0.15Ω	670mA	10×10.2	1	EEVFC1E221P
	35V	330	0.065Ω	1205mA	12.5×16.5	1	EEVFC1V331LQ
FK (Surface Mount)	25V	330	0.160Ω	600mA	8×10.2	1	EEVFK1E331P
United Chemi-Con							
LXZ	25V	330	0.090Ω	755mA	10×12.5	1	LXZ25VB331M10X12L
	35V	220	0.090Ω	760mA	10×12.5	1	LXZ35VB221M10X12L
MVY	25V	330	0.15Ω	670mA	10×10.3	1	MVY25VC331M10x10TP
Nichicon PM	25V	220	0.13Ω	600mA	10×12.5	1	UPM1E221MPH6
	25V	330	0.095Ω	750mA	10×15	1	UPM1E331MPH6
Oscon- SS/SV						N/R	Do Not Use On the +15V Bus
AVX:							
Tantalum TPS	35V	33	0.4Ω÷3 =0.133Ω	707mA×3	7.3L	3	TPSV336M035R0400
Ceramic X7R	50V	1	0.006Ω	500mA	×5.7W	1	MR065C105KAA(leads)C
Ceramic X7R	50V	1	0.006Ω	500mA	×4.1	1	1825C105MAT2(SM)
Kemet:							
Tantalum 495	35V	22	0.275Ω	697mA×3	7.3L×5.7W	3	T495X226M035AS
X7R Ceramic	50V	1	0.006Ω	>775mA	×4.0H	1	C1825C1055RAC
Sprague:							
Tantalum 594D	35V	33	0.200Ω	896mA	7.2L×6W	1	594D336X0035R2T
X7R Ceramic	50V	1	0.006Ω	>775	4.1W	1	VJ1825Y105MXAÑ

Table 2; Output Capacitors for Vo_2, and Vo_3 *(See Note B)*

Capacitor Vendor/ Component Series	Capacitor Characteristics, Low Voltage Bus Selection (<5V)					Quantity	
	Working Voltage	Value(µF)	(ESR) Equivalent Series Resistance	Max Ripple Current @85°C (Irms)	Physical Size (mm)	Vo_2/Vo_3 (<5V)	Vendor Number
Panasonic:							
FC (Surface Mount)	35V	680	0.043Ω	1655mA	16×15	1	EEUFC1V681S
	35V	390	0.065Ω	1205mA	12.5×15	1	EEVFC1V391S
FC (Radial)	16V	330	0.090Ω	755mA	10.×12.5	1	EEUFC1E331
United Chemi-Con:							
LFZ	35V	330	0.068Ω	1050mA	10×16	1	LXZ35VB331M10X16LL
	25V	330	0.090Ω	760mA	10×12.5	1	LXZ25VB331M10X12LL
FS	10V	330	0.025Ω	3500mA	10×10.5	1	10FS3390M
FX	20V	220	0.020Ω	4405mA	10×10.5	1	20FX220M
Nichicon PM	35V	560	0.048Ω	1360mA	16×15	1	UPM1V561MHH6
	35V	330	0.065Ω	1020mA	12.5×15	1	UPM1V331MHH6
	25V	330	0.095Ω	750mA	10.5×15	1	UPM1C331MHH6
Panasonic FK	35V	330	0.080Ω	850mA	10×10.2	1	EEVFK1V331P
(Surface Mount)	35V	470	0.060Ω	1100mA	12.5×13.5	1	EEVFK1V471Q
Oscon -SS (Radial)	10V	330	0.025Ω	2660mA	10×10.5	1	10SS330M
SV (Surface Mount)	10V	330	0.020Ω	2660mA	10.3×10.3×	1	10SV330M
	20V	150	0.024Ω	2520mA	×12.6	1	20SV150M
AVX TPS Tantalum	10V	330	0.100Ω	1414mA	7.3L	1	TPSV337X010R0100
	10V	330	0.060Ω	1826mA	×5.7W	1	TPSV337X010R0060
	16V	150	0.075Ω	1633mA	×4.1	1	TPSV157X016R0075
Kemet:							
T520	10V	330	0.040Ω	2000mA	4.3W×7.3L	1	T520X337M010AS
T495	10V	220	0.070Ω	1382mA	×4.0H	1	T495X227M010AS
Sprague Tantalum	10V	330	0.045Ω	1888mA	7.2L×6W	1	594D337X0010R2T
594D (Surface Mount)	16V	180	0.055Ω÷2	1704mA	×4.1W	2	594D187X0016R2T

Note A: *N/R –Not Recommended. Ultra-low ESR capacitors are not recommended for Vo_1 (+15V) output bus.*
Note B: *The part numbers listed in Table 2 can be used for any low-output bus voltage of <5VDC.*

Adjusting the Output Voltage of the PT4840 Dual Output Voltage DC/DC Converters

The Vo_2 and Vo_3 output voltages from the PT4840 series of DC/DC converters can be independantly adjusted by up to ±10% from their factory pre-set voltage. The method of adjustment uses a single external resistor. [1] The value of the resistor determines the magnitude of adustment, and the placement of the resistor determines the direction of adjustment (up or down). The resistor value can be calculated directly from a simple formula. The constants are given in Table 1. Alternatively, Table 2 provides the resistor values for a select number of output voltages. The placement of each resistor is as follows.

Vo_2 Adjust Up: To increase the output, add a resistor R_1 between pin 17 (Vo_2 Adjust) and pin 18 (COM).

Vo_2 Adjust Down: Add a resistor (R_2), between pin 17 (Vo_2 Adjust) and pin 16 ($+Vo_1$).

Vo_3 Adjust Up: Add a resistor R_3 between pin 21 (Vo_3 Adjust) and pins 20 (COM).

Vo_3 Adjust Down: Add a resistor (R_4) between pin 21 (Vo_3 Adjust) and pin 22 ($+Vo_3$).

Refer to Figure 1 for further information on resistor placement.

Notes:

1. Use only a single 1% resistor in either the R_1 or (R_2) location to adjust Vo_2, and in the R_3 or (R_4) location to adjust Vo_3. Place the resistor as close to the ISR as possible.
2. Never connect capacitors to either the Vo_2 Adjust or Vo_3 Adjust pins. Any capacitance added to these control pins will affect the stability of the respective regulated output.

The adjust resistor values may be calculated. Use the applicable formula and select the appropriate constants from Table 1 for the output and model being adjusted.

$$R_1 \text{ or } R_3 = \frac{R_o \cdot V_r}{V_a - V_o} - R_s \quad k\Omega$$

$$(R_2) \text{ or } (R_4) = \frac{R_o\,(V_a - V_r)}{V_o - V_a} - R_s \quad k\Omega$$

Where: V_o = Original output voltage, (Vo_2 or Vo_3)
V_a = Adjusted output voltage
V_r = The reference voltage from Table 1
R_o = The resistance value in Table 1
R_s = The series resistance from Table 1

Figure 1

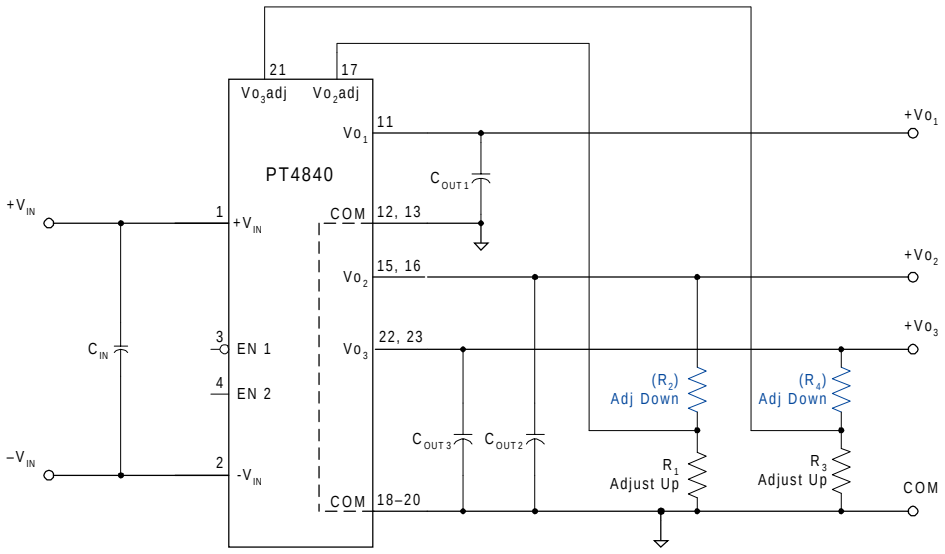


Table 1

ADJUSTMENT RANGE AND FORMULA PARAMETERS

	V_{O2} Bus	V_{O3} Bus	
Series Pt #	**PT4841/42**	**PT4841**	**PT4842**
Adj. Resistor	**R_1/(R_2)**	**R_3/(R_4)**	**R_3/(R_4)**
V_o(nom)	3.3V	1.5V	1.8V
V_a(min)	2.97V	1.35V	1.62V
V_a(max)	3.63V	1.65V	1.98V
V_r	2.5V	1.0V	TBD
R_o (kΩ)	6.34	4.99	TBD
R_s (kΩ)	7.5	10.0	TBD

Table 2

ADJUSTMENT RESISTOR VALUES

	V_{O2} Bus	V_{O3} Bus	
Series Pt #	**PT4841/42**	**PT4841**	**PT4842**
Adj. Resistor	**R_1/(R_2)**	**R_3/(R_4)**	**R_3/(R_4)**
V_o(nom)	3.3V	1.5V	1.8V
V_a(req'd)		**V_a(req'd)**	
3.0	(3.1)	1.35	(1.6)kΩ
3.05	(6.5)kΩ	1.4	(10.0)kΩ
3.1	(11.5)kΩ	1.45	(34.9)kΩ
3.15	(20.0)kΩ	1.5	
3.2	(36.9)kΩ	1.55	89.8kΩ
3.25	(87.6)kΩ	1.6	39.9kΩ
3.3		1.65	23.3kΩ
3.35	309.0kΩ	1.7	
3.4	151.0kΩ	1.7	
3.45	98.2kΩ	1.8	
3.5	71.7kΩ	1.85	
3.55	55.9kΩ	1.9	
3.6	45.3kΩ	1.95	
		2.0	

R_1/R_3 = Black, R_2/R_4 = (Blue)

VDE Approved Installation Instructions (Installationsanleitung)

Nennspannnug (Rated Voltage):	PT4840 36 to 72 Vdc, Transient to 80Vdc
Nennaufnahme (Rated Input):	PT4840 2.2 Adc
Nennleistung (Rated Power):	25 Watts Maximum PT4841, 65 Watts Maximum PT4842, 62 Watts Maximum
Ausgangsspannung (Sec. Voltage):	PT4840 Series PT4841, +15/ +3.3/ +1.5 Vdc, 1.25 Adc/ 3.0 Adc/ 2.0 Adc Maximum total current is 13.7 Adc or 65 Watts PT4842, +12V/ +3.3V/ +1.8V, 2.7Adc/ 6Adc/ 7Adc
Ausgangsstrom (Sec. Current): oder (or) Ausgangsleistung (Sec. Power):	Maximum total current is 13.7 Adc or 62 Watts

Angabe der Umgebungstemperatur

(Information on ambient temperature): +85 °C maximum

Besondere Hinweise (Special Instructions):

Es ist vorzusehen, daß die Spannungsversorgung in einer Endanwendung über eine isolierte Sekundaerschaltung bereit gestellt wird. Die Eingangspannung der Spannungsversorgungsmodule muss eine verstaerkte Isolierung von der Wechselstromquelle aufweisen.

Die Spannungsversorgung muss gemaess den Gehaeuse-, Montage-, Kriech- und Luftstrecken-, Markierungs- und Trennanforderungen der Endanwendung installiert werden. Bei Einsatz eines TNV-3-Einganges muss die SELV-Schaltung ordnungsgemaess geerdet werden.

(The power supply is intended to be supplied by isolated secondary circuitry in an end use application. The input power to these power supplies shall have reinforced insulation from the AC mains.

The power supply shall be installed in compliance with the enclosure, mounting, creepage, clearance, casualty, markings, and segregation requirements of the end-use application. When the input is TNV-3, the SELV circuitry must be reliably grounded.)

Offenbach,

VDE Prüf- und Zertifizierungsinstitut
Abteilung / *Department TD*

(Jürgen Bärwinkel)

Ort / *Place*: Datum / *Date*:

12/12/01

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