

Product Summary

BV_{DSS}	$R_{DS(ON)} \text{ Max}$	I_D $T_c = +25^\circ\text{C}$ (Note 9)
60V	2mΩ @ $V_{GS} = 10\text{V}$	100A
	3mΩ @ $V_{GS} = 6\text{V}$	100A
	3.3mΩ @ $V_{GS} = 4.5\text{V}$	100A

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

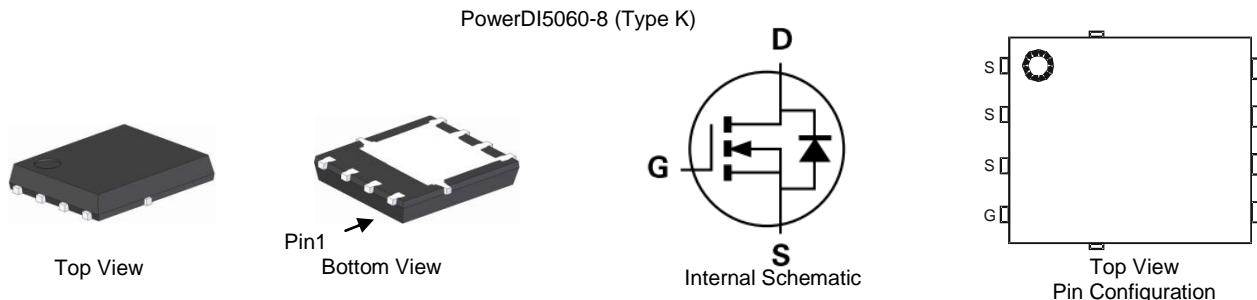
- Switching
- Synchronous Rectification
- DC-DC Converters

Features

- Rated to $+175^\circ\text{C}$ – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching – Ensures More Reliable and Robust End Application
- Thermally Efficient Package – Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On-State Losses
- $<1.1\text{mm}$ Package Profile – Ideal for Thin Applications
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: PowerDI®5060-8 (Type K)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.097 grams (Approximate)



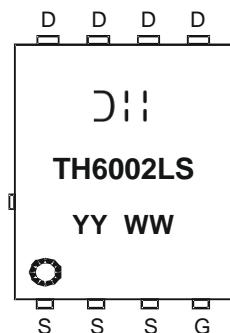
Ordering Information (Note 4)

Part Number	Case	Packaging
DMTH6002LPS-13	PowerDI5060-8 (Type K)	2,500 / Tape & Reel

Notes:

1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



DI = Manufacturer's Marking
 TH6002LS = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last Two Digits of Year (ex: 17 = 2017)
 WW = Week Code (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current, $V_{GS} = 10\text{V}$ (Note 6)	I_D	100	A
		100	
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)	I_{DM}	200	A
Continuous Body Diode Forward Current (Note 6)	I_S	100	A
Pulsed Body Diode Forward Current (10 μs Pulse, Duty Cycle = 1%)	I_{SM}	200	A
Avalanche Current, $L = 3\text{mH}$	I_{AS}	14	A
Avalanche Energy, $L = 3\text{mH}$	E_{AS}	294	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	2.3	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	55	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	P_D	167	W
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	0.9	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	—	3	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	1.7	2	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 30\text{A}$
		—	2	3		$V_{GS} = 6\text{V}, I_D = 30\text{A}$
		—	2.3	3.3		$V_{GS} = 4.5\text{V}, I_D = 30\text{A}$
Diode Forward Voltage	V_{SD}	—	—	1.2	V	$V_{GS} = 0\text{V}, I_S = 50\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	6555	—	pF	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	2264	—		
Reverse Transfer Capacitance	C_{rss}	—	187	—		
Gate Resistance	R_g	—	0.7	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	130.8	—	nC	$V_{DS} = 30\text{V}, I_D = 50\text{A}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	63.6	—		
Gate-Source Charge	Q_{gs}	—	20.8	—		
Gate-Drain Charge	Q_{gd}	—	29.4	—	ns	$V_{DD} = 20\text{V}, V_{GS} = 10\text{V}, I_D = 50\text{A}, R_g = 2.5\Omega$
Turn-On Delay Time	$t_{D(ON)}$	—	11.2	—		
Turn-On Rise Time	t_R	—	10.8	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	44	—		
Turn-Off Fall Time	t_F	—	19.5	—	nC	$I_F = 50\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Time	t_{RR}	—	61.8	—		
Reverse Recovery Charge	Q_{RR}	—	123	—		

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

6. Thermal resistance from junction to soldering point (on the exposed drain pad).

7. Short duration pulse test used to minimize self-heating effect.

8. Guaranteed by design. Not subject to product testing.

9. Package limited.

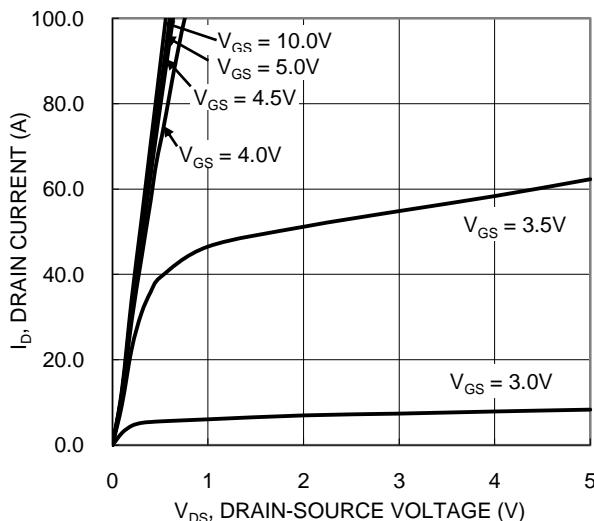


Figure 1. Typical Output Characteristic

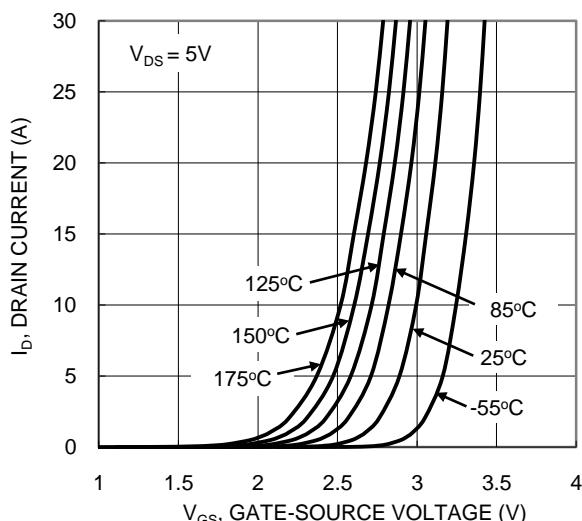


Figure 2. Typical Transfer Characteristic

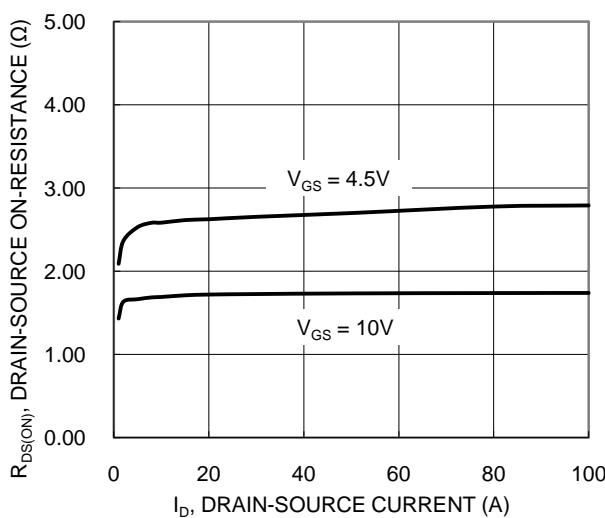


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

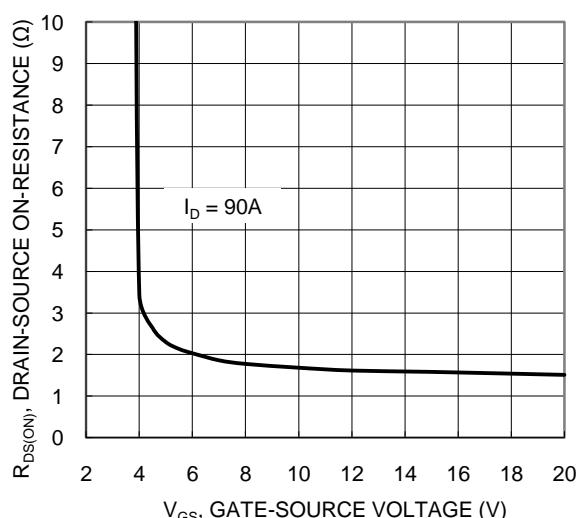


Figure 4. Typical Transfer Characteristic

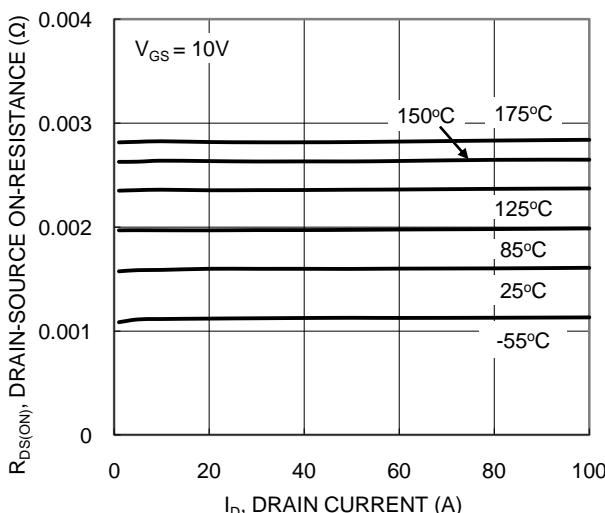


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

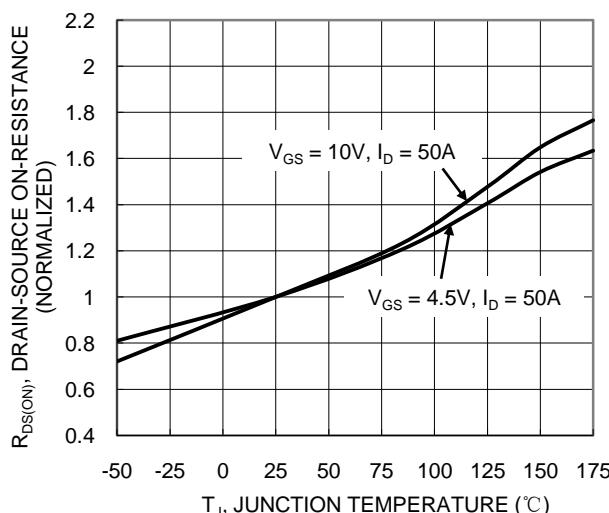


Figure 6. On-Resistance Variation with Temperature

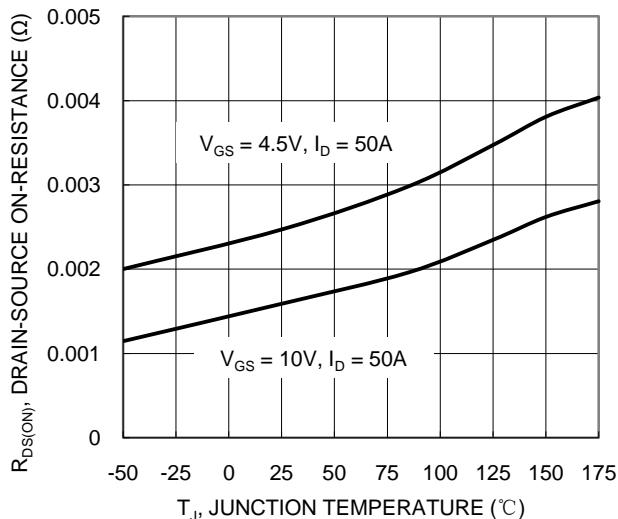


Figure 7. On-Resistance Variation with Temperature

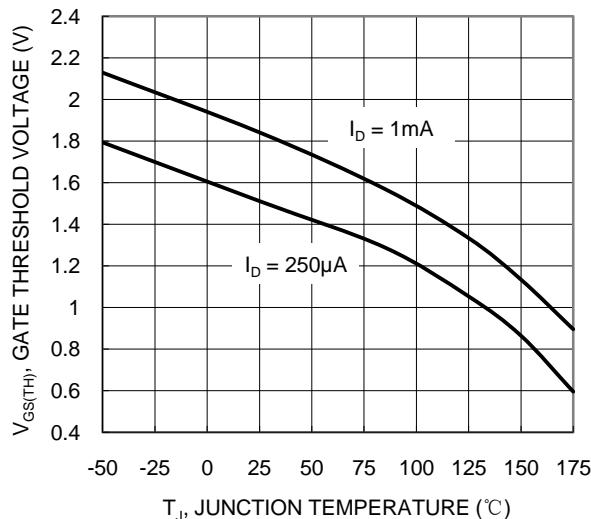


Figure 8. Gate Threshold Variation vs. Junction Temperature

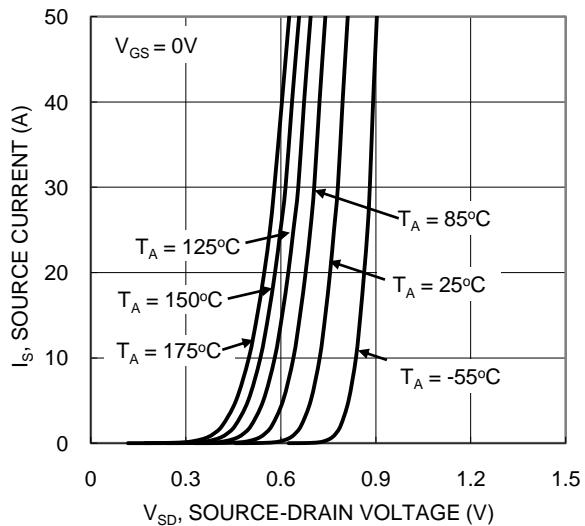


Figure 9. Diode Forward Voltage vs. Current

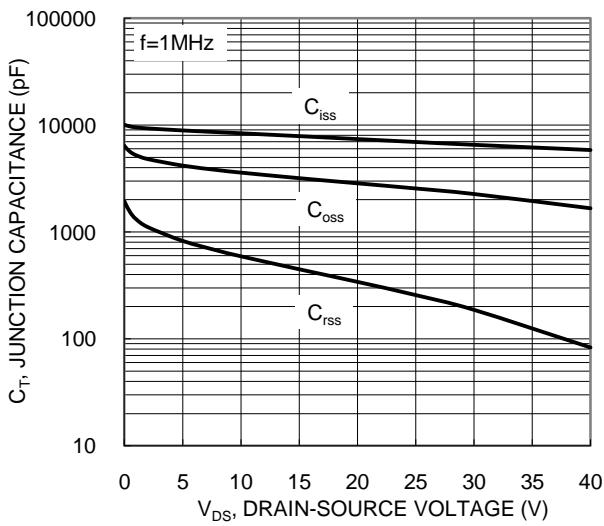


Figure 10. Typical Junction Capacitance

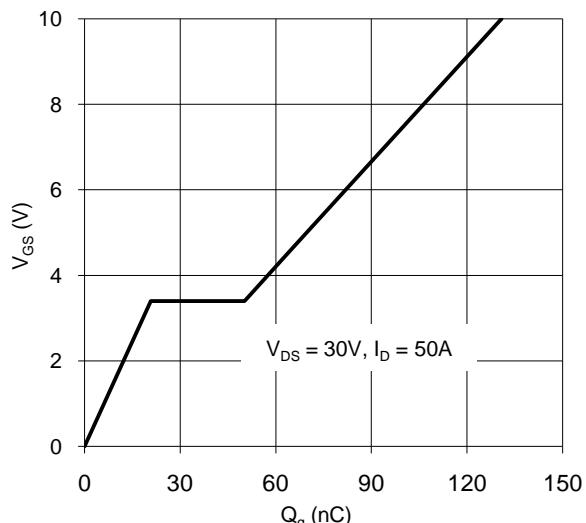


Figure 11. Gate Charge

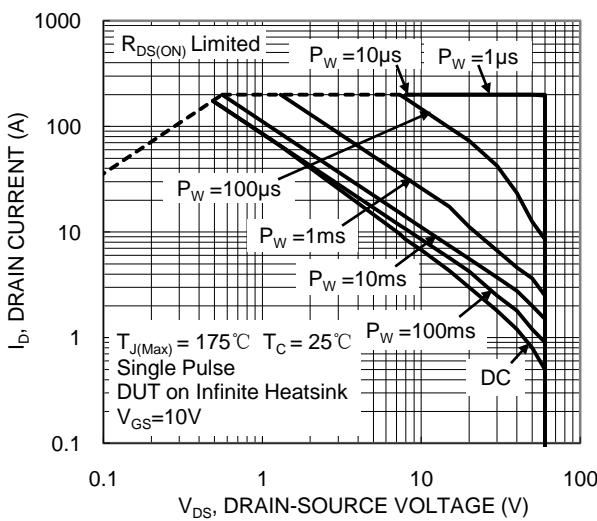


Figure 12. SOA, Safe Operation Area

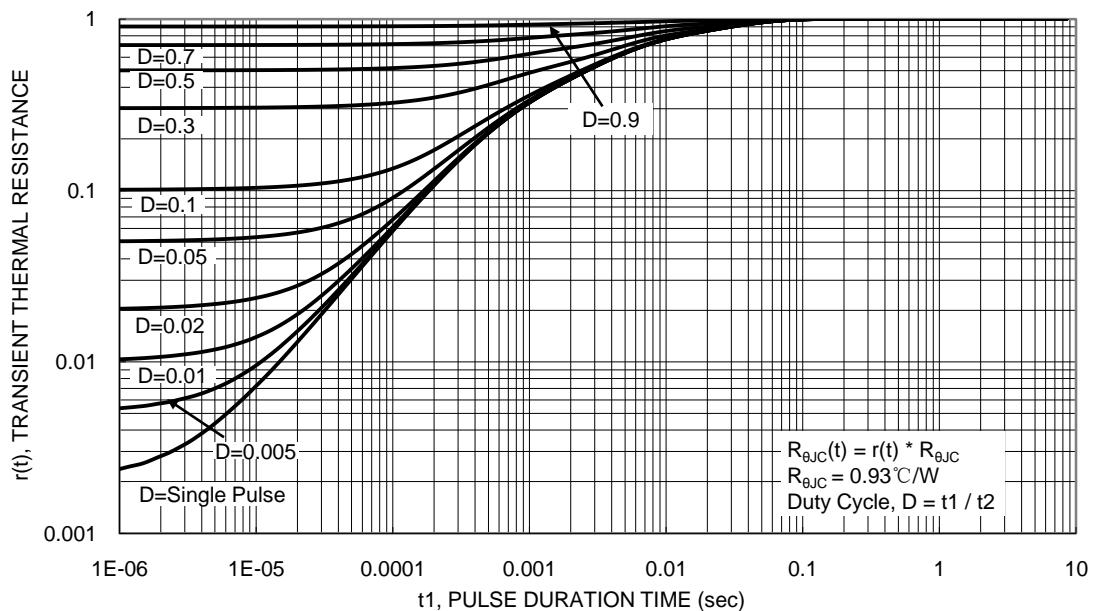
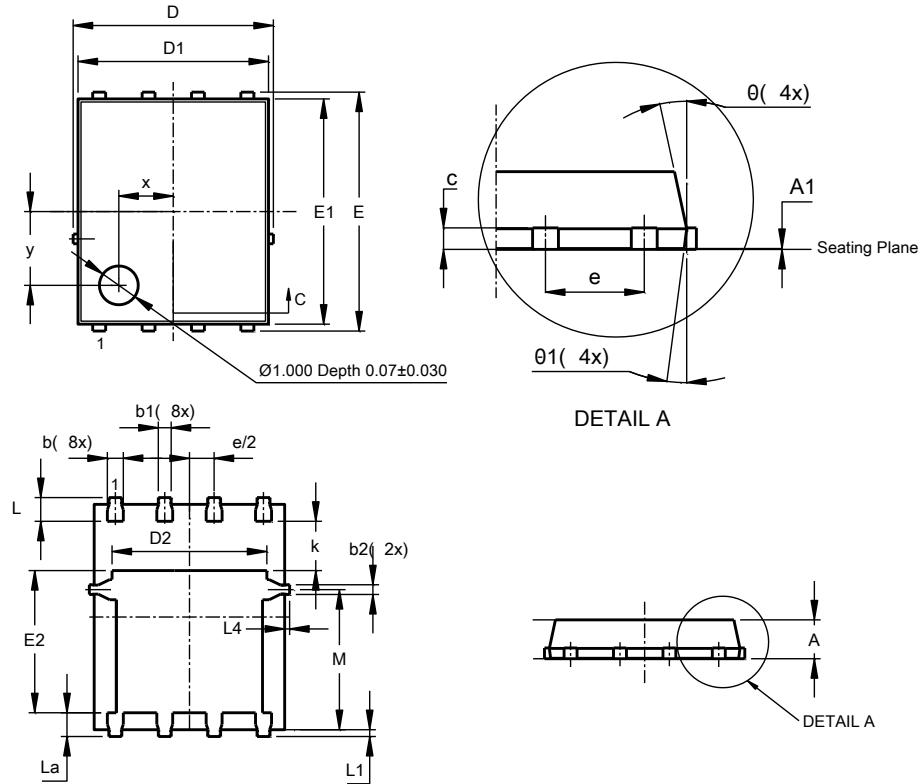


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8 (Type K)



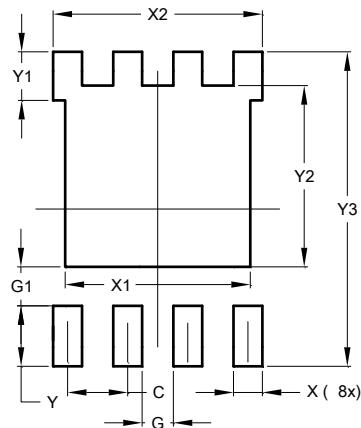
PowerDI5060-8 (Type K)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	0.02
b	0.33	0.51	0.41
b1	0.300	0.366	0.333
b2	0.20	0.35	0.25
c	0.23	0.33	0.277
D	5.15 BSC		
D1	4.85	4.95	4.90
D2	-	-	3.98
E	6.15 BSC		
E1	5.75	5.85	5.80
E2	3.56	3.725	3.66
e	1.27BSC		
k	-	-	1.27
L	0.51	0.71	0.61
La	0.51	0.675	0.61
L1	0.05	0.20	0.175
L4	-	-	0.125
M	3.50	3.71	3.605
x	-	-	1.400
y	-	-	1.900
θ	10°	12°	11°
θ1	6°	8°	7°

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8 (Type K)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	3.910
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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