

## Features

- Pin- and function-compatible with CY7C1020B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 80 \text{ mA @ } 10 \text{ ns}$
- Low complementary metal oxide semiconductor (CMOS) standby power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin thin small outline package (TSOP) II packages

## Functional Description

The CY7C1020D <sup>[1]</sup> is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected. The input and output pins ( $IO_0$  through  $IO_{15}$ ) are placed in a high-impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH)
- When the write operation is active ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW)

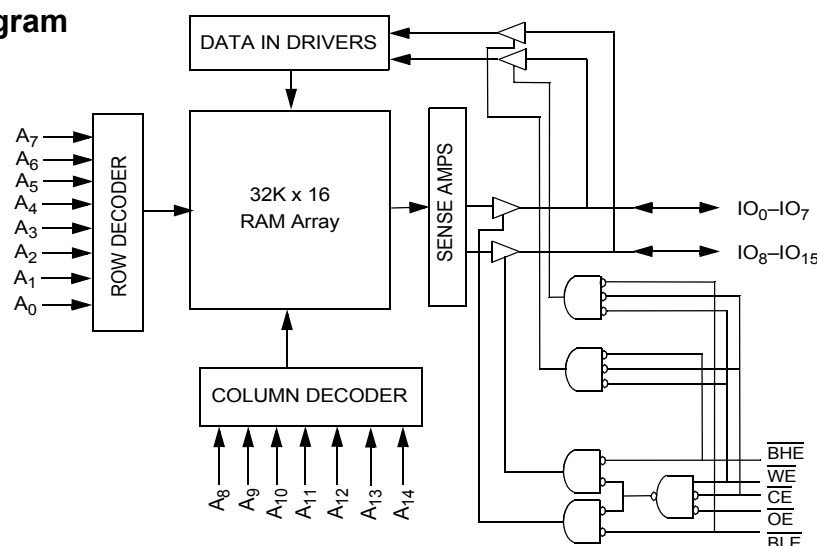
Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from IO pins ( $IO_0$  through  $IO_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{14}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from IO pins ( $IO_8$  through  $IO_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{14}$ ).

Reading from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on  $IO_0$  to  $IO_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $IO_8$  to  $IO_{15}$ . See the “Truth Table” on page 11 for a complete description of read and write modes.

The CY7C1020D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

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## Pin Configurations

Figure 1. 44-pin SOJ/TSOP II pinout (Top View) <sup>[2]</sup>

|                 |    |    |                  |
|-----------------|----|----|------------------|
| NC              | 1  | 44 | A <sub>5</sub>   |
| A <sub>3</sub>  | 2  | 43 | A <sub>6</sub>   |
| A <sub>2</sub>  | 3  | 42 | A <sub>7</sub>   |
| A <sub>1</sub>  | 4  | 41 | OE               |
| A <sub>0</sub>  | 5  | 40 | BHE              |
| CE              | 6  | 39 | BLE              |
| IO <sub>0</sub> | 7  | 38 | IO <sub>15</sub> |
| IO <sub>1</sub> | 8  | 37 | IO <sub>14</sub> |
| IO <sub>2</sub> | 9  | 36 | IO <sub>13</sub> |
| IO <sub>3</sub> | 10 | 35 | IO <sub>12</sub> |
| V <sub>CC</sub> | 11 | 34 | V <sub>SS</sub>  |
| V <sub>SS</sub> | 12 | 33 | V <sub>CC</sub>  |
| IO <sub>4</sub> | 13 | 32 | IO <sub>11</sub> |
| IO <sub>5</sub> | 14 | 31 | IO <sub>10</sub> |
| IO <sub>6</sub> | 15 | 30 | IO <sub>9</sub>  |
| IO <sub>7</sub> | 16 | 29 | IO <sub>8</sub>  |
| WE              | 17 | 28 | NC               |
| A <sub>4</sub>  | 18 | 27 | A <sub>8</sub>   |
| A <sub>14</sub> | 19 | 26 | A <sub>9</sub>   |
| A <sub>13</sub> | 20 | 25 | A <sub>10</sub>  |
| A <sub>12</sub> | 21 | 24 | A <sub>11</sub>  |
| NC              | 22 | 23 | NC               |

## Selection Guide

| Description                  | -10 (Industrial) | Unit |
|------------------------------|------------------|------|
| Maximum access time          | 10               | ns   |
| Maximum operating current    | 80               | mA   |
| Maximum CMOS standby current | 3                | mA   |

### Note

- NC pins are not connected on the die.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  to Relative GND <sup>[3]</sup> ..... -0.5 V to +6.0 V

DC voltage applied to outputs in High Z State <sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature | $V_{CC}$    | Speed |
|------------|---------------------|-------------|-------|
| Industrial | -40 °C to +85 °C    | 5 V ± 0.5 V | 10 ns |

## Electrical Characteristics

Over the Operating Range

| Parameter        | Description                                   | Test Conditions  |         | -10 (Industrial) |                       | Unit |
|------------------|---|--|---------|------------------|-----------------------|------|
|                  |   |  |         | Min              | Max                   |      |
| V <sub>OH</sub>  | Output HIGH voltage                           | I <sub>OH</sub> = −4.0 mA  |         | 2.4              | –                     | V    |
|                  |   | I <sub>OH</sub> = −0.1 mA  |         | –                | 3.4 <sup>[4]</sup>    |      |
| V <sub>OL</sub>  | Output LOW voltage                            | I <sub>OL</sub> = 8.0 mA   |         | –                | 0.4                   | V    |
| V <sub>IH</sub>  | Input HIGH voltage                            | –  |         | 2.2              | V <sub>CC</sub> + 0.5 | V    |
| V <sub>IL</sub>  | Input LOW voltage <sup>[3]</sup>              | –  |         | −0.5             | 0.8                   | V    |
| I <sub>IX</sub>  | Input load current                            | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   |         | −1               | +1                    | μA   |
| I <sub>OZ</sub>  | Output leakage current                        | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , output disabled   |         | −1               | +1                    | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> operating supply current      | V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA,<br>f = f <sub>max</sub> = 1/t <sub>RC</sub>  | 100 MHz | –                | 80                    | mA   |
|                  |   |  | 83 MHz  | –                | 72                    | mA   |
|                  |   |  | 66 MHz  | –                | 58                    | mA   |
|                  |   |  | 40 MHz  | –                | 37                    | mA   |
| I <sub>SB1</sub> | Automatic CE power-down current – TTL inputs  | Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ ,<br>V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>max</sub> |         | –                | 10                    | mA   |
| I <sub>SB2</sub> | Automatic CE Power-Down current – CMOS inputs | Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3$ V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0           |         | –                | 3                     | mA   |

### Note

3.  $V_{IL}$  (min) = -2.0 V and  $V_{IH}$  (max) =  $V_{CC} + 1$  V for pulse durations of less than 5 ns.

4. Please note that the maximum  $V_{OH}$  limit does not exceed minimum CMOS  $V_{IH}$  of 3.5V. If you are interfacing this SRAM with 5V legacy processors that require a minimum  $V_{IH}$  of 3.5V, please refer to Application Note [AN6081](#) for technical details and options you may consider.

## Capacitance

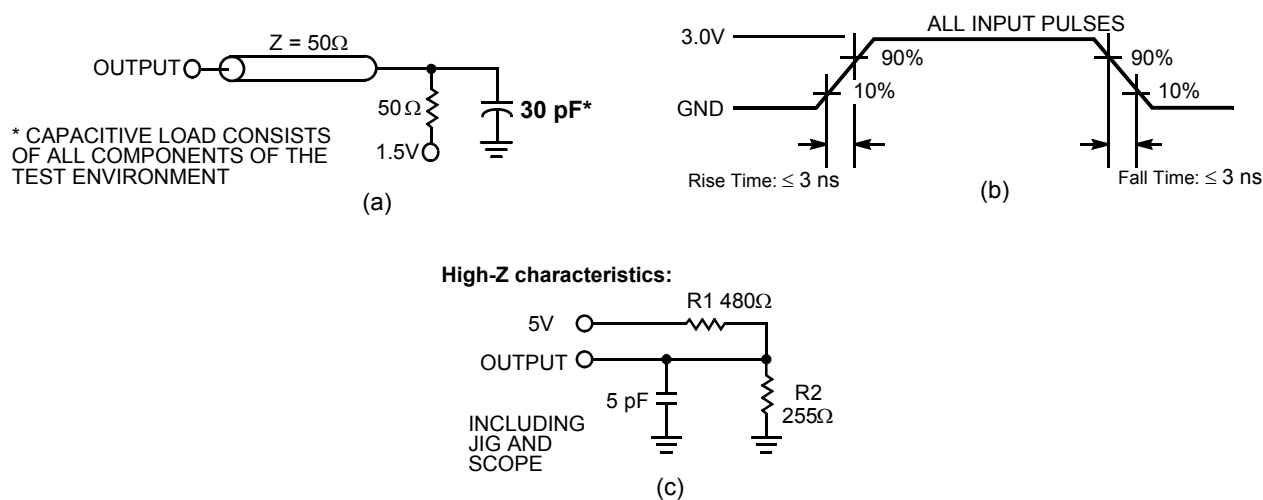
| Parameter <sup>[5]</sup> | Description        | Test Conditions   | Max | Unit |
|--------------------------|--------------------|---|-----|------|
| $C_{IN}$                 | Input capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$ | 8   | pF   |
| $C_{OUT}$                | Output capacitance |   | 8   | pF   |

## Thermal Resistance

| Parameter <sup>[5]</sup> | Description                              | Test Conditions  | SOJ   | TSOP II | Unit               |
|--------------------------|--|--|-------|---------|--------------------|
| $\Theta_{JA}$            | Thermal resistance (junction to ambient) | Still Air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board | 59.52 | 53.91   | $^\circ\text{C/W}$ |
| $\Theta_{JC}$            | Thermal resistance (junction to case)    |  | 36.75 | 21.24   | $^\circ\text{C/W}$ |

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[6]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

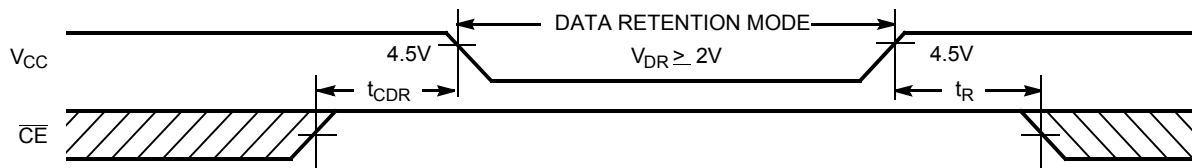
## Data Retention Characteristics

Over the Operating Range

| Parameter       | Description                          | Conditions   | Min      | Max | Unit |
|-----------------|--------------------------------------|--|----------|-----|------|
| $V_{DR}$        | $V_{CC}$ for data retention          | –  | 2.0      | –   | V    |
| $I_{CCDR}$      | Data retention current               | $V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$ | –        | 3   | mA   |
| $t_{CDR}^{[7]}$ | Chip deselect to data retention time | –  | 0        | –   | ns   |
| $t_R^{[8]}$     | Operation recovery time              | –  | $t_{RC}$ | –   | ns   |

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\text{ }\mu\text{s}$ .

## Switching Characteristics

Over the Operating Range

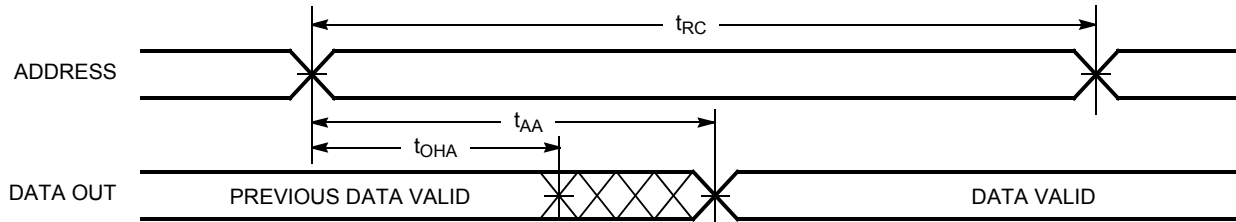
| Parameter <sup>[9]</sup>           | Description   | -10 (Industrial) |     | Unit |
|------------------------------------|---|------------------|-----|------|
|                                    |   | Min              | Max |      |
| Read Cycle                         |   |                  |     |      |
| t <sub>power</sub> <sup>[10]</sup> | V <sub>CC</sub> (typical) to the first access             | 100              | –   | μs   |
| t <sub>RC</sub>                    | Read cycle time   | 10               | –   | ns   |
| t <sub>AA</sub>                    | Address to data valid                                     | –                | 10  | ns   |
| t <sub>OHA</sub>                   | Data hold from address change                             | 3                | –   | ns   |
| t <sub>ACE</sub>                   | $\overline{\text{CE}}$ LOW to data valid                  | –                | 10  | ns   |
| t <sub>DOE</sub>                   | $\overline{\text{OE}}$ LOW to data valid                  | –                | 5   | ns   |
| t <sub>LZOE</sub>                  | $\overline{\text{OE}}$ LOW to Low Z <sup>[12]</sup>       | 0                |     | ns   |
| t <sub>HZOE</sub>                  | $\overline{\text{OE}}$ HIGH to High Z <sup>[11, 12]</sup> | –                | 5   | ns   |
| t <sub>LZCE</sub>                  | $\overline{\text{CE}}$ LOW to Low Z <sup>[12]</sup>       | 3                | –   | ns   |
| t <sub>HZCE</sub>                  | $\overline{\text{CE}}$ HIGH to High Z <sup>[11, 12]</sup> | –                | 5   | ns   |
| t <sub>PU</sub> <sup>[13]</sup>    | $\overline{\text{CE}}$ LOW to power-up                    | 0                | –   | ns   |
| t <sub>PD</sub> <sup>[13]</sup>    | $\overline{\text{CE}}$ HIGH to power-down                 | –                | 10  | ns   |
| t <sub>DBE</sub>                   | Byte enable to data valid                                 |                  | 5   | ns   |
| t <sub>LZBE</sub>                  | Byte enable to Low Z                                      | 0                | –   | ns   |
| t <sub>HZBE</sub>                  | Byte disable to High Z                                    | –                | 5   | ns   |
| Write Cycle <sup>[14, 15]</sup>    |   |                  |     |      |
| t <sub>WC</sub>                    | Write cycle time  | 10               | –   | ns   |
| t <sub>SCE</sub>                   | $\overline{\text{CE}}$ LOW to write end                   | 7                | –   | ns   |
| t <sub>AW</sub>                    | Address set-up to write end                               | 7                | –   | ns   |
| t <sub>HA</sub>                    | Address hold from write end                               | 0                | –   | ns   |
| t <sub>SA</sub>                    | Address set-up to write start                             | 0                | –   | ns   |
| t <sub>PWE</sub>                   | $\overline{\text{WE}}$ pulse width                        | 7                | –   | ns   |
| t <sub>SD</sub>                    | Data set-up to write end                                  | 6                | –   | ns   |
| t <sub>HD</sub>                    | Data hold from write end                                  | 0                | –   | ns   |
| t <sub>LZWE</sub>                  | $\overline{\text{WE}}$ HIGH to Low Z <sup>[12]</sup>      | 3                | –   | ns   |
| t <sub>HZWE</sub>                  | $\overline{\text{WE}}$ LOW to High Z <sup>[11, 12]</sup>  | –                | 5   | ns   |
| t <sub>BW</sub>                    | Byte enable to end of write                               | 7                | –   | ns   |

### Notes

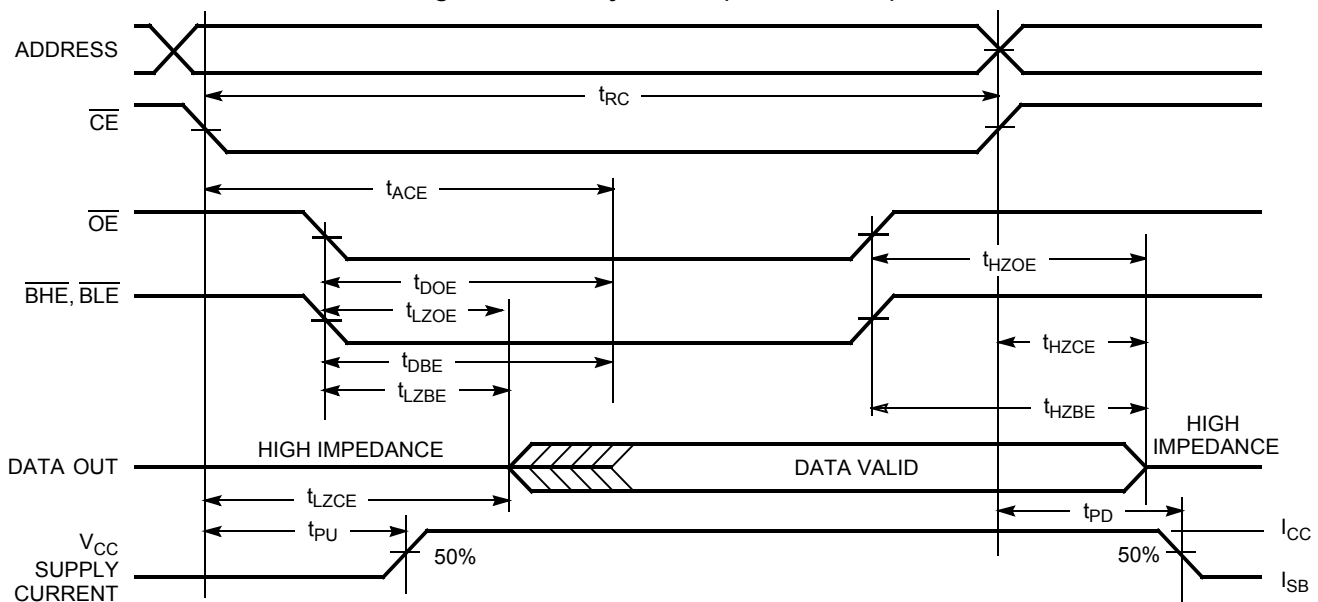
9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and 30-pF load capacitance.
10.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access can be performed.
11.  $t_{\text{HZOE}}$ ,  $t_{\text{HZBE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (c) of Figure 2 on page 5. Transition is measured when the outputs enter a high impedance state.
12. At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
13. This parameter is guaranteed by design and is not tested.
14. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW,  $\overline{\text{WE}}$  LOW and  $\overline{\text{BHE}}/\overline{\text{BLE}}$  LOW.  $\overline{\text{CE}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{BHE}}/\overline{\text{BLE}}$  must be LOW to initiate a write and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
15. The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) should be equal to the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms

**Figure 4. Read Cycle No.1 (Address Transition Controlled)** [16, 17]



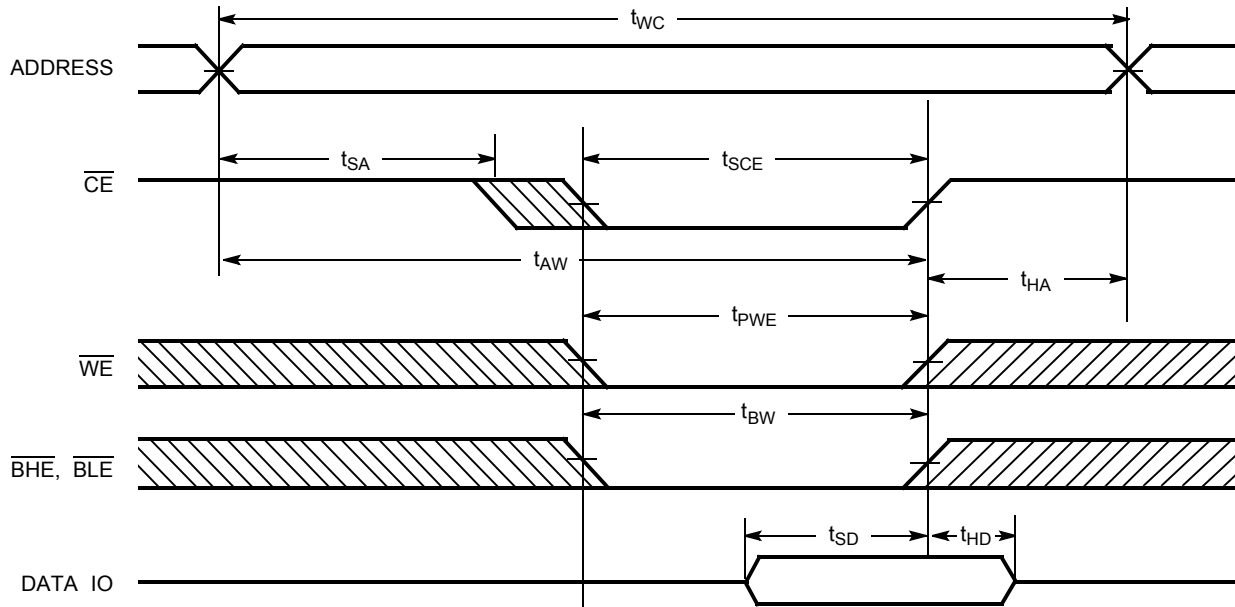
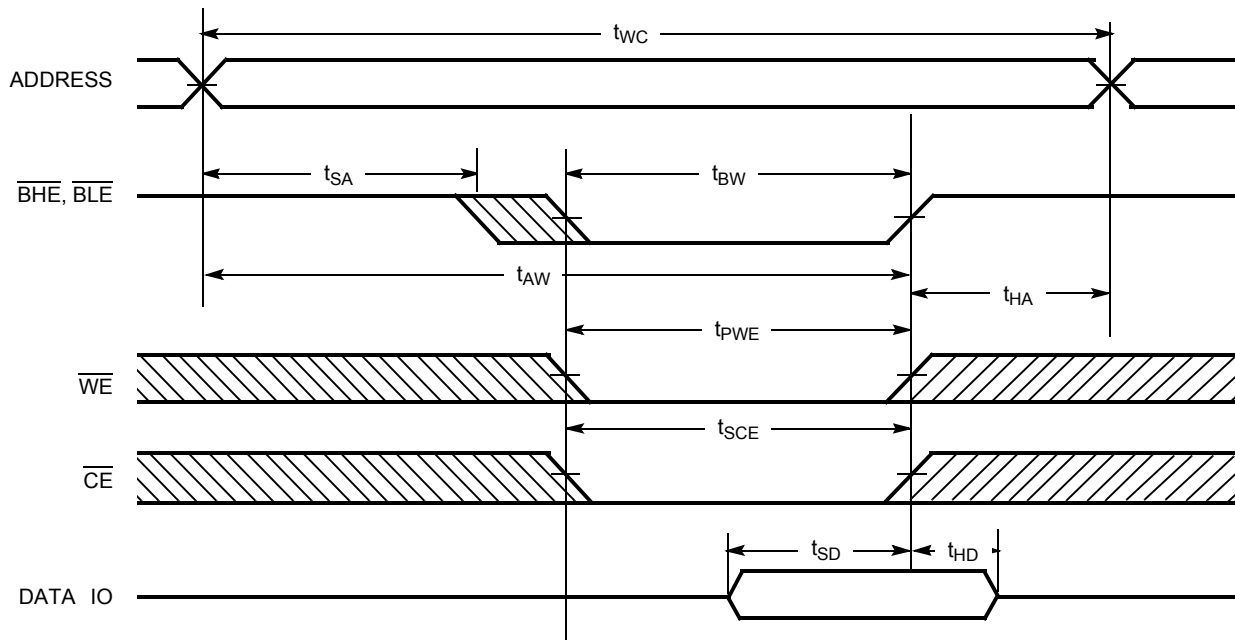
**Figure 5. Read Cycle No.2 ( $\overline{OE}$  Controlled)** [17, 18]



### Notes

16. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
17.  $\overline{WE}$  is HIGH for read cycle.
18. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.



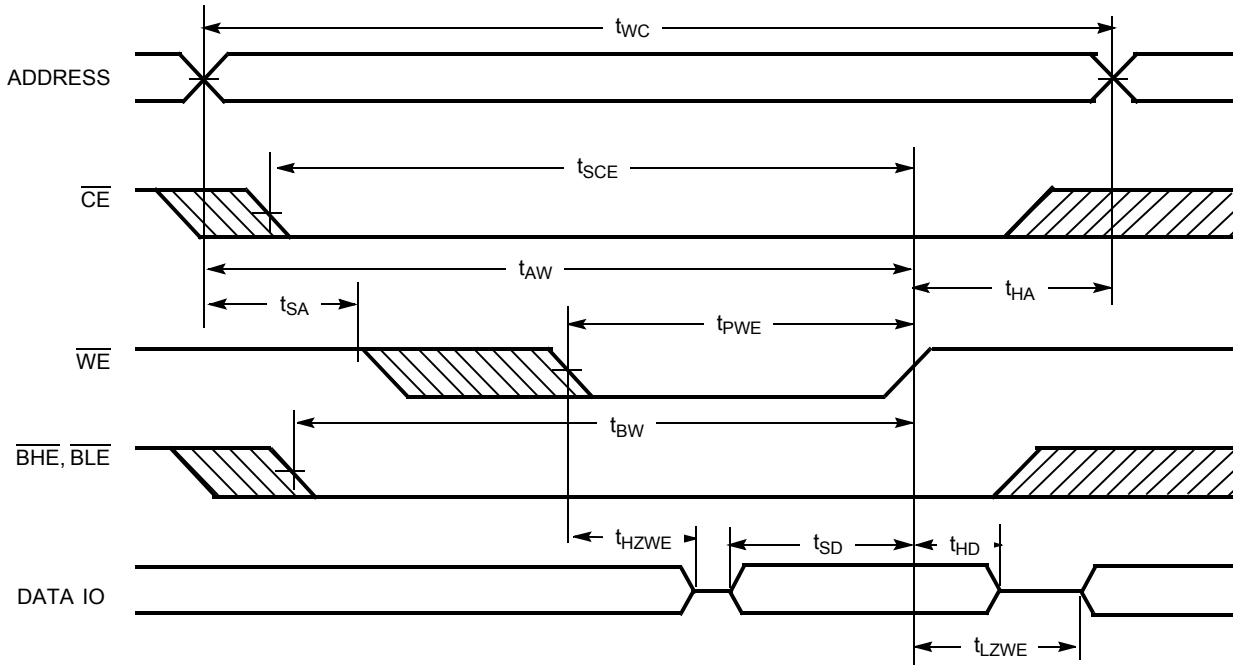
**Switching Waveforms(continued)**
**Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [19, 20]**

**Figure 7. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled) [19, 20]**

**Notes**

19. Data IO is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .

20. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

## Switching Waveforms(continued)

**Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [21, 22]**



### Notes

21. The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) should be equal to the sum of  $t_{HZWE}$  and  $t_{SD}$ .  
 22. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Truth Table**

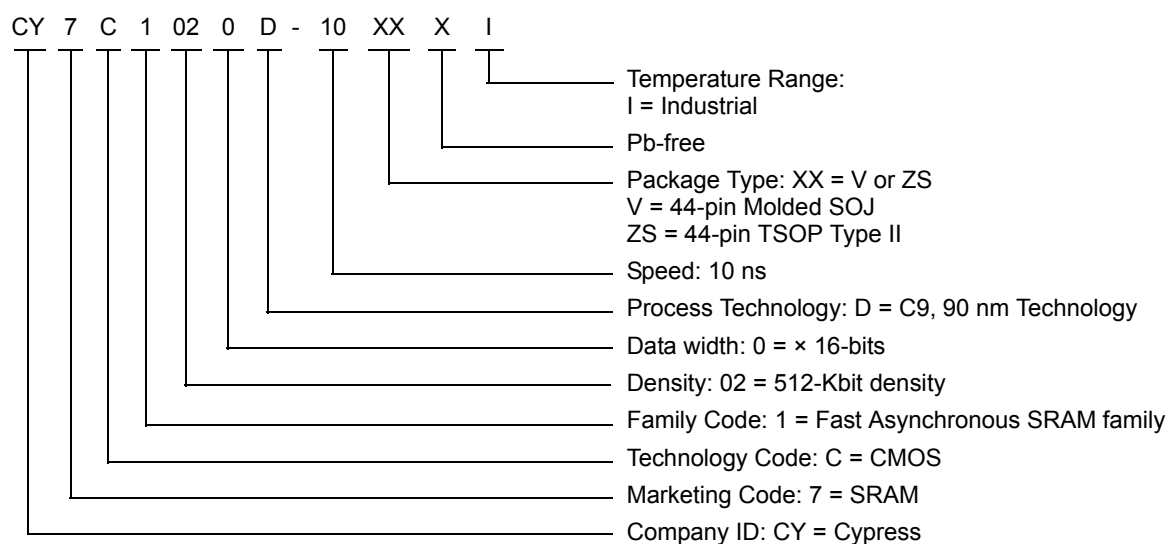
| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | IO <sub>0</sub> -IO <sub>7</sub> | IO <sub>8</sub> -IO <sub>15</sub> | Mode                       | Power                      |
|-----------------|-----------------|-----------------|------------------|------------------|----------------------------------|-----------------------------------|----------------------------|----------------------------|
| H               | X               | X               | X                | X                | High Z                           | High Z                            | Power-down                 | Standby (I <sub>SB</sub> ) |
| L               | L               | H               | L                | L                | Data out                         | Data out                          | Read – All bits            | Active (I <sub>CC</sub> )  |
|                 |                 |                 | L                | H                | Data out                         | High Z                            | Read – Lower bits only     | Active (I <sub>CC</sub> )  |
|                 |                 |                 | H                | L                | High Z                           | Data out                          | Read – Upper bits only     | Active (I <sub>CC</sub> )  |
| L               | X               | L               | L                | L                | Data in                          | Data in                           | Write – All bits           | Active (I <sub>CC</sub> )  |
|                 |                 |                 | L                | H                | Data in                          | High Z                            | Write – Lower bits only    | Active (I <sub>CC</sub> )  |
|                 |                 |                 | H                | L                | High Z                           | Data in                           | Write – Upper bits only    | Active (I <sub>CC</sub> )  |
| L               | H               | H               | X                | X                | High Z                           | High Z                            | Selected, outputs disabled | Active (I <sub>CC</sub> )  |
| L               | X               | X               | H                | H                | High Z                           | High Z                            | selected, outputs disabled | Active (I <sub>CC</sub> )  |

## Ordering Information

| Speed (ns) | Ordering Code    | Package Diagram | Package Type                  | Operating Range |
|------------|------------------|-----------------|-------------------------------|-----------------|
| 10         | CY7C1020D-10VXI  | 51-85082        | 44-pin SOJ (400 Mils) Pb-free | Industrial      |
|            | CY7C1020D-10ZSXI | 51-85087        | 44-pin TSOP (Type II) Pb-free |                 |

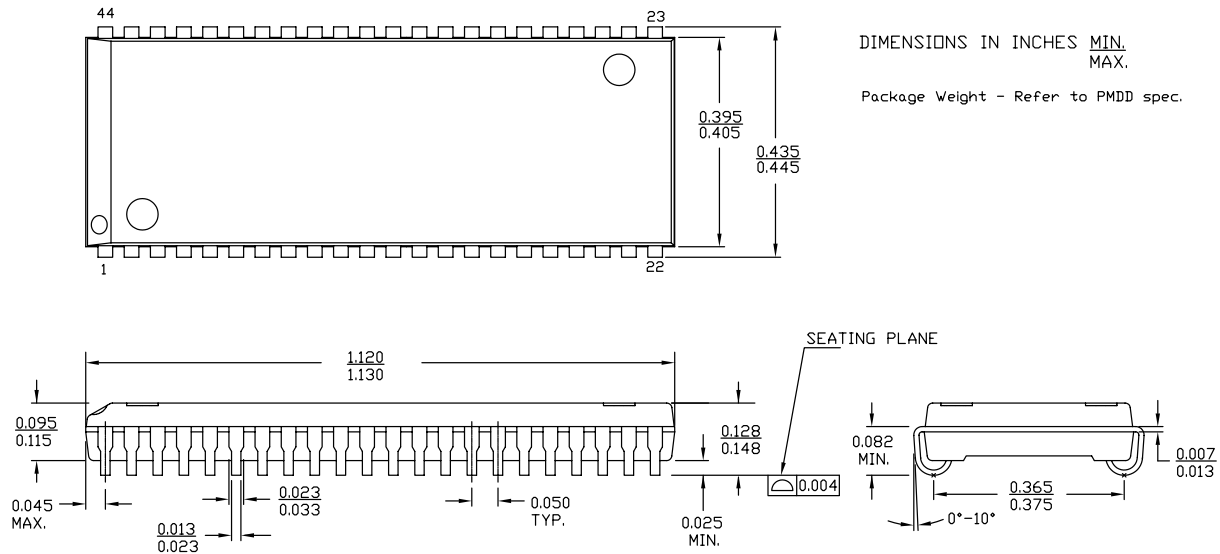
Please contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions



## Package Diagrams

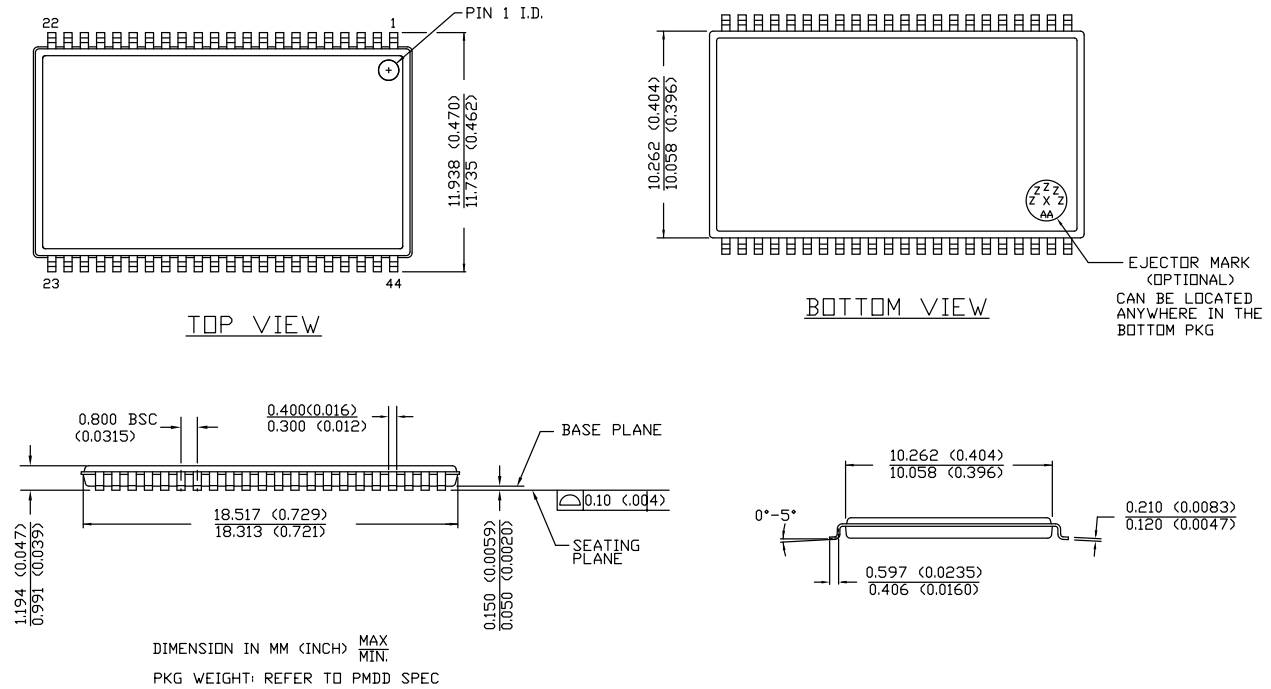
**Figure 9. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082**



51-85082 \*E

## Package Diagrams(continued)

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 \*E

## Acronyms

| Acronym | Description                             |
|---------|---|
| BGA     | Ball Grid Array                         |
| CMOS    | Complementary Metal Oxide Semiconductor |
| FBGA    | Fine-Pitch Ball Grid Array              |
| I/O     | Input/Output                            |
| SRAM    | Static Random Access Memory             |
| TSOP    | Thin Small Outline Package              |
| TTL     | Transistor-Transistor Logic             |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| mA     | milliampere     |
| ns     | nanosecond      |
| Ω      | ohm             |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

| Document Title: CY7C1020D, 512-Kbit (32 K × 16) Static RAM<br>Document Number: 38-05463 |         |            |                 |  |
|---|---------|------------|-----------------|--|
| Rev.  | ECN No. | Issue Date | Orig. of Change | Description of Change  |
| **  | 201560  | See ECN    | SWI             | Advance Data sheet for C9 IPP  |
| *A  | 233695  | See ECN    | RKF             | 1) DC parameters modified as per EROS (Spec # 01-0216)<br>2) Pb-free Offering in the 'Ordering Information'  |
| *B  | 263769  | See ECN    | RKF             | 1) Corrected pin #18 on SOJ/TSOPII Pinout (Page #1) from A <sub>15</sub> to A <sub>4</sub><br>2) Changed IO <sub>1</sub> - IO <sub>16</sub> to IO <sub>0</sub> - IO <sub>15</sub> on the Pin-out diagram<br>3) Added T <sub>power</sub> Spec in Switching Characteristics Table<br>4) Added Data Retention Characteristics Table and Waveforms<br>5) Shaded 'Ordering Information'   |
| *C  | 307594  | See ECN    | RKF             | Reduced Speed bins to -10, -12 and -15 ns  |
| *D  | 560995  | See ECN    | VKN             | Converted from Preliminary to Final<br>Removed Commercial Operating range<br>Removed 12 ns speed bin<br>Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz<br>Updated Thermal Resistance table<br>Updated Ordering Information Table<br>Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #3   |
| *E  | 802877  | See ECN    | VKN             | Changed I <sub>CC</sub> specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz   |
| *F  | 3109992 | 12/14/2010 | AJU             | Added <a href="#">Ordering Code Definitions</a> .<br>Updated <a href="#">Package Diagrams</a> .  |
| *G  | 3219056 | 04/07/2011 | PRAS            | Added TOC<br>Added Acronyms and Units of Measure table.<br>Updated Datasheet as per template.  |
| *H  | 4033925 | 06/19/2013 | MEMJ            | Updated <a href="#">Functional Description</a> .<br>Updated <a href="#">Electrical Characteristics</a> :<br>Added one more Test Condition "I <sub>OH</sub> = -0.1mA" for V <sub>OH</sub> parameter and added maximum value corresponding to that Test Condition.<br>Added Note 4 and referred the same note in maximum value for V <sub>OH</sub> parameter corresponding to Test Condition "I <sub>OH</sub> = -0.1mA".<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85082 – Changed revision from *C to *E.<br>spec 51-85087 – Changed revision from *C to *E. |
| *I  | 4385769 | 05/21/2014 | MEMJ            | No technical updates.<br>Completing Sunset Review.   |
| *J  | 4576526 | 11/21/2014 | MEMJ            | Added related documentation hyperlink in page 1.   |



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