

SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

SDLS004

D2633, JANUARY 1981—REVISED MARCH 1988

- Parallel Register Inputs ('LS592)
- Parallel 3-State I/O: Register Inputs/ Counter Outputs ('LS593)
- Counter has Direct Overriding Load and Clear
- Accurate Counter Frequency:
DC to 20 MHz

description

The 'LS592 comes in a 16-pin package and consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive-edge-triggered clocks. In addition, the counter has direct load and clear functions. A low-going RCO pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting RCO of the first stage to CCKEN of the second stage. Cascading for larger count chains can be accomplished by connecting RCO of each stage to CCK of the following stage.

The 'LS593 comes in a 20-pin package and has all the features of the 'LS592 plus 3-state I/O, which provides parallel counter outputs. The tables below show the operation of the enable (CCKEN, CCKEN) inputs. A register clock enable (RCKEN) is also provided.

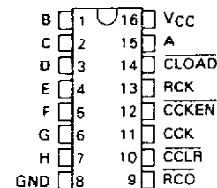
OUTPUT ENABLE CONTROL ('593 ONLY)

G	\bar{G}	A/Q_A thru H/Q_H
L	L	input mode
L	H	input mode
H	L	output mode
H	H	input mode

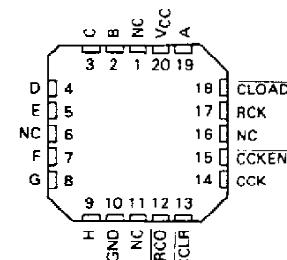
COUNTER CLOCK ENABLE CONTROL

CCKEN	CCKEN	EFFECT ON CCK
L	L	Enable
L	H	Disable
H	L	Enable
H	H	Enable

SN54LS592 . . . J OR W PACKAGE
SN74LS592 . . . N PACKAGE

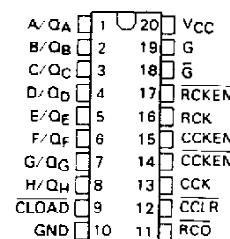


SN54LS592 . . . FK PACKAGE
(TOP VIEW)

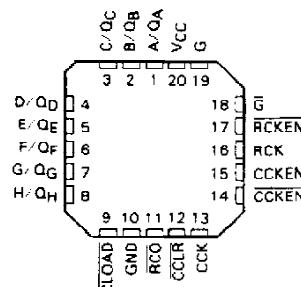


NC — No internal connection

SN54LS593 . . . J OR W PACKAGE
SN74LS593 . . . DW OR N PACKAGE
(TOP VIEW)



SN64LS693 . . . FK PACKAGE
(TOP VIEW)

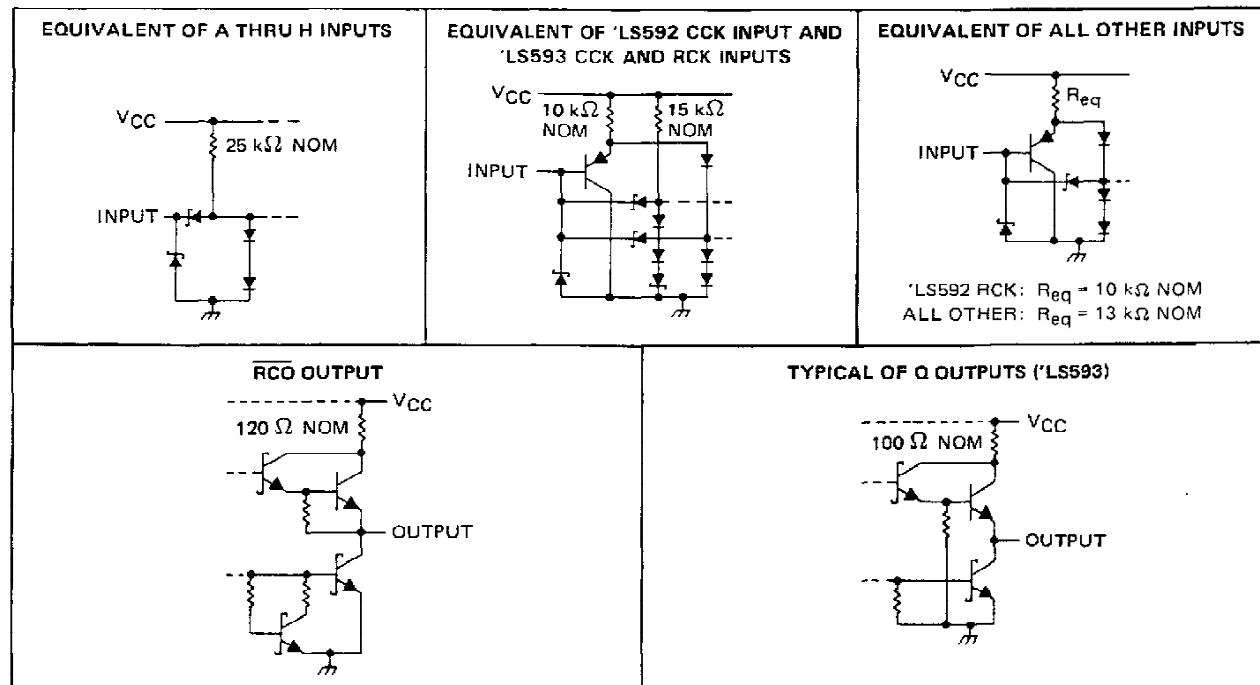


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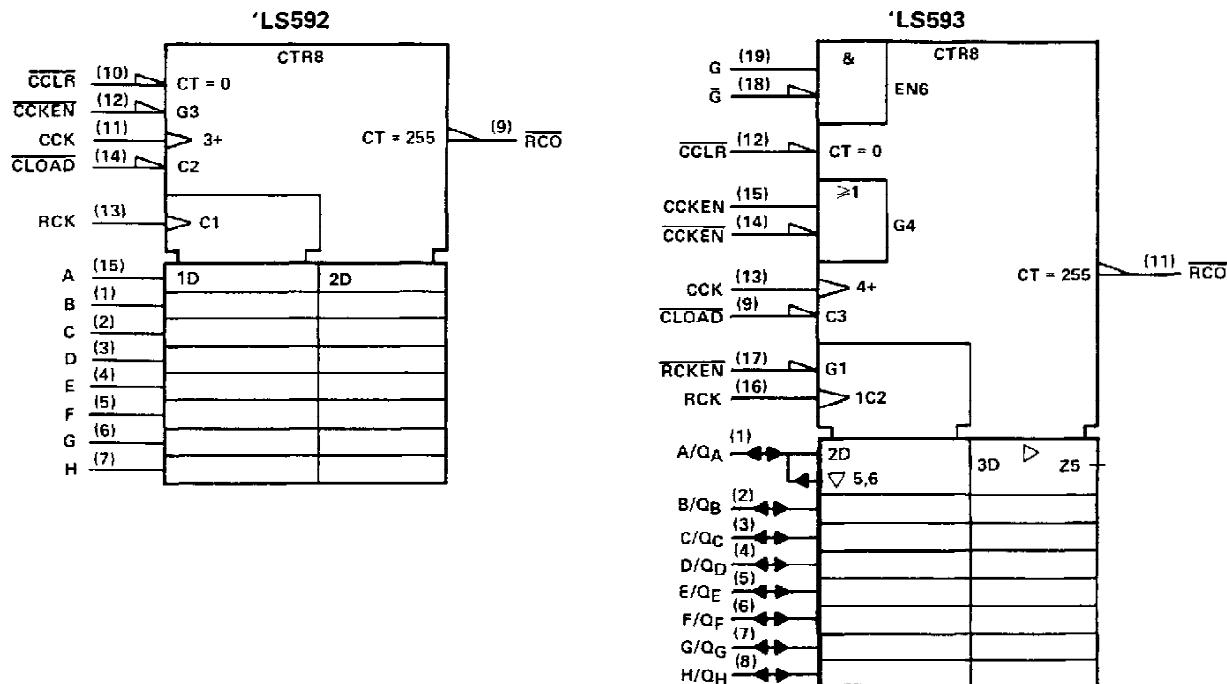
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schematics of inputs and outputs



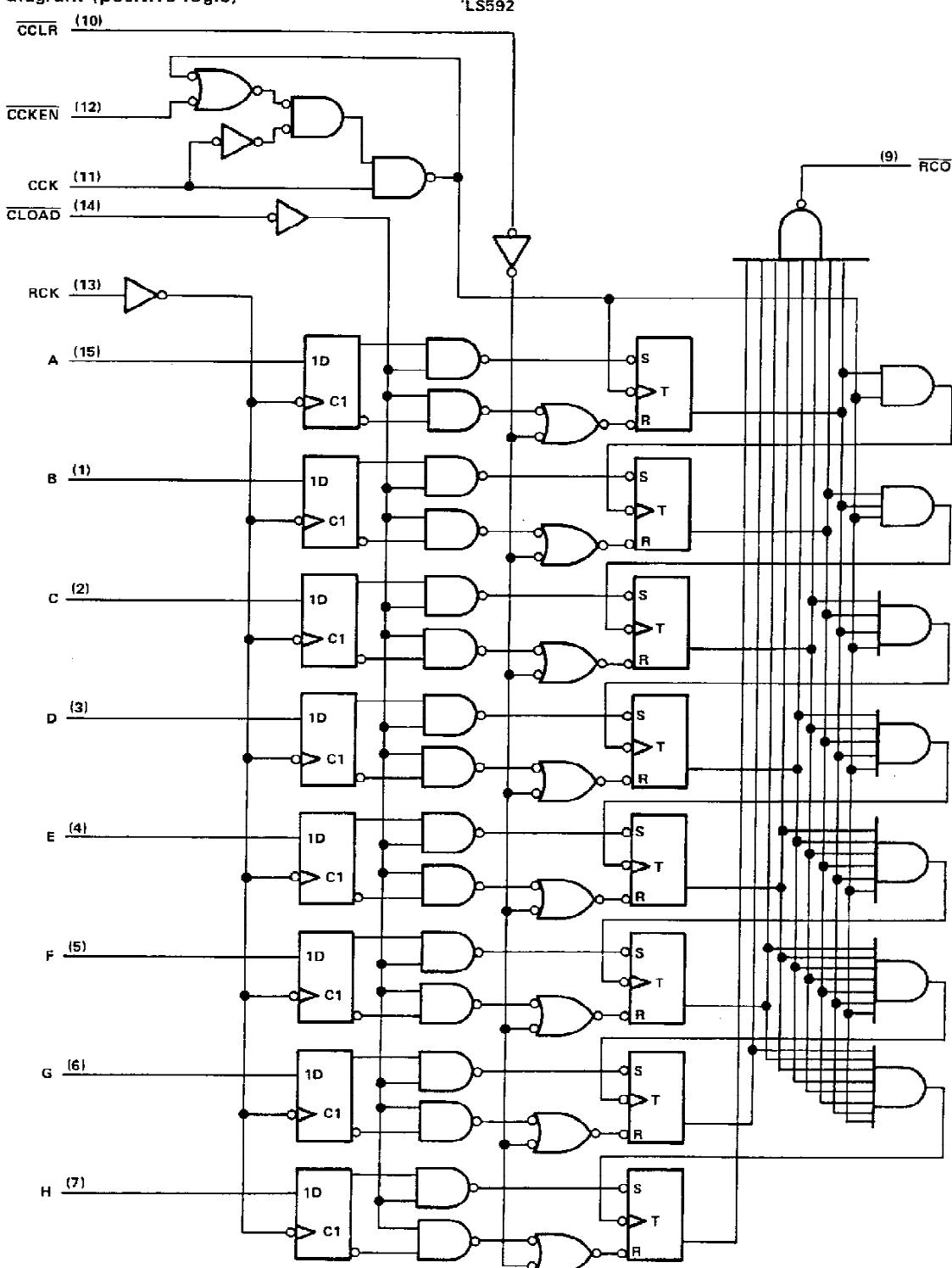
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

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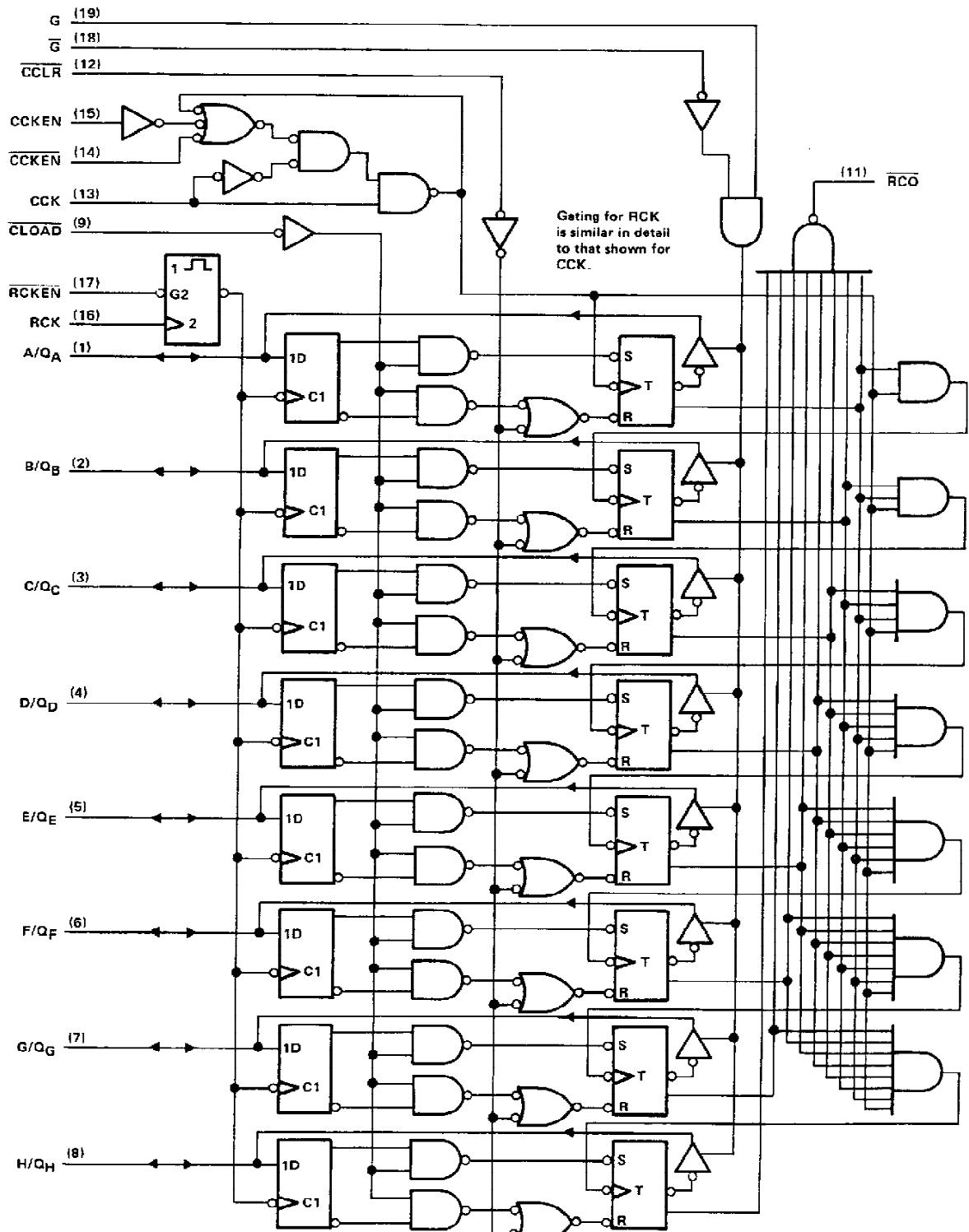
logic diagram (positive logic)



SN54LS593, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

logic diagram (positive logic)

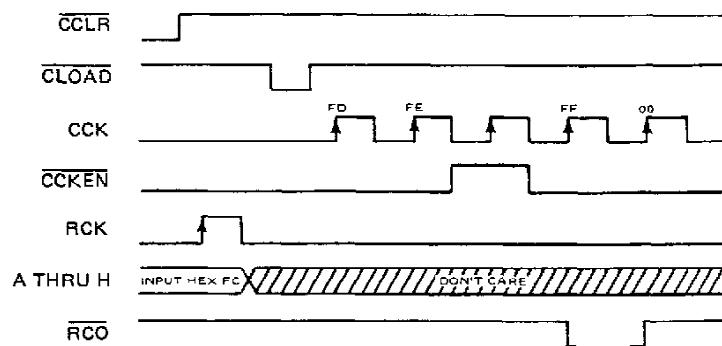
'LS593



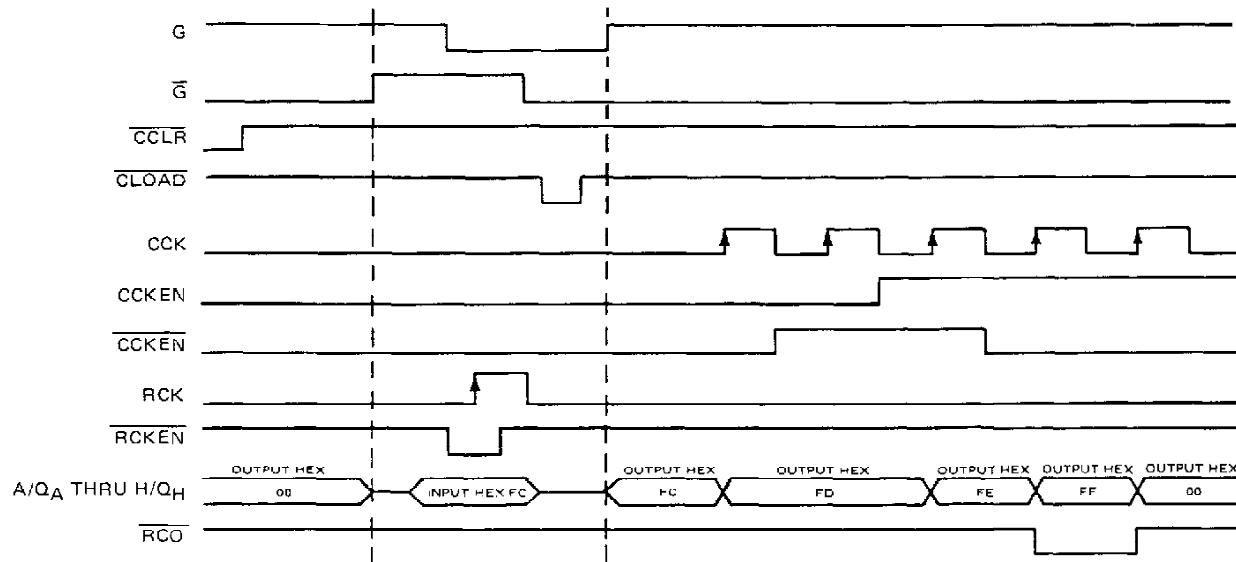
**SN54LS592, SN54LS593, SN74LS592, SN74LS593
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typical operating sequences

'LS592



'LS593



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SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current	RCO		—1	—1			mA
		Q 'LS593 only		—1	—2.6			
I _{OL}	Low-level output current	RCO		8	16			mA
		Q 'LS593 only		12	24			
f _{CCK}	Counter clock frequency	0	20	0	0	20	MHz	
t _w (CCK)	Duration of counter clock pulse	25			25			ns
t _w (CCLR)	Duration of counter clear pulse	20			20			ns
t _w (RCK)	Duration of register clock pulse	20			20			ns
t _w (CLOAD)	Duration of counter load pulse	40			40			ns
t _{su}	Register enable setup time	RCKEN low to RCK ↑, 'LS593		20	20			ns
t _{su}	Counter enable setup time before CCK ↑	CCKEN low, 'LS592		30	30			ns
		CCKEN low or CCKEN high, 'LS593		30	30			
t _{su}	Setup time	CCLR inactive before CCK ↑		20	20			ns
		CLOAD inactive before CCK ↑		20	20			
		RCK ↑ before CLOAD ↑ (see Note 2)		30	30			
		Data A thru H before RCK ↑		20	20			
		Data A thru H after RCK ↑		0	0			
t _h	Hold time	All others		0	0			ns
		Operating free-air temperature		—55	125		0	
T _A					70			°C

NOTE 2: This time insures the data saved by RCK ↑ will also be loaded into the counter.

SN54LS592, SN54LS593, SN74LS592, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS [*]			SN74LS [*]			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
VIK		V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	'LS593 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -1 mA	2.4	3.2				V
	RCO		I _{OH} = -2.6 mA			2.4	3.1		
			I _{OH} = -1 mA	2.4	3.2	2.4	3.2		
V _{OL}	'LS593 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA		0.25	0.4	0.25	0.4	V
	RCO		I _{OL} = 24 mA			0.35	0.5		
			I _{OL} = 8 mA	0.25	0.4	0.25	0.4		
			I _{OL} = 16 mA			0.35	0.5		
IOZH	'LS593 Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 2.7 V			20		20		μA
IOZL	'LS593 Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 0.4 V			-0.4		-0.4		mA
II	'LS593 Q	V _{CC} = MAX	V _I = 5.5 V			0.1		0.1	mA
	Others		V _I = 7 V			0.1		0.1	
IIH		V _{CC} = MAX, V _I = 2.7 V			20		20		μA
IIL	CCK	V _{CC} = MAX, V _I = 0.4 V			-0.8		-0.8		
	RCK				-0.2		-0.2		
	'LS592				-0.8		-0.8		
	'LS593				-0.4		-0.4		
	A thru H				-0.2		-0.2		
IOS [§]	'LS593 Q	V _{CC} = MAX, V _O = 0 V			-30	-130	-30	-130	mA
	RCO				-20	-100	-20	-100	
ICC	'LS592	V _{CC} = MAX, All possible inputs grounded, All outputs open	I _{CCH}		40	60	40	60	mA
			I _{CCL}		40	60	40	60	
			I _{CCH}		47	70	47	70	
			I _{CCL}		53	80	53	80	
			I _{CCZ}		57	85	57	85	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ C$, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS592			'LS593			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CCK	RCO	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	20	35		20	35		MHz
t_{PLH}	CCK \uparrow	Q					14	21	ns	
t_{PHL}	CCK \uparrow	Q					26	39	ns	
t_{PLH}	CLOAD \downarrow	Q					34	51	ns	
t_{PHL}	CLOAD \downarrow	Q					28	42	ns	
t_{PHL}	CCLR \downarrow	Q					25	38	ns	
t_{PZH}	G \uparrow	Q					31	47	ns	
t_{PZL}	G \uparrow	Q					27	40	ns	
t_{PZH}	\overline{G} \downarrow	Q					29	45	ns	
t_{PZL}	\overline{G} \downarrow	Q					31	47	ns	
t_{PHZ}	G \downarrow	Q	$R_L = 667\text{ }\Omega$, $C_L = 5\text{ pF}$				33	50	ns	
t_{PLZ}	G \downarrow	Q					35	52	ns	
t_{PHZ}	\overline{G} \uparrow	Q					26	39	ns	
t_{PLZ}	\overline{G} \uparrow	Q					28	42	ns	
t_{PLH}	CCK \uparrow	RCO	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	15	23		14	21	ns	
t_{PHL}	CCK \uparrow	RCO		20	30		20	30	ns	
t_{PLH}	CLOAD \downarrow	RCO		31	47		31	47	ns	
t_{PHL}	CLOAD \downarrow	RCO		27	41		27	41	ns	
t_{PLH}	CCLR \downarrow	RCO		30	45		30	45	ns	
t_{PLH}	RCK \uparrow	RCO	$R_L = 1\text{ k}\Omega$, $CLOAD = L$	35	53		42	63	ns	
t_{PHL}	RCK \uparrow	RCO		30	45		33	50	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87621012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87621012A SNJ54LS592FK	Samples
5962-8762101EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762101EA SNJ54LS592J	Samples
5962-8762101EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762101EA SNJ54LS592J	Samples
5962-8762101FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762101FA SNJ54LS592W	Samples
5962-8762101FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762101FA SNJ54LS592W	Samples
SN54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS592J	Samples
SN54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS592J	Samples
SN54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS593J	Samples
SN54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS593J	Samples
SN74LS592D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS592	Samples
SN74LS592D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS592	Samples
SN74LS592DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS592	Samples
SN74LS592DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS592	Samples
SN74LS592DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS592	Samples
SN74LS592DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS592	Samples
SN74LS592DR	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	LS592	
SN74LS592DR	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	LS592	
SN74LS592DRE4	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS592DRE4	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS592DRG4	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS592DRG4	OBsolete	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74LS592N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS592N	Samples
SN74LS592N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS592N	Samples
SN74LS592N3	OBsolete	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS592N3	OBsolete	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS592NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS592	Samples
SN74LS592NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS592	Samples
SN74LS593DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS593	Samples
SN74LS593DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS593	Samples
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS593	Samples
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS593	Samples
SN74LS593N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS593N	Samples
SN74LS593N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS593N	Samples
SN74LS593N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74LS593N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SNJ54LS592FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87621012A SNJ54LS 592FK	Samples
SNJ54LS592FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87621012A SNJ54LS 592FK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762101EA SNJ54LS592J	Samples
SNJ54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762101EA SNJ54LS592J	Samples
SNJ54LS592W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762101FA SNJ54LS592W	Samples
SNJ54LS592W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8762101FA SNJ54LS592W	Samples
SNJ54LS593FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 593FK	Samples
SNJ54LS593FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 593FK	Samples
SNJ54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS593J	Samples
SNJ54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS593J	Samples
SNJ54LS593W	OBsolete			20		TBD	Call TI	Call TI	-55 to 125		
SNJ54LS593W	OBsolete			20		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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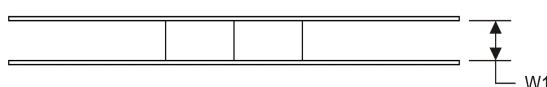
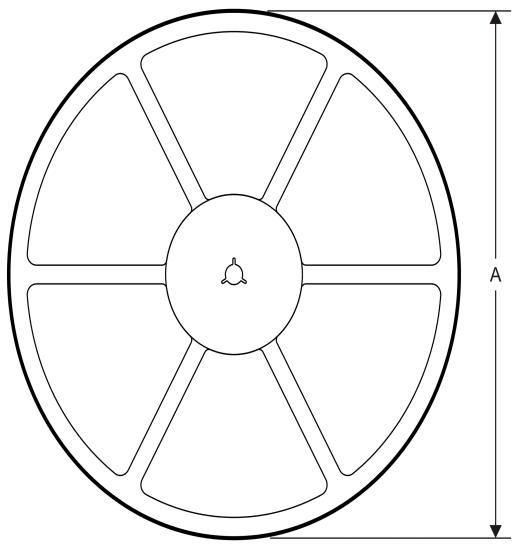
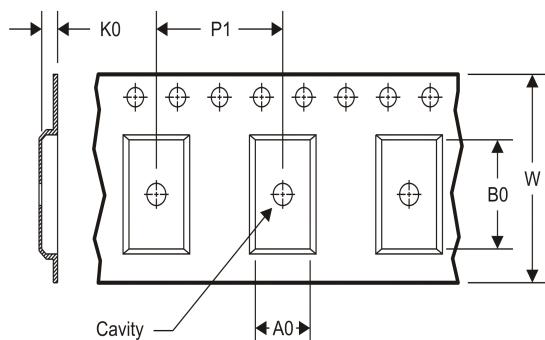
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OTHER QUALIFIED VERSIONS OF SN54LS592, SN54LS593, SN74LS592, SN74LS593 :

- Catalog: [SN74LS592](#), [SN74LS593](#)
- Military: [SN54LS592](#), [SN54LS593](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS592NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS593DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

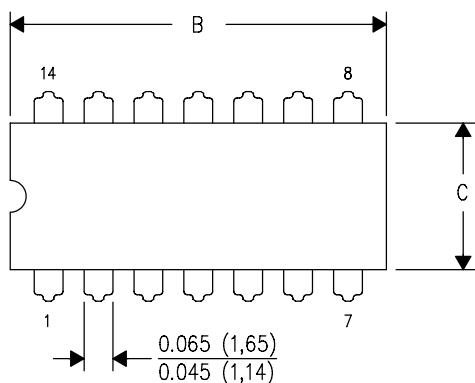

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS592NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LS593DWR	SOIC	DW	20	2000	367.0	367.0	45.0

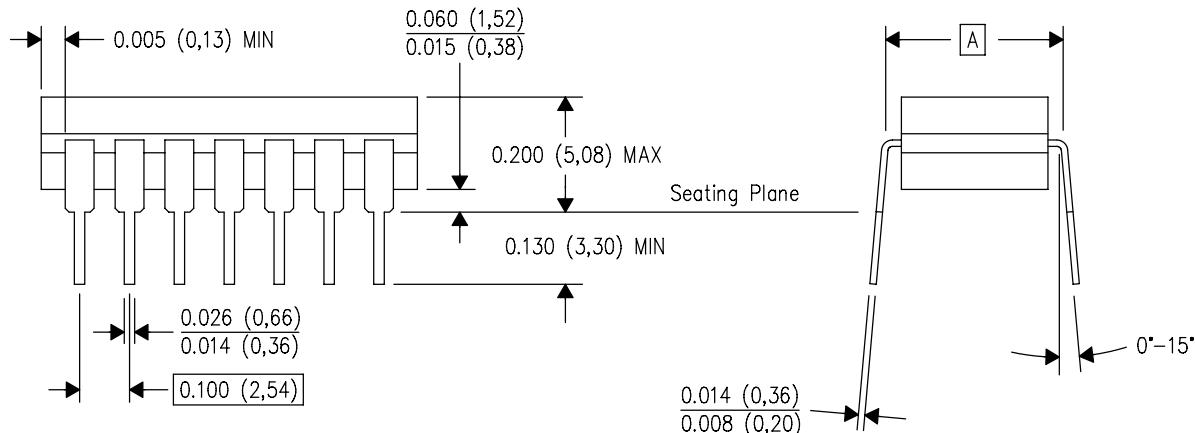
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

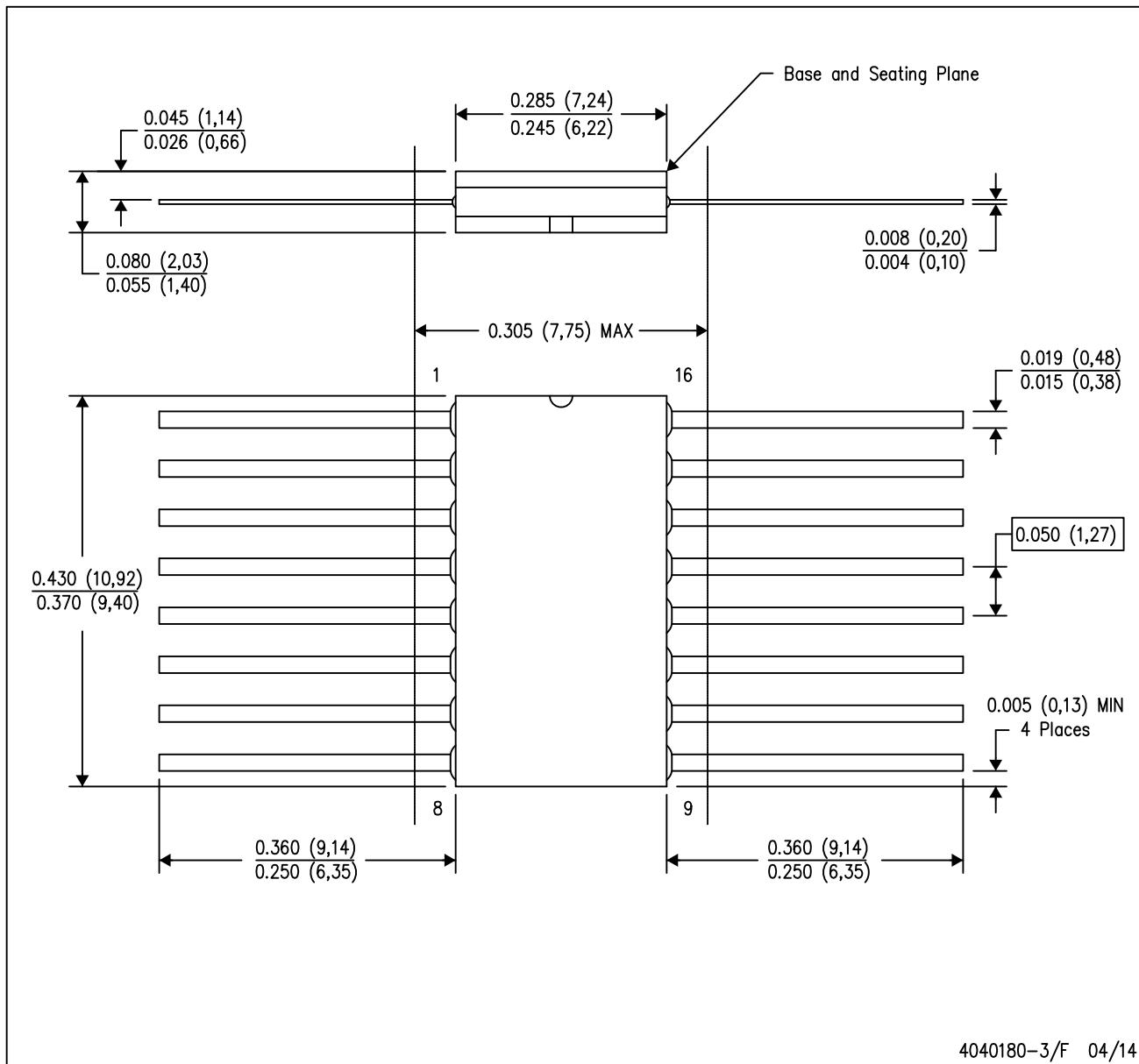


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/F 04/14

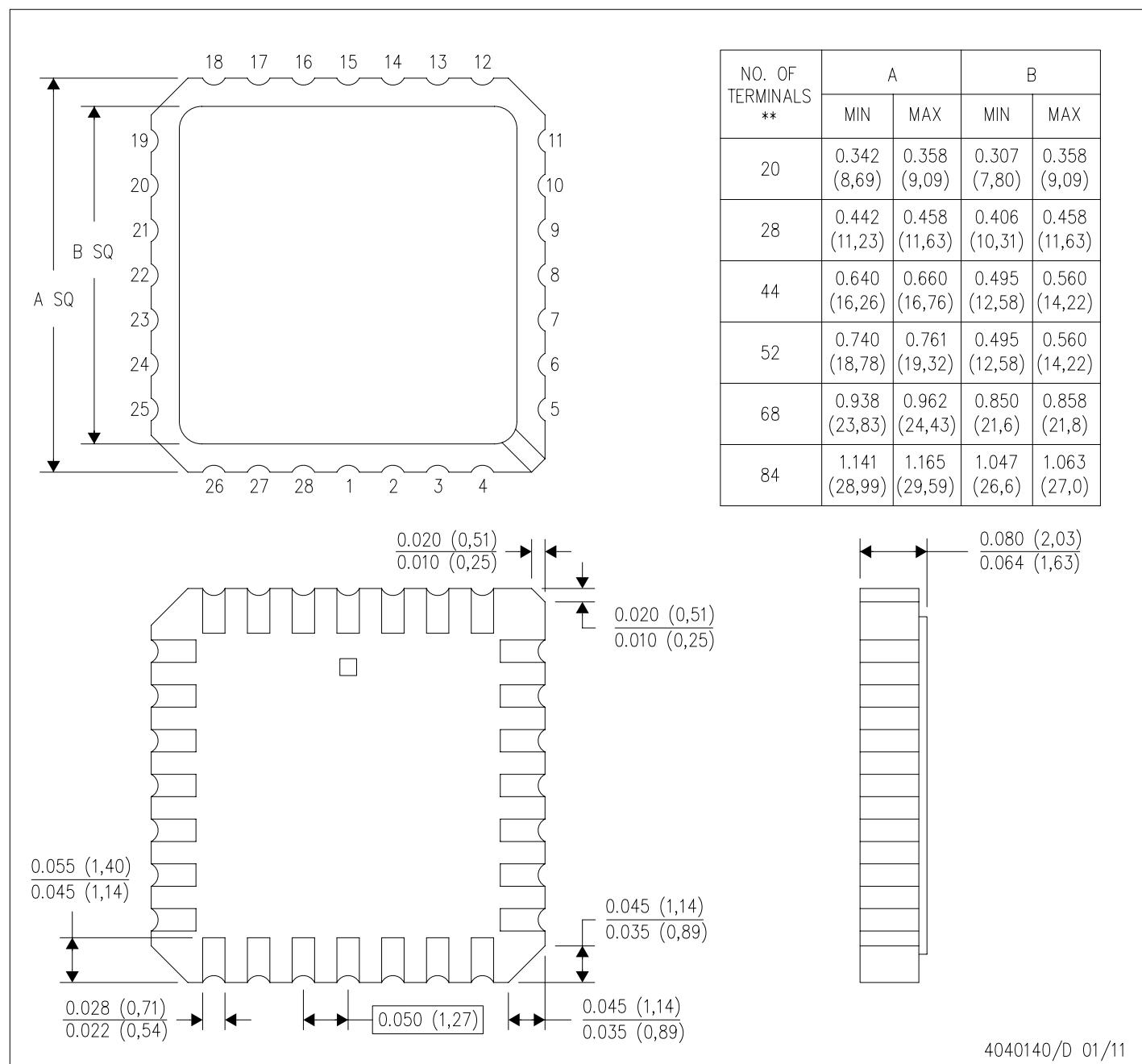
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP2-F16

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

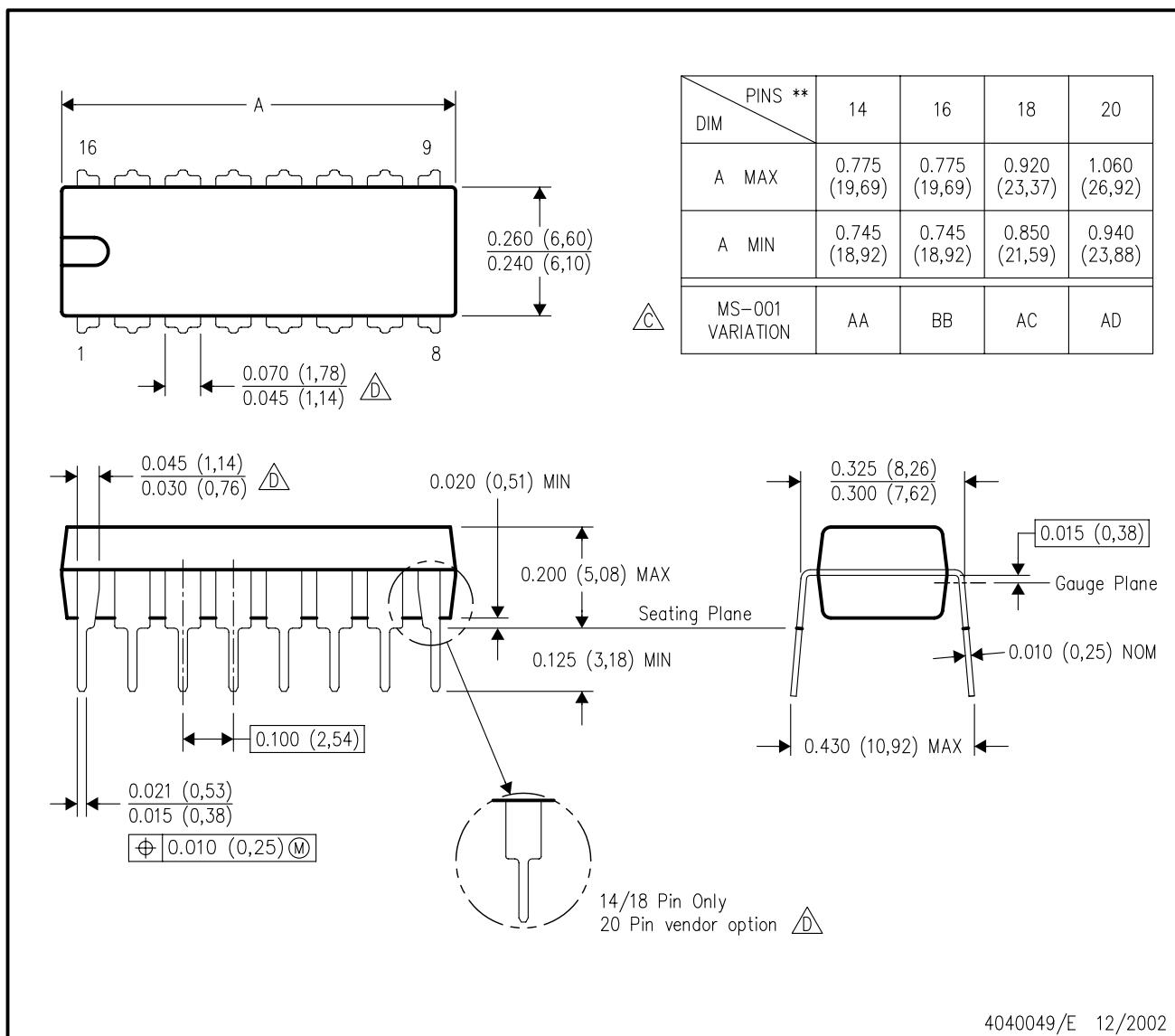
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a metal lid.
- Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

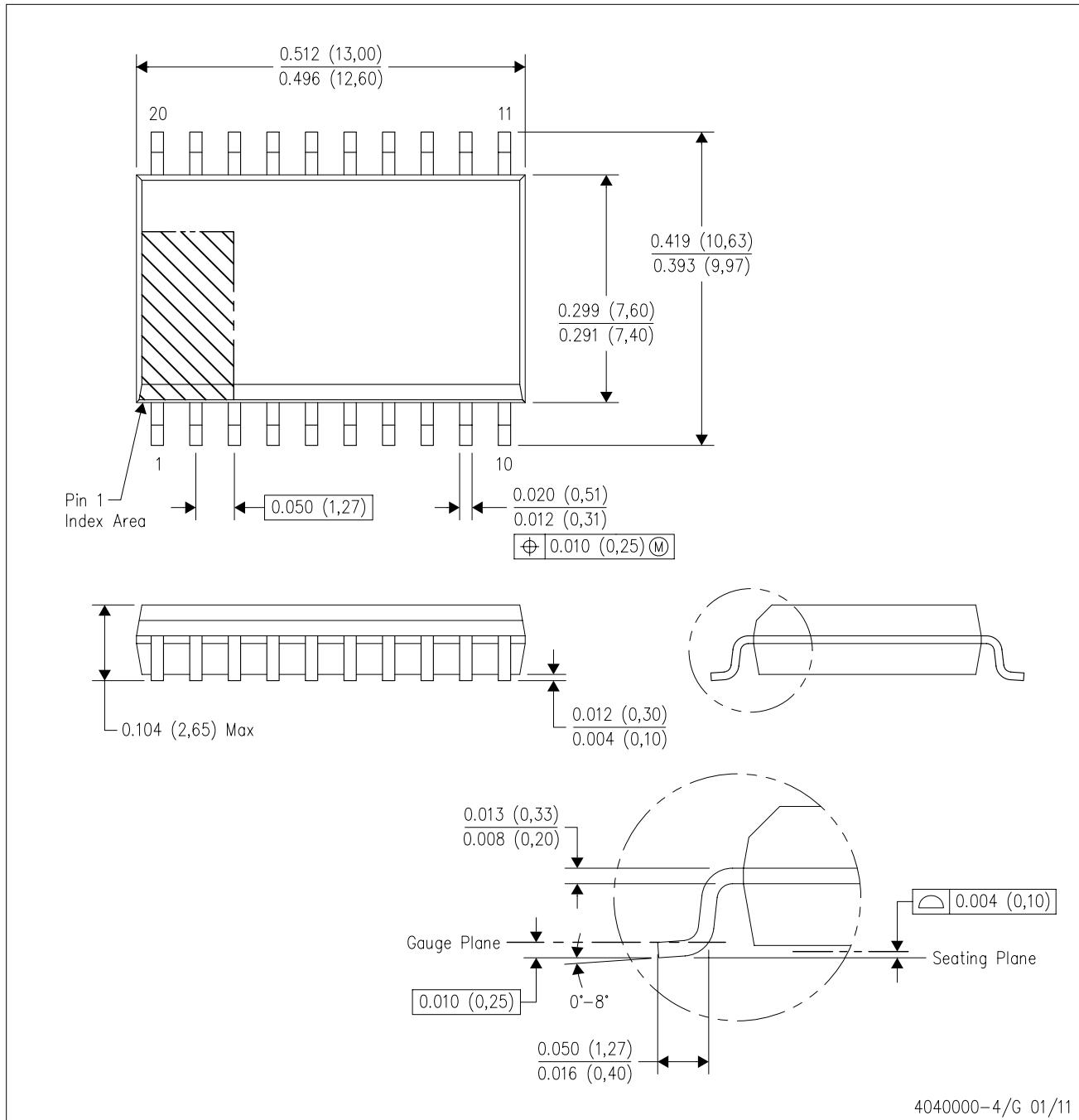
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

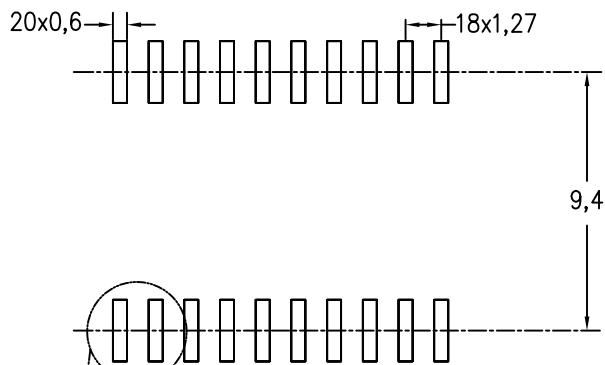
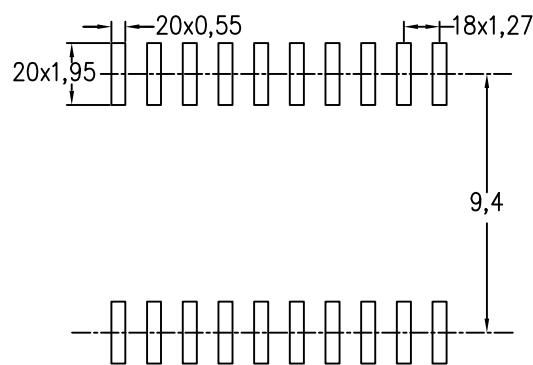


NOTES:

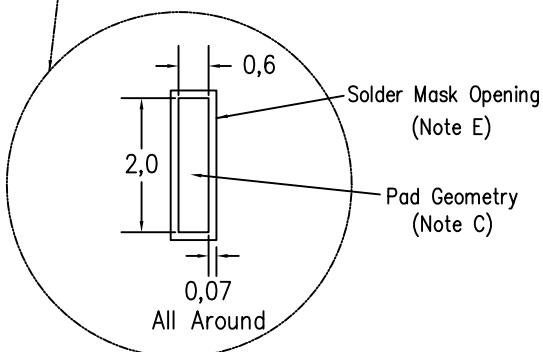
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)

Non Solder Mask Define Pad



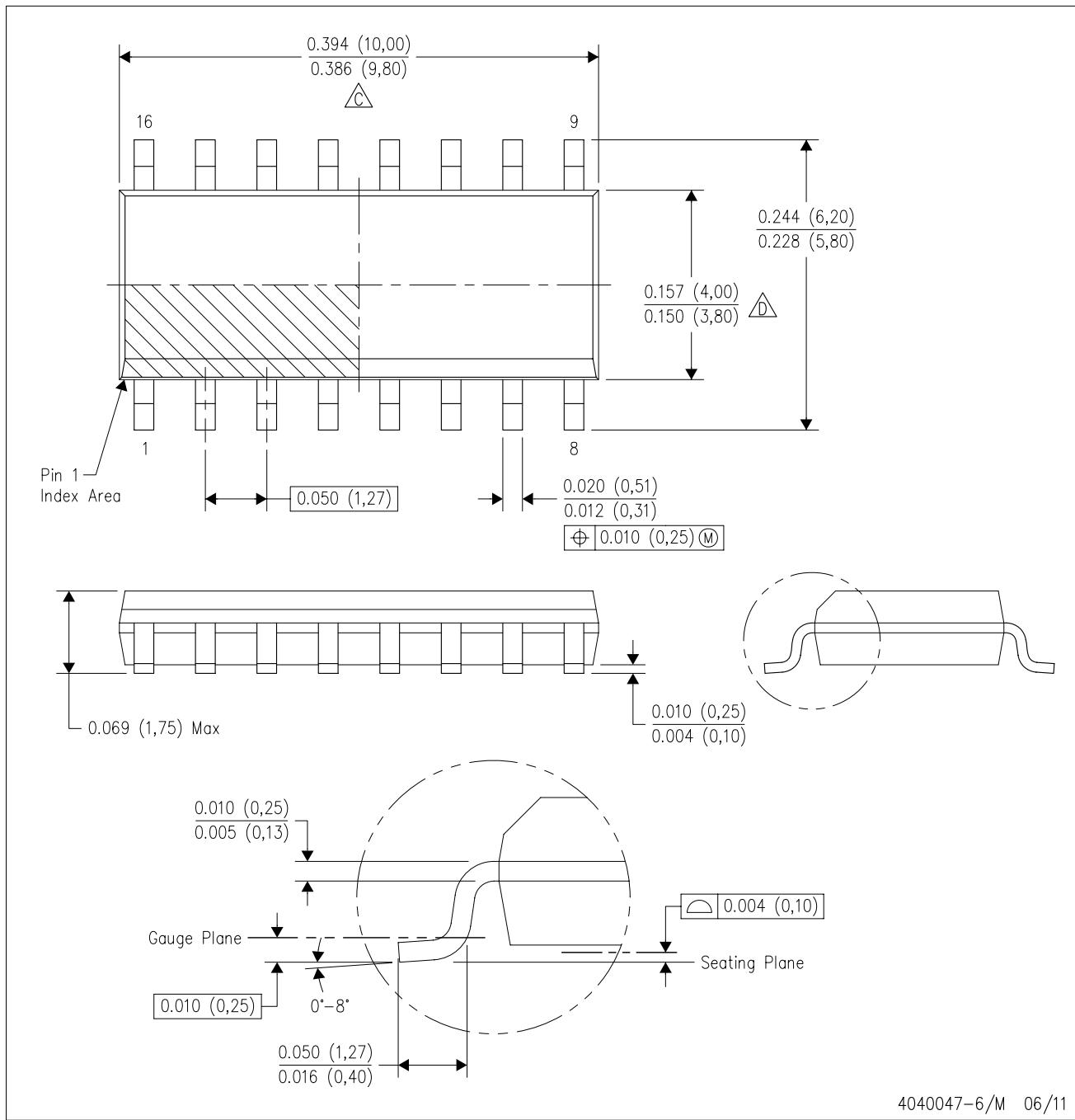
4209202-4/F 08/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

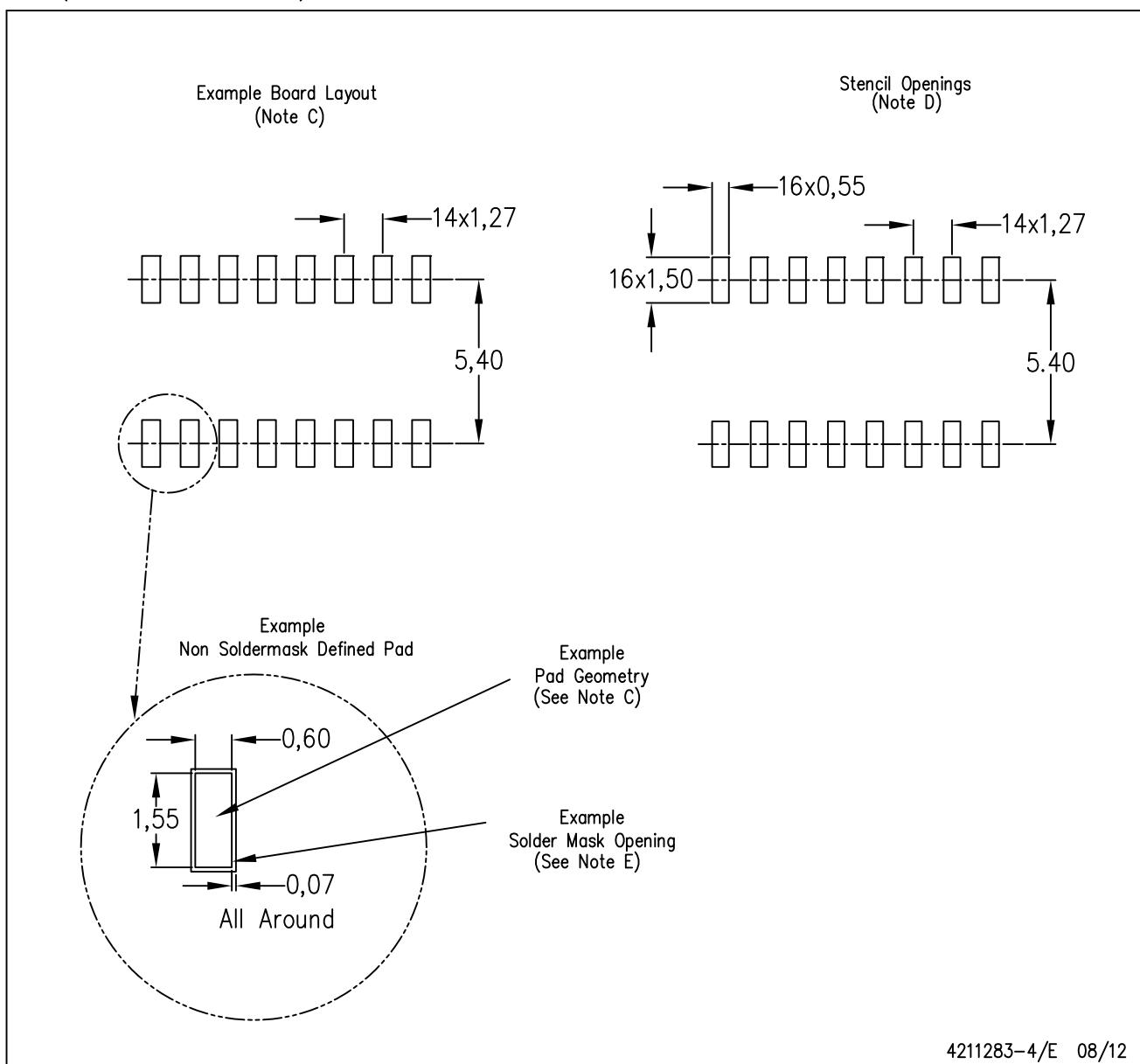
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

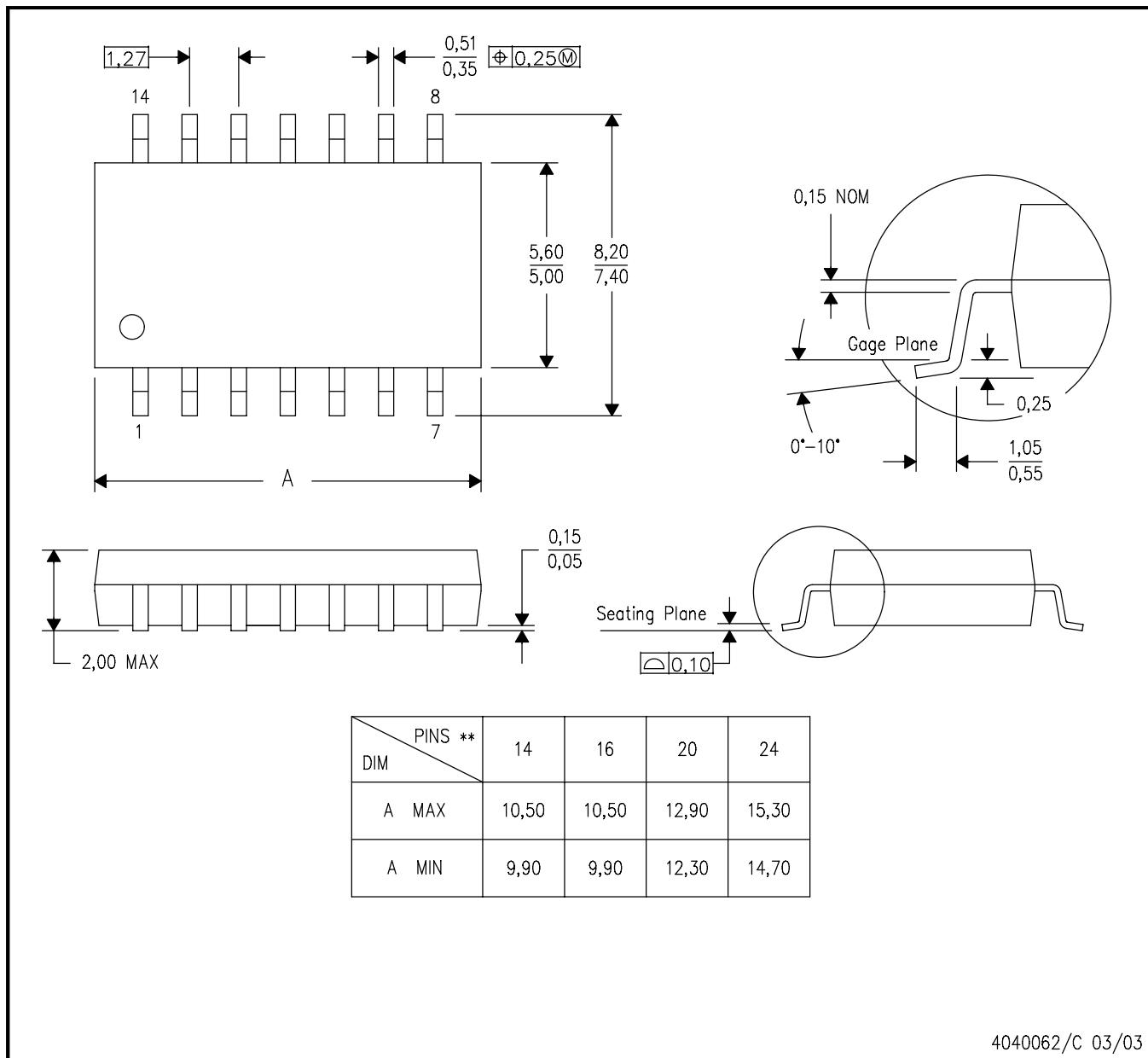
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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