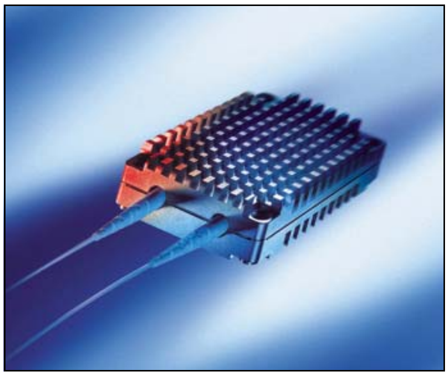
Fiber Optics

3.3 V, 4-Line LVDS Parallel 2.5 GBd Transponder OC-48 SONET/SDH Short Reach (SR) up to 2 km

V23816-N1018-C312-A
V23816-N1018-L312-A

Preliminary Data

Features



- Compliant with existing standards
- Compact integrated transponder unit with
  - FP laser diode transmitter
  - InGaAs PIN photodiode receiver
  - Pigtailed optical connections
  - Integrated Mux, Demux and Clock Recovery
- Class 1 FDA and IEC laser safety compliant
- Single +3.3 V power supply
- OC-48 optical transmit and receive at 2488.32 Mbit/s
- 4-line LVDS differential interface at 622.08 Mbit/s
- External control for laser shutoff
- Loss of optical signal and Loss of synch indicators (Rx)
- Loss of lock indicator for Tx high speed clock
- Laser bias monitor
- Rx power monitor output
- Loopback operating modes
- 155.520 MHz LVPECL input Tx reference clock
- 2.8 W Typical Power Consumption
- Tx Fault output indicator

Part Number	Connector Type	Fiber Length
V23816-N1018-C312-A	SC	24.1 ±0.8 "
V23816-N1018-L312-A	LC	24.1 ±0.8 "

Connector Pin Assignments

Pin No.	Signal Name	Pin No.	Signal Name
1	TxDATAP0	2	SLPTIME
3	TxDATAN0	4	RLPTIME
5	GND	6	GND
7	TxDATAP1	8	PCLKN
9	TxDATAN1	10	PCLKP
11	GND	12	GND
13	TxDATAP2	14	SDSCLKP
15	TxDATAN2	16	SDSCLKN
17	GND	18	GND
19	TxDATAP3	20	RxDATAN3
21	TxDATAN3	22	RxDATAP3
23	GND	24	GND
25	TxCLKN	26	RxDATAN2
27	TxCLKP	28	RxDATAP2
29	GND	30	GND
31	REFCLKP	32	RxDATAN1
33	REFCLKN	34	RxDATAP1
35	GND	36	GND
37	No connect	38	LLEB_L
39	No connect	40	DLEB_L
41	V_{CC}	42	RxDATAN0
43	No connect	44	RxDATAP0
45	No connect	46	V_{CC}
47	V_{CC}	48	V_{CC}
49	LASER_DISABLE	50	V_{CC}
51	TxLOCK	52	V_{CC}
53	Tx_FAULT	54	V_{CC}
55	Rx_LOS	56	RESET_L
57	Rx_LOSYNC	58	Rx_MON
59	Tx_BIASALM	60	SPARE
BLADE	GND		

Functional Signal Description

Signal Name	Level	I/O	Pin No.	Description
Transmit Functions				
TxDATAP0 TxDATAN0 TxDATAP1 TxDATAN1 TxDATAP2 TxDATAN2 TxDATAP3 TxDATAN3	LVDS	I	1 3 7 9 13 15 19 21	Transmit Parallel input data at 622.08 Mb/s, aligned to the TxCLKP/N parallel input clock. TxDATAP/N[3] is the most significant bit (MSB), and is the first bit transmitted in the outgoing OC-48 serial data stream. TxDATAP/N[3:0] is sampled on the rising edge of TxCLKP. DC coupled and internally terminated.
TxCLKP TxCLKN	LVDS	I	27 25	Transmit Parallel input clock, 622.08 MHz, to which TxDATAP/N[3:0] is aligned. TxCLK transfers the data on the TxDATAP/N inputs into a 4-bit wide latch in the Transceiver IC. Data is sampled on the rising edge of TxCLKP. DC coupled and internally terminated.
REFCLKP REFCLKN	LVPECL	I	31 33	155.52 MHz Transmit Reference Clock input to the bit clock frequency synthesizer of the Transceiver IC. DC coupled and internally biased.
No connect			37 39	Do not connect.
LASER_ DISABLE	LVTTL	I	49	Laser Disable. Control input to disable Transmit laser. High = Disable laser. Pulled low through 1 kΩ resistor.
TxLOCK	LVTTL	O	51	Loss Of Lock alarm for Tx PLL of the Transceiver IC. High = Locked. Asynchronous output.
No connect			45,43	Do not connect.
Tx_FAULT	LVTTL	O	53	Transmit Fault alarm output. Indicates that the laser has been automatically shut off due to a fault in the Tx laser circuit. High = Tx Fault. Fault may be cleared by cycling DC power, or by strobing the RESET_L input.
Tx_BIASALM	LVTTL	O	59	Transmit Bias Alarm output. Indicates that the bias current of the Tx laser is currently outside normal operating limits. High = Tx Bias outside limits.

Signal Name	Level	I/O	Pin No.	Description
PCLKP PCLKN	LVDS	O	10 8	622.08 MHz Parallel Clock output. Generated by dividing the internal high-speed Tx clock by 4.
RESET_L	LVTTL	I	56	Master Reset input. A Low level resets the Tx Mux and Laser Driver. RESET_L must be held low for at least 6 millisec. Pulled high through a 1 kΩ resistor.
Receive Functions				
RxDATAP0 RxDATAN0 RxDATAP1 RxDATAN1 RxDATAP2 RxDATAN2 RxDATAP3 RxDATAN3	LVDS	O	44 42 34 32 28 26 22 20	Parallel Output Data at 622.08 Mb/s from the Receiver, aligned to the Parallel Output Clock (RxCLKP/N). RxDATAP/N[3] is the Most Significant Bit, and is the first bit received in the incoming OC-48 serial data stream. RxDATAP/N[3:0] is clocked out on the falling edge of SDSCLKP. All data outputs are forced to zero level under Loss Of Signal or Loss Of Synchronization conditions. DC coupled outputs. Internally terminated.
SDSCLKN SDSCLKP	LVDS	O	16 14	Parallel Output Clock from the Receiver at 622.08 MHz. This clock is aligned to the RxDATAP/N[3:0] parallel output data. RxDATAP/N[3:0] is clocked out on the falling edge of SDSCLKP. Clock output is continuous under Loss Of Signal or Loss Of Synchronization conditions. DC coupled output. Internally terminated.
Rx_LOS	LVTTL	O	55	Receive Loss Of Signal alarm output. A High output level indicates Rx input power is below the sensitivity level of the receiver (high BER condition).
Rx_LOSYNC	LVTTL	O	57	Receive Loss Of Synchronization alarm output. A High output level indicates that the receive Clock Recovery unit has lost synchronization, due to either very low Rx input power level, or input data rate outside of frequency tolerance.
Rx_MON	Analog	O	58	Receive power monitor output. A voltage output which is directly proportional to the optical Rx input power.

Signal Name	Level	I/O	Pin No.	Description
Loopback Modes				
LLEB_L	LVTTL	I	38	Line Loopback Enable input. A Low level enables Line Loopback mode. When active, the Rx inputs to the Transceiver IC will be routed directly to the Tx outputs. Pulled high through a 1 kΩ resistor.
DLEB_L	LVTTL	I	40	Diagnostic Loopback Enable input. A Low level enables Diagnostic Loopback mode. When active, the Tx outputs of the Transceiver IC are routed directly to the Rx inputs. Pulled high through a 1 kΩ resistor.
RLPTIME	LVTTL	I	4	Reference Loop Time Enable input. A High level enables Reference Loop Time. When active, a divide-by-4 version of the POCLKP/N output of the Rx is used as the reference clock input to the Tx. Pulled low through a 1 kΩ resistor.
SLPTIME	LVTTL	I	2	Serial Loop Time Enable input. A High level enables Serial Loop Time. When active, the recovered high-speed clock (RSCLKP/N) from the Rx section is used in place of the synthesized transmit clock. Pulled low through a 1 kΩ resistor.
DC Power				
GROUND	0 V DC	I	5,6, 11,12, 17,18, 23,24, 29,30, 35,36, Blade	Ground connection for both signal and chassis ground on the transponder. The blade contact of the 60 pin interface connector is tied to ground in the transponder. Therefore, the blade of the user's mating connector should be connected to ground, as well.
V_{CC}	+3.3 V DC	I	41,47, 46,48, 50,52, 54	DC Power Input. +3.3 V DC, nominal.

Description

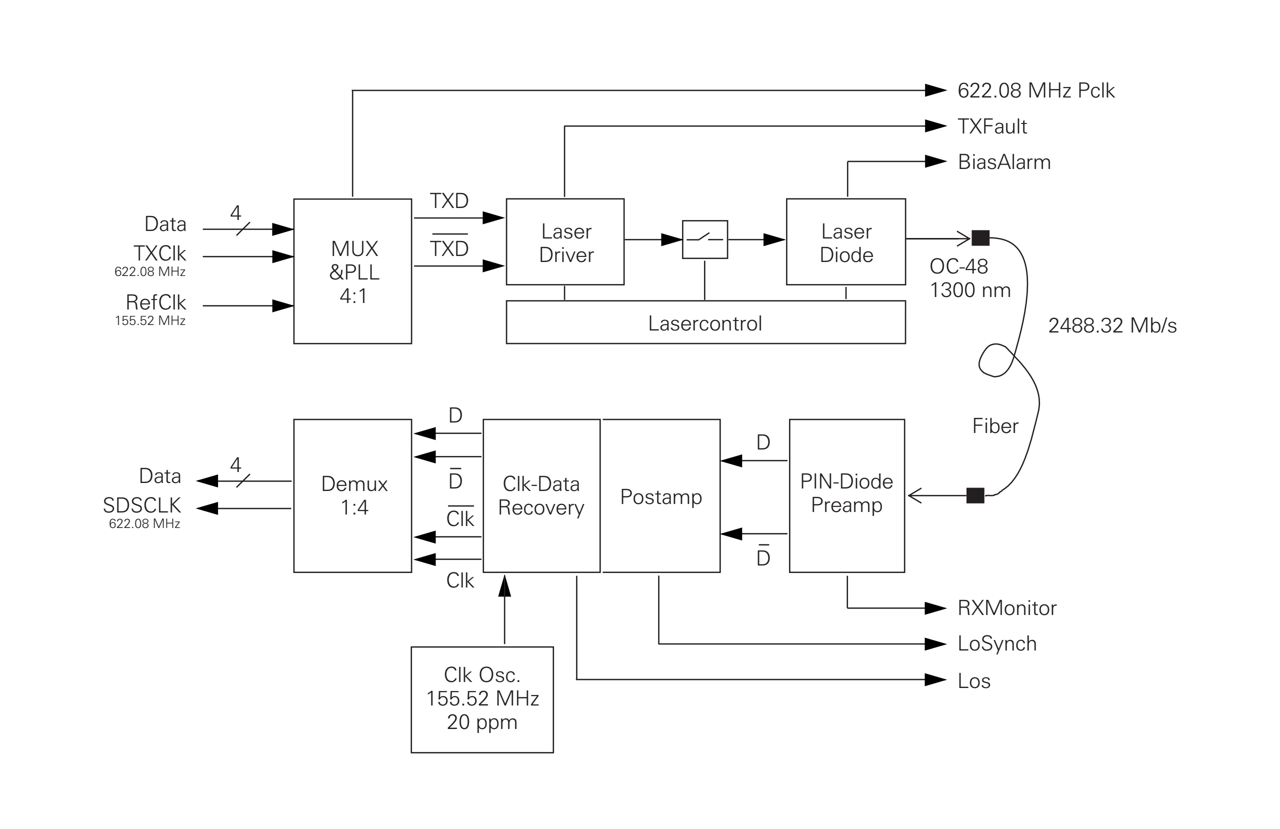


Figure 1 Block Diagram

The Infineon single mode SONET/SDH transponder is compliant with the Bellcore GR-253, ITU-T G.957, and ITU-T G.958 specifications. The transmitter section consists of a multiplexer (Mux), laser driver, Fabry Perot (FP) laser diode and pigtail single mode fiber with LC/PC or SC/PC 0° termination. The receiver section consists of a multimode fiber pigtail with LC/PC or SC/PC termination, a packaged PIN photodiode and preamplifier, postamplifier, clock and data recovery (CDR), and a demultiplexer (Demux). The Mux and Demux functions are integrated together onto a single Transceiver IC. The 622.08 MHz parallel data interface frees the user from the concerns of pcb layout at 2.5 Gb/s. The pluggable connector blind mates easily to the customer pcb, and allows the transponder to be removed prior to any solder reflow or washing of the users pcb.

The transponder operates from a single +3.3 V power supply. The electrical interface is via a 60 pin pluggable connector. The transmit and receive electrical signals each consist of 4 parallel differential LVDS data, and a differential LVDS clock. The transmit input data and clock lines, and the receive output data and clock lines, are all internally biased and terminated. All lines are DC coupled to the interface connector.

The transponder is designed to transmit and receive serial OC-48 (2488.32 Mb/s) data over standard non-dispersion-shifted single mode fiber at a wavelength of 1310 nm.

Transmitter (Mux Section)

Please refer to the transponder block diagram.

The transmitter accepts a 4 bit wide parallel input data word, TxDATAP/N[3:0], at a 622.08 Mb/s data rate. The Tx input clock, TxCLKP/N, is synchronous with the incoming data, at a frequency of 622.08 MHz. This clock is used to load the data into a 4-bit latch. The data is read in on the rising edge of the positive input clock (see **Figure 4 "Tx Input Timing Diagram" on Page 11**).

A reference input clock, REFCLKP/N, at 155.52 MHz, is supplied as a reference input to the high speed Clock Synthesizer. The high speed output of the clock synthesizer will clock the Timing Generator and the Parallel-to-Serial Converter. The Parallel-to-Serial Converter will output the retimed data as a serial bit stream, TSDP/N, at 2488.32 Mb/s data rate. Bit 3 of the TxDATAP/N parallel input word is the MSB, and is transmitted first in the data stream. Bit 0, the LSB, is transmitted last.

The output of the high speed Clock Synthesizer, which is internally set to 2488.32 MHz, is tapped off the Timing Generator, and is divided to 622.08 MHz. This output (PCLKP/N) is intended to be used as a reference clock for Tx upstream logic.

The Tx Clock Synthesizer section provides a lock alarm output signal, TxLOCK, which indicates if the clock synthesizer is properly phase locked.

Transmitter (Electro-Optical Section)

The serial data output, TSDP/N, of the Transceiver IC is input to a laser driver IC. The laser driver provides both bias and modulation to a laser diode. The laser bias current is controlled by a closed-loop circuit, which regulates the output average power of the laser over conditions of temperature and aging. The Monitor PIN diode, which is mechanically built into the laser, provides a feedback signal to the laser driver, and prevents the laser power from exceeding the factory preset operating limits.

The laser driver includes an eye safety feature that will automatically shut off power to the laser if a fault condition occurs which causes excessively high laser bias current or excessively high average output power. Such a fault will be indicated on the Tx_FAULT output. The fault can be cleared by cycling DC power, or by strobing the RESET_L input.

The Mux and Laser Driver can be reset with the RESET_L input. During the time that RESET_L is held active, there will be no optical output from the transmitter. The RESET_L input will clear any fault indication that has occurred on the Tx_FAULT output.

The laser can be switched off at any time with the LASER_DISABLE input.

The Tx_BIASALM output is provided as an alarm to indicate if the laser bias current is outside of the normal operating range. This output can be used to monitor the aging of the laser.

The laser diode is a Fabry-Perot type, which, due to the cavity nature of its design, will emit light at several longitudinal wavelengths, or modes centered about 1310 nm. This type of laser is suitable for the short reach transmission over single-mode fiber that this transponder is intended for. The laser has a single-mode fiber pigtail, which is terminated in an LC/PC or SC/PC 0° optical connector.

Receiver (Electro-Optical Section)

The input light to the Rx is coupled from the transmission fiber into a PIN/Preamp assembly on the transponder. The PIN/Preamp contains a multi-mode fiber pigtail, which is terminated in an LC/PC or SC/PC 0° optical connector. The multi-mode fiber pigtail has a larger core diameter (50 µm) than the single-mode transmission fiber (9 µm). Therefore, all the light from the single-mode fiber is coupled into the larger diameter core of the multi-mode pigtail.

The PIN/Preamp contains a PIN photodiode, trans-impedance amplifier and non-limiting post-amplifier in one package. The PIN diode produces a current output, which is directly proportional to the intensity of the incoming light. The trans-impedance amplifier performs current-to-voltage conversion, and the non-limiting post-amplifier quantizes the signal into a digital output.

The receiver contains a Rx power monitor output, which is a voltage output directly proportional to the average optical input power.

The Limiting Post-Amplifier provides additional voltage amplification, and also provides a Loss Of Signal (Rx_LOS) indicator. LOS will occur at a Rx input power level less than the specified Rx Sensitivity, and is an indication that the Rx is taking bit errors.

The Clock and Data Recovery (CDR) uses a PLL based approach to recover the high speed clock from the incoming serial data stream. A lock alarm, Rx_LOSYNC, indicates if the CDR has lost synchronization. This will occur if the input Rx power level is very low (below the LOS threshold level), or if the input data rate is outside the specified frequency tolerance. In these cases, the CDR will phase lock to a Crystal Oscillator so it can produce a valid clock output, with a frequency accuracy of ±20 ppm. In both cases of Loss Of Signal or Loss Of Synchronization, the Transceiver IC will force all the Rx output data bits, RxDATAP/N [3:0] to a constant zero state.

Receiver (Demux Section)

The incoming serial data is latched into the Transceiver IC by the recovered clock. The data and clock are applied to a 4 bit wide Serial-to-Parallel Converter (Demux), which demultiplexes the data into a parallel format. The first bit received, i.e. the MSB which is transmitted first in the serial data stream, is placed into the highest order bit of the parallel output word, i.e. Bit 3 = MSB. The Transceiver IC, however, does not perform a frame alignment function. This means that the parallel output word will contain the bits in the correct order, however, the position of the bits within the parallel output word may be shifted by an arbitrary amount between 0 and 4 bits. It is the function of downstream framer logic to realign the bits.

The retimed Rx output data, RxDATAP/N[3:0], is output at a 622.08 Mb/s data rate. The output clock, SDSCLKP/N, is at 622.08 MHz. The RxDATAP/N[3:0] data is clocked out on the falling edge of SDSCLKP (see **Figure 5 "Rx Output Timing Diagram" on Page 11**).

Loopback Operation

Four loopback modes of operation are provided.

Line Loopback is enabled with the LLEB_L input. In Line Loopback operation, the Rx Serial Data and Clock inputs to the Transceiver IC (RSDP/N and RSCLKP/N) are routed directly to the Tx Serial outputs of the IC (TSDP/N and TSCLKP/N). This effectively eliminates the Transceiver IC from the signal path.

Diagnostic Loopback is enabled with the DLEB_L input. In Diagnostic Loopback operation, the Tx output Serial Data and Clock of the Transceiver IC (TSDP/N and TSCLKP/N) are routed directly to the Rx Serial Data and Clock inputs of the IC (RSDP/N and RSCLKP/N). This effectively eliminates the optical and electro-optical components from the signal path.

Reference Loop Time is enabled with the RLPTIME input. In Reference Loop Time operation, a divide-by-4 version of the POCLKP/N output of the Rx is used as the reference clock input to the Tx.

Serial Loop Time is enabled with the SLPTIME input. In Serial Loop Time operation, the recovered high-speed clock (RSCLKP/N) from the Rx section is used in place of the synthesized transmit clock.

Jitter

The transponder is specified to meet the Sonet Jitter performance as outlined in ITU-T G.958 and Bellcore GR-253.

Jitter Generation is defined as the amount of jitter that is generated by the transponder. The Jitter Generation specifications are referenced to the optical OC-48 signals. If no or minimum jitter is applied to the electrical inputs of the transmitter, then Jitter Generation can simply be defined as the amount of jitter on the Tx Optical output. The Sonet specifications for Jitter Generation are 0.01 UI rms, maximum and 0.1 UI p-p, maximum. Both are measured with a 12 KHz-20 MHz filter in line. A UI is a Unit Interval, which is equivalent to one bit slot. At OC-48, the bit slot is 400 ps, so the Jitter Generation specification translates to 4 ps rms, max. and 40 ps p-p, max.

Jitter Tolerance is defined as the amount of jitter applied to the Rx Optical input that the receiver will tolerate while producing less than a 1 dB penalty in Rx Sensitivity. The minimum Jitter Tolerance levels are normally expressed as a mask of jitter amplitude versus jitter frequency. Measured Jitter Tolerance levels must be greater than the mask limits. The Jitter Tolerance mask specified in the Bellcore GR-253 document covers jitter frequencies down to 10 Hz. The transponder is designed to meet this mask.

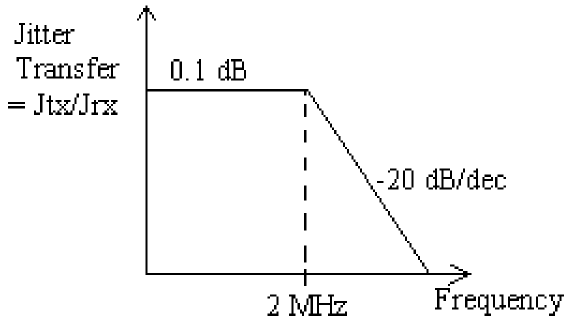


Figure 2 Sonet Jitter Transfer Mask (ITU-T G.958 & Bellcore GR-253)

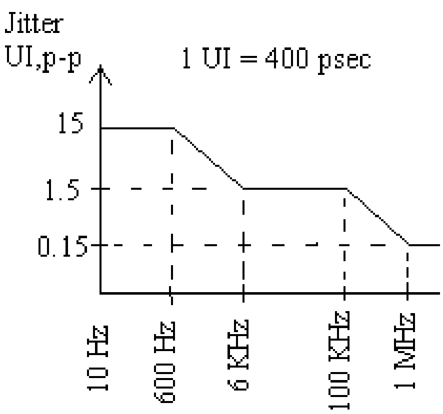


Figure 3 Sonet Jitter Tolerance Mask (Bellcore GR-253)

Jitter Transfer is defined as the ratio of output jitter to input jitter. Referenced to an optical transponder, it is defined as the ratio of Tx Optical Output Jitter to Rx Optical Input Jitter. To measure Jitter Transfer, the transponder must be operating in electrical loopback mode, with the Rx electrical outputs looped back into the Tx electrical inputs. Jitter Transfer is defined to be less than 0.1 dB up to 2 MHz, then dropping at –20 dB decade thereafter, per ITU-T G.958 and Bellcore GR-253. The Jitter Transfer must be less than the following mask limits.

Functional Diagrams

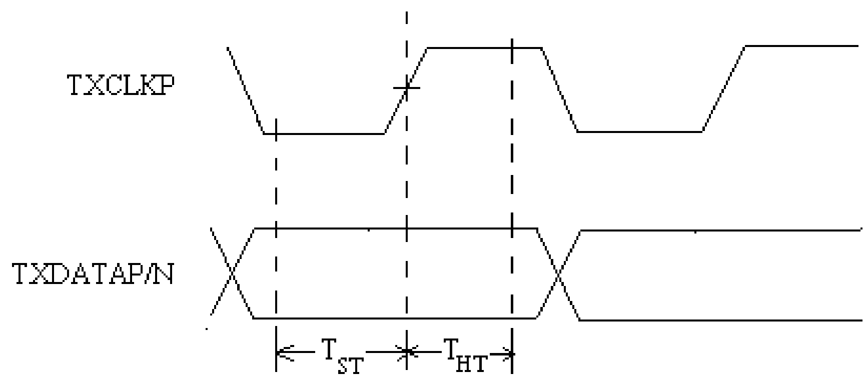


Figure 4 Tx Input Timing Diagram

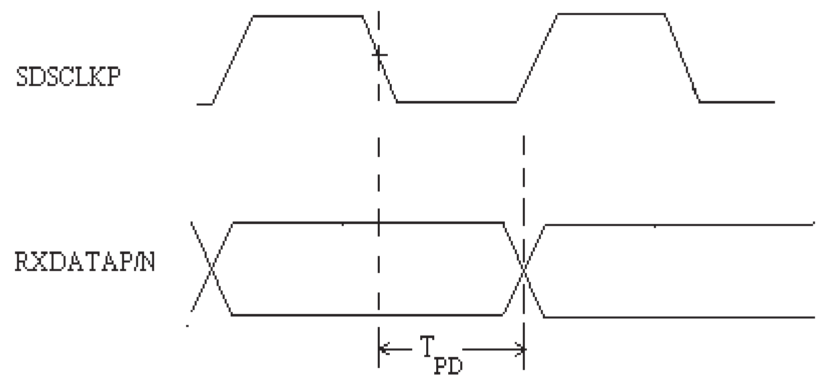


Figure 5 Rx Output Timing Diagram

Agency Certifications

Feature	Standard	Comments
Electrostatic Discharge (ESD) to the Electrical Pins	EIA/JESD22-A114-A (MIL-STD 883D Method 3015.7)	Class 1 (2000 V)
Immunity: Electrostatic Discharge (ESD) to Housing/Pigtails	EN 61000-4-2 IEC 61000-4-2	Discharges ranging from ±2 kV to ±15 kV on housing/pigtails cause no damage to transponder (under recommended conditions).
Immunity: Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 61000-4-3	With a field strength of 10 V/m rms, noise frequency ranges from 10 MHz to 2 GHz. No effect on transponder performance between the specification limits.
Emission: Electromagnetic Interference (EMI)	FCC Part 15, Class B EN 55022 Class B CISPR 22	Noise frequency range: 250 MHz to 18 GHz

Technical Data

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply Voltage	V_{CC}	0	3.6	V
LVDS Input Levels		0	V_{CC}	
LVPECL Input Level		0	V_{CC}	
LVTTL Input Level		0	5.5	
LVDS Output Source Current			5	mA
LVPECL Output Source Current			24	
LVTTL Output Source Current			1	
Operating Ambient Temperature		0	70	°C
Storage Ambient Temperature		-40	85	
Static Discharge Voltage, All Pins			1000	V

Operation beyond these ratings may cause permanent damage to the transponder.

Recommended Operating Conditions

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Operating Case Temperature[1]	T_C	0		70	°C
Transponder Total Power Consumption	P_{TOT}		2.8	3.46	W
3.3 V Supply Voltage	V_{CC}	3.13	3.3	3.46	V
3.3 V Supply Current	I_{CC}		0.85	1.0	A
Input Differential Noise, All Pins	N_{DIFF}			15	mV 0-p

[1] T_{CASE} is measured on top of the transponder (see details on **Page 28**, outline dimensions)

DC Electrical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
LVDS Input High Voltage	LVDS V_{IH}	1.2		2.9	V
LVDS Input Low Voltage	LVDS V_{IL}	0.6		2.8	
LVDS Input Voltage Differential	LVDS V_{INDIFF}	200		2600	mV
LVDS Input Single Ended Voltage	LVDS V_{INSING}	100		1300	
LVDS Differential Input Resistance	LVDS R_{DIFF}	80	100	120	Ω
LVDS Output High Voltage	LVDS V_{OH}	1.25		1.8	V
LVDS Output Low Voltage	LVDS V_{OL}	0.85		1.4	
LVDS Output Differential Voltage	LVDS $V_{OUTDIFF}$	440	740	1100	mV
LVDS Output Single Ended Voltage	LVDS $V_{OUTSINGLE}$	220	370	550	
LVPECL Input Low Voltage	LVPECL V_{IL}	V_{CC}–2.0		V_{CC}–1.5	V
LVPECL Input High Voltage	LVPECL V_{IH}	V_{CC}–1.15		V_{CC}–0.75	
LVPECL Input Single Ended Swing	LVPECL $V_{INSINGLE}$	200		1200	mV
LVPECL Input Differential Swing	LVPECL V_{INDIFF}	400		2400	
LVTTL Input High Voltage	LVTTL V_{IH}	2.0		V_{CC}	V
LVTTL Input Low Voltage	LVTTL V_{IL}	0		0.8	
LVTTL Input High Current	LVTTL I_{IH}			50	µA
LVTTL Output Current	LVTTL I_O	–500			
LVTTL Output High Voltage	LVTTL V_{OH}	2.4			V
LVTTL Output Low Voltage	LVTTL V_{OL}			0.8	

AC Electrical Characteristics

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Transmitter						
TxDATAP/N[3:0] Input Bit Rate			622.08		Mb/s	
TxCLKP/N Input Frequency			622.08		MHz	
TxCLKP/N Input Duty Cycle		40		60	%	
TxCLKP/N Input Rise/Fall Time		100		300	ps	20-80%
TxDATA Setup Time with respect to the Rising edge of TxCLKP	T_{ST}	200				See **Figure 4 "Tx Input Timing Diagram" on Page 11**
TxDATA Hold Time with respect to the Rising edge of TxCLKP	T_{HT}	200				
REFCLKP/N Input Frequency			155.52		MHz	
REFCLKP/N Input Frequency Tolerance [1]				±20	ppm	
REFCLKP/N Input Duty Cycle		45		55	%	
REFCLKP/N Input Rise/Fall Time				1.5	ns	10-90%
REFCLKP/N Input Jitter [2]				1	ps, rms	
PHASE_INITP/N Input Min. Pulse Width		3.2			ns	
PCLKP/N Output Frequency			622.08		MHz	
PCLKP/N Output Duty Cycle		45		55	%	
Return Loss, All AC Inputs & Outputs		15			dB	10 MHz - 1 GHz
RESET_L Input Min. Pulse Width		30			ms	

AC Electrical Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Receiver						
RxDATAP/N[3:0] Output Bit Rate			622.08		Mb/s	
SDSCLKP/N Output Frequency			622.08		MHz	
SDSCLKP/N Output Duty Cycle		45		55	%	
SDSCLKP/N Output Rise/ Fall Time		100		300	ps	20-80%
RxDATA Propogation Delay with respect to the Falling edge of SDSCLKP	T_{PD}			600		See **Figure 5 "Rx Output Timing Diagram" on Page 11**
Return Loss, all AC Inputs & Outputs		15			dB	10 MHz - 1 GHz
SDSCLKP/N Output Frequency Accuracy during LOS or LOSYNC[3]				±20	ppm	Over operating Temp Range

[1] The REFCLK input must be connected and not left open-circuit.
[2] Maximum allowable jitter on the reference clock input (REFCLKP/N) such that the transmitter will meet ITU-T G.958 and Bellcore GR-253 Jitter Generation requirements. Measured with a 12 KHz - 20 MHz filter.
[3] T_{CASE} is measured on top of the transponder (see details on **Page 28**, outline dimensions)

Transmitter Electro-Optical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Nominal Center Wavelength	Tx λ_{NOM}	1310			nm
Range Of Center Wavelengths	Tx λ_{MIN}-λ_{MAX}	1260		1360	
Spectral Bandwidth	Tx $\Delta\lambda_{RMS}$			5	nm, rms
Average Output Power[1)]	Tx P_{AVG}	–10	–4	–3	dBm
Extinction Ratio	Tx ER	8.2	14		dB
Output Rise Time 20%-80%	Tx T_R		100	200	ps
Output Fall Time 80%-20%	Tx T_F		175	250	
Eye Diagram[2)]	Tx ED				
Tx Jitter Generation, rms[3)]	Tx $J_{GEN\ rms}$		0.007	0.01	UI rms
Tx Jitter Generation, p-p[3)]	Tx $J_{GEN\ p\text{-}p}$		0.075	0.1	UI p-p
Reset Threshold for V_{CC}[4)]	Tx V_{TH}	2.2		2.95	V
Power On Delay for V_{CC}[4)]	Tx T_{POD}	8	11	14	ms
Fault Delay[5)]	Tx T_{FAULT}	15	22	29	
Tx Bias Monitor switching threshold	Tx I_{BIAS}			60	mA

1) The laser driver contains a control circuit, which regulates the average optical output power. Nominal output power is factory set to be within the specified range.

2) The Eye Diagram is compliant with Bellcore GR-253 and ITU-T G.957 Eye Mask specifications.

3) Jitter Generation is defined as the amount of jitter on the Tx Optical Output, when there is no or minimum jitter on the Tx electrical inputs. Jitter Generation is compliant with GR-253 and ITU-T G.958 specifications, when measured using a 12 KHz - 20 MHz filter, and with a jitter level on the REFCLKP/N input which is less than the level specified in ”AC Electrical Characteristics - Transmitter”.

4) If the +3.3 V power supply drops below the specified level, the laser bias and modulation currents will be held disabled until the supply voltage rises above threshold and after the Power On Delay Time period.

5) A fault, such as high laser bias current or high average power, which lasts longer than the specified Fault Delay time, will cause the transmitter to be disabled. The fault can be cleared by cycling of DC power, or by strobing the RESET_L input.

Receiver Electro-Optical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Nominal Center Wavelength	Rx λ_{NOM}		1310		nm
Sensitivity (Average Power)[1]	Rx P_{SENS}		–25	–18	dBm
Overload (Average Power)[1]	Rx P_{OL}	–3			
Optical Return Loss	Rx RL	27			dB
Rx Jitter Tolerance[2]	Rx J_{TOL}				
Rx-to-Tx Jitter Transfer[3]	Rx-Tx J_{XFR}				
Optical Path Penalty	Rx P_{PEN}			1.0	dB
Clock Recovery Capture Frequency Range[4]	Rx F_{CAPT}		±200		ppm
Clock Recovery Acquisition Lock Time	Rx T_{LOCK}		32	250	µs
Rx_LOS Output Assert relative To Rx Optical Input Power[5]	Rx_ LOS_{ASSERT}	–30		–25	dBm
Rx_LOSYNC Output Assert relative to Rx input frequency[4]	Rx_ $LOSYNC_{ASSERT}$	±450	±600	±770	ppm
Rx_LOS Output Hysteresis[5]	Rx_ LOS_{HYST}			3	dB
Rx_LOS & Rx_LOSYNC Output Assert Time[4), 5]	Rx T_{ASSERT}		100		µs
Rx_LOS & Rx_LOSYNC Output Deassert Time[4), 5]	Rx $T_{DEASSERT}$		100		
Rx_MON Transfer Slope[6]			4.4		mV/µW

Receiver Electro-Optical Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Rx_MON Dark Offset Voltage[6]			53		mV
Rx_MON Output Voltage at P_{IN} = –17 dBm[6]			142		
Rx_MON Output Voltage at P_{IN} = –7 dBm[6]			900		

1) Average Rx power for a 1×10^{-10} BER, and using a PRBS pattern of $2^{23}-1$ length with 72 zeros and 72 ones inserted, as per ITU-T G.958.

2) Jitter Tolerance is defined as the amount of jitter applied to the Rx optical input that the receiver will tolerate without producing bit errors. The minimum required Jitter Tolerance for a 1 dB power penalty is defined to be 15 UI from 10 Hz to 600 Hz, 1.5 UI from 6 KHz to 100 KHz, and 0.15 UI from 1 MHz onwards, per Bellcore GR-253.

3) Jitter Transfer is defined as the ratio of Tx Output Jitter to Rx Input Jitter, when the transponder is operated in electrical loopback mode (Rx electrical outputs looped back into Tx electrical inputs). Jitter Transfer is specified to be less than 0.1 dB up to 2 MHz, and dropping at –20 dB/Decade after that point, per ITU-T G.958 and Bellcore GR-253.

4) The receiver lock range is typically ±300 ppm from nominal OC-48 data rate. When the data rate of the Rx signal deviates by more than ±600 ppm (typically) from nominal, or if the Rx is in a Loss Of Signal (LOS) condition, then the Clock Recovery module will lock to an internal 155.52 MHz crystal oscillator. Under this condition: The appropriate fault output (Rx_LOS or Rx_LOSYNC) switches active; The RxDATAP/N[3:0] output data is forced to all zeros; and, the switching of the SDSCLKP/N output is done so that the clock is continuous, and there are no violations of the minimum pulse width and period.

5) The Rx_LOS output is an active high LVTTL output, which is set HIGH if there is a loss of Rx optical signal input (LOS), A decrease in optical input power below the assert level will cause the Rx_LOS output to switch HIGH (ON). Hysteresis occurs when the optical input power is raised back above the threshold switching level. The Rx_LOSYNC output is an active high LVTTL output, which is set HIGH if the Clock Data Recovery PLL becomes unlocked. Loss Of Sync will occur at a lower optical input power level than LOS, but still within the specified input power range.

6) Rx_MON output voltage is measured between V_{CC} (+) and Rx_MON (–). Rx_MON is specified up to a maximum optical input average power of –5 dBm (316.2 µW).

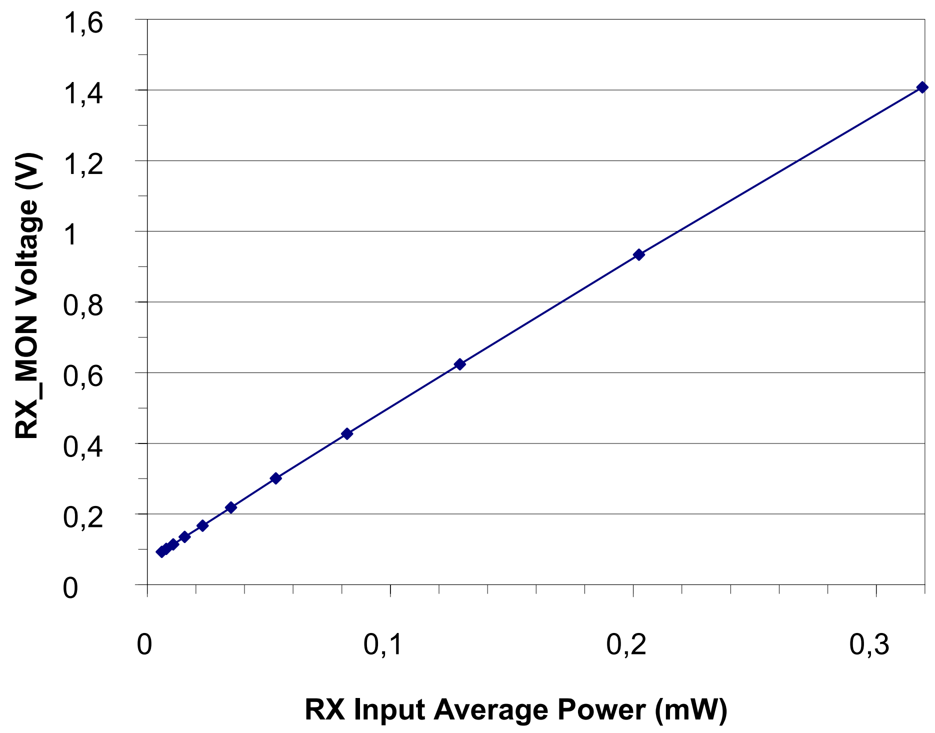


Figure 6 Typical Rx_MON Characteristic (Linear)

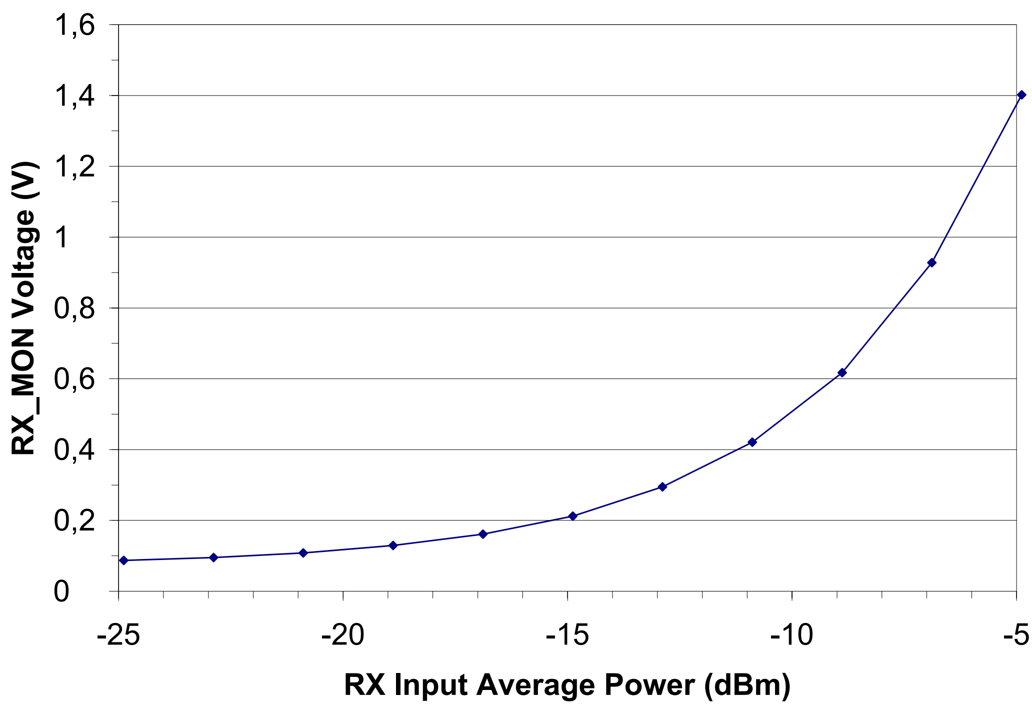


Figure 7 Typical Rx_MON Characteristic (Logarithmic)

Eye Safety

This laser based single mode transponder is a Class 1 product. It complies with IEC 60825-1 and FDA 21 CFR 1040.10 and 1040.11.

The transponder has been certified with FDA under accession number 9911449-03.

To meet laser safety requirements the transponder shall be operated within the Absolute Maximum Ratings.

Attention: All adjustments have been made at the factory prior to shipment of the devices. No maintenance or alteration to the device is required. Tampering with or modifying the performance of the device will result in voided product warranty.

Note: Failure to adhere to the above restrictions could result in a modification that is considered an act of "manufacturing", and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration (ref. 21 CFR 1040.10 (i)).

Laser Data

Wavelength	1310 nm
Total output power (as defined by IEC: 7 mm aperture at 14 mm distance)	2 mW
Total output power (as defined by FDA: 7 mm aperture at 20 cm distance)	180 µW
Beam divergence	5°

FDA

Complies with 21 CFR 1040.10 and 1040.11

IEC

Class 1 Laser Product

Figure 8 Required Labels

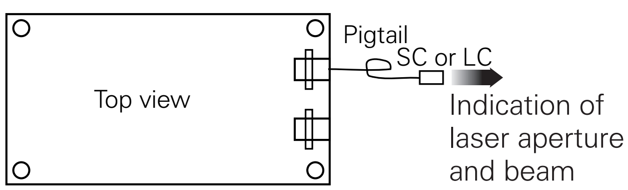


Figure 9 Laser Emission

Application Notes

Interfacing the 4-Line Transponder

Scope

This Application Note is meant to define the interfacing between the Infineon 4-Line OC-48 Transponder, and the customer equipment.

Introduction

The signals which interface to the OC-48 Transponder can be grouped into Transmit (Tx) and Receive (Rx) functions.

The Tx signals are:

- TxDATAP/N[0..3]: 4 differential LVDS inputs for Tx Data.
- TxCLKP/N: A differential LVDS input for Tx Clock.
- REFCLKP/N: A differential LVPECL input for Tx Reference Clock.
- PCLKP/N: A differential LVDS output which is a divide-by-4 version of the Tx high speed clock.

The Rx signals are:

- RxDATAP/N[0..3]: 4 differential LVDS outputs for Rx Data.
- SDSCLKP/N: A differential LVDS output for Rx Clock.

Interfacing

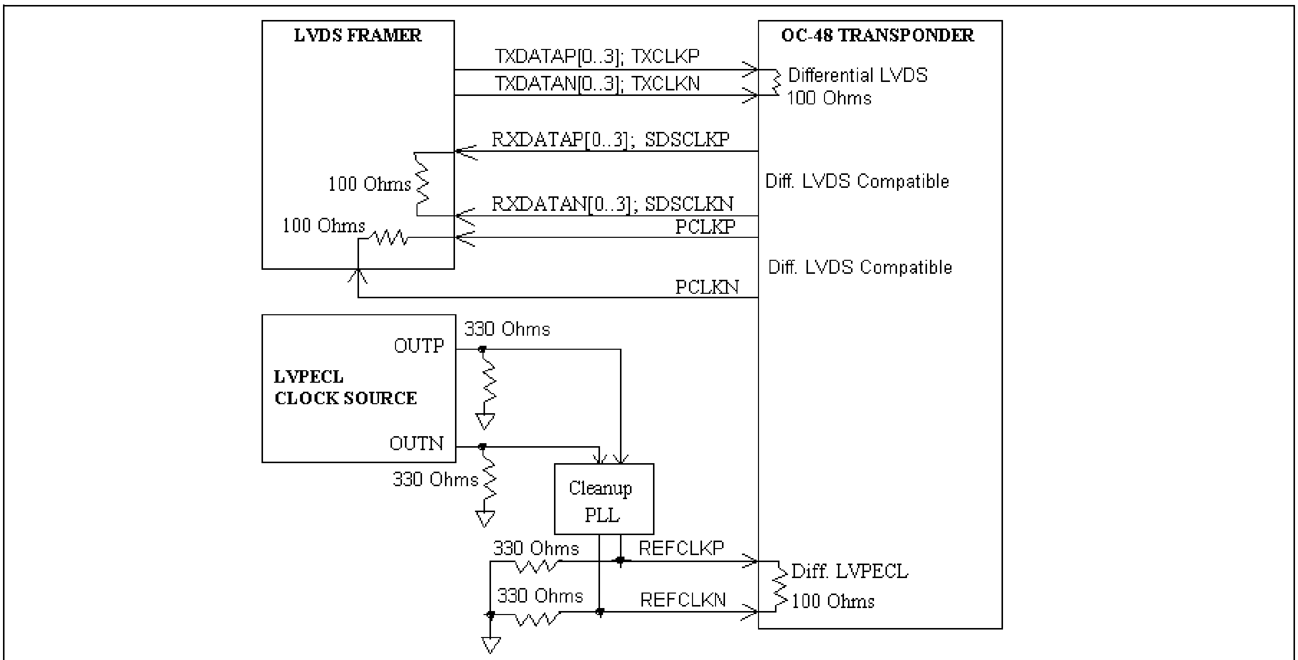


Figure 10 Interfacing Diagram

Tx Signals

The customer OC-48 framer drives the TxDATA and TxCLK inputs. In order to use DC Coupling, the framer should be a +3.3 V LVDS device. Each of the inputs is terminated with 100 Ω differential between lines in the transponder.

The REFCLK input is a LVPECL input, which is driven by the customer Clock Source, which should be an LVPECL device. DC coupling is acceptable if the clock source is a +3.3 V LVPECL. The REFCLK input is terminated with 100 Ω differential between lines in the transponder. It is necessary for the customer to provide the external 330 Ω resistors to ground for the source termination.

Rx Signals

The customer framer accepts as input the RxDATA and SDSCLK outputs of the transponder. In order to use DC Coupling, the framer should be a +3.3 V LVDS device. The RxDATA and SDSCLK outputs of the transponder are not true LVDS, but are LVDS level compatible, which use a 330 Ω to ground termination in the transponder. If the framer does not have a 100 Ω differential termination between lines, then the customer will have to supply the terminations on their board.

Line Impedance

For proper impedance matching, all LVDS traces should be constructed as a differential trace pair, with 100 Ω characteristic impedance between the lines of each pair, and 50 Ω characteristic impedance per line. The LVPECL traces should be constructed as 50 Ω per line.

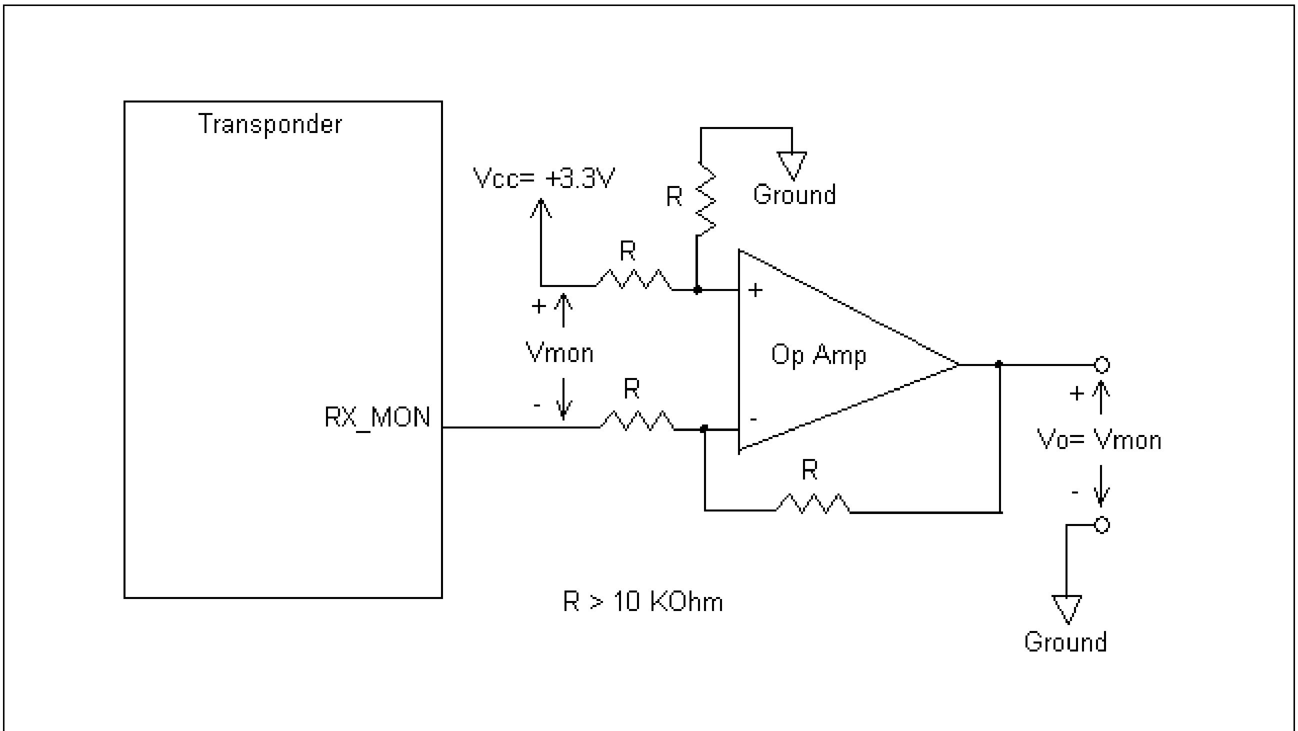


Figure 11 Conversion of Rx_MON Output to a Voltage with Respect to Ground

Mechanical

Size

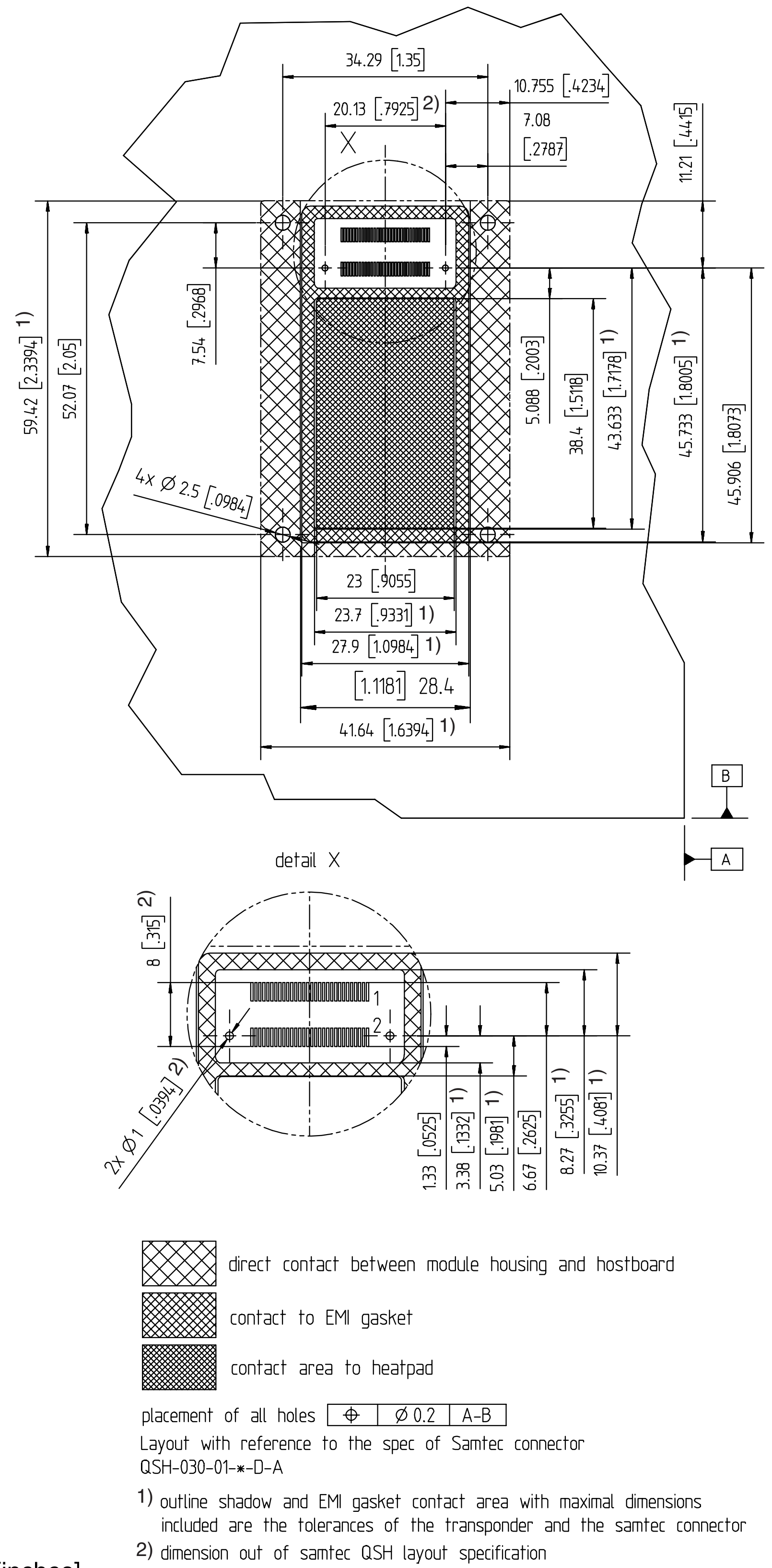
The outline size for the transponder housing is 2.3 in x1.6 in x0.54 inches. Please refer to the outline drawing.

Fiber & Connectors

The transponder has fiber pigtails for both Tx and Rx. The Tx pigtail is Single Mode Fiber, 9 µm/125 µm. The Rx pigtail is Multi Mode Fiber, 50 µm/125 µm, allowing a highly tolerant coupling with a Single Mode Fiber. Each pigtail is terminated with a LC/PC or SC/PC optical connector with 0° polish. The minimum bend radius of the fiber pigtails is 30 mm (1.18 inches), typical. The fiber length see table on **Page 1**, as measured from the transponder housing to the tip of the connector.

Interface Connector

The transponder interface connector is a 60 pin SMT, dual row, header, 0.5 mm pitch, with ground blade, Samtec part number QTH-030-01-L-D-A. The appropriate mating connector for the customer pcb is a 60 pin SMT, dual row, socket, 0.5 mm pitch, with mating alignment pins, Samtec part number QSH-030-01-L-D-A. The internal blade of the connector should be connected to signal ground on the user’s pcb. Contact Samtec for recommended pcb layout pattern for QSH connector.



Dimensions in mm [inches]

Figure 12 Hostboard Contact Area

For detailed connector layout information, check http://www.samtec.com, and go to “QSH” connector.

For the guaranteed EMI-performance an optimal electrical contact between the transponder housing and the user's pcb signal ground is necessary. For the user's pcb (hostboard) we recommend a full signal ground plane underneath the entire transponder housing (including the standoff area, the EMI gasket area and the optional heatsink area).

The transponder is equipped with an attached EMI gasket. According to the drawing “Hostboard Contact Area” the contact surface of the entire EMI gasket should be connected to signal ground on the user's pcb. The area under the EMI gaskets (EMI gasket area) should be gold flash or tin plated copper with no solder mask or other nonconductive coatings.

The four mounting screws of the housing also must be connected to signal ground on the user's pcb. Therefore the mounting screw areas should have square pads of gold flash or tin plated copper, that are connected to signal ground. These pads are located on the pcb opposite side to the transponder. Use a torque wrench to tighten the mounting screws. The recommended torque value is
10 ±2 Ncm = 0.1 ±0.02 Nm = 14.16 ±2.83 oz-in. With a higher or lower value,
the EMI-performance will deteriorate.

The heatsink area under the center of the transponder is optional and could be used for critical ambient temperature or critical airflow. Currently it is not a complete replacement for the regular heatsink. The contact area should be connected to signal ground. Gold (Au), Tin or other metal platings are recommended for good heat transfer. Any polymer coating will decrease the heatsinking performance. Special heat transfer pads are in progress. For reliable heatsinking to the hostboard, the max. hostboard temperature must be lower or equal to the specified ambient air temperature.

Scheme of tightening mounting screws

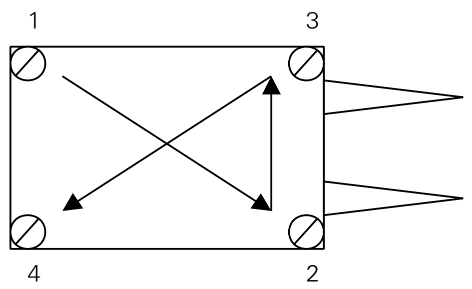
It is recommended to use a torque wrench to tighten the mounting screws. Tightening torque value is:
10 ±2 Ncm = 0.1 ±0.02 Nm = 14.16 ±2.83 oz-in.
With a higher or lower value, the EMI-performance will deteriorate.

In order to avoid a mechanical stress of the users PCB and to reduce the impacting forces (twisting or wresting of the PCB) we recommend a crosswise tightening of the 4 mounting screws.

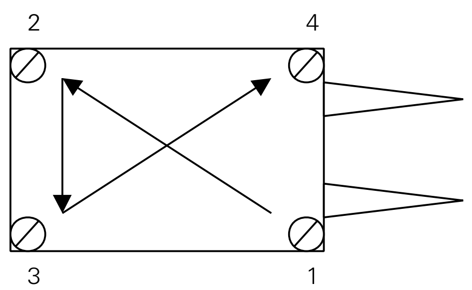
Scheme

Please tighten the screws according to the following scheme:

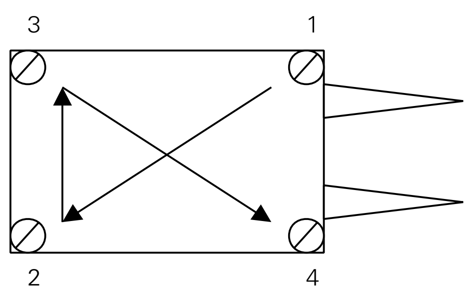
1. Insert four screws and tighten them very loose in the following order:



2. Tighten the four screws hand-screwed in the following order:

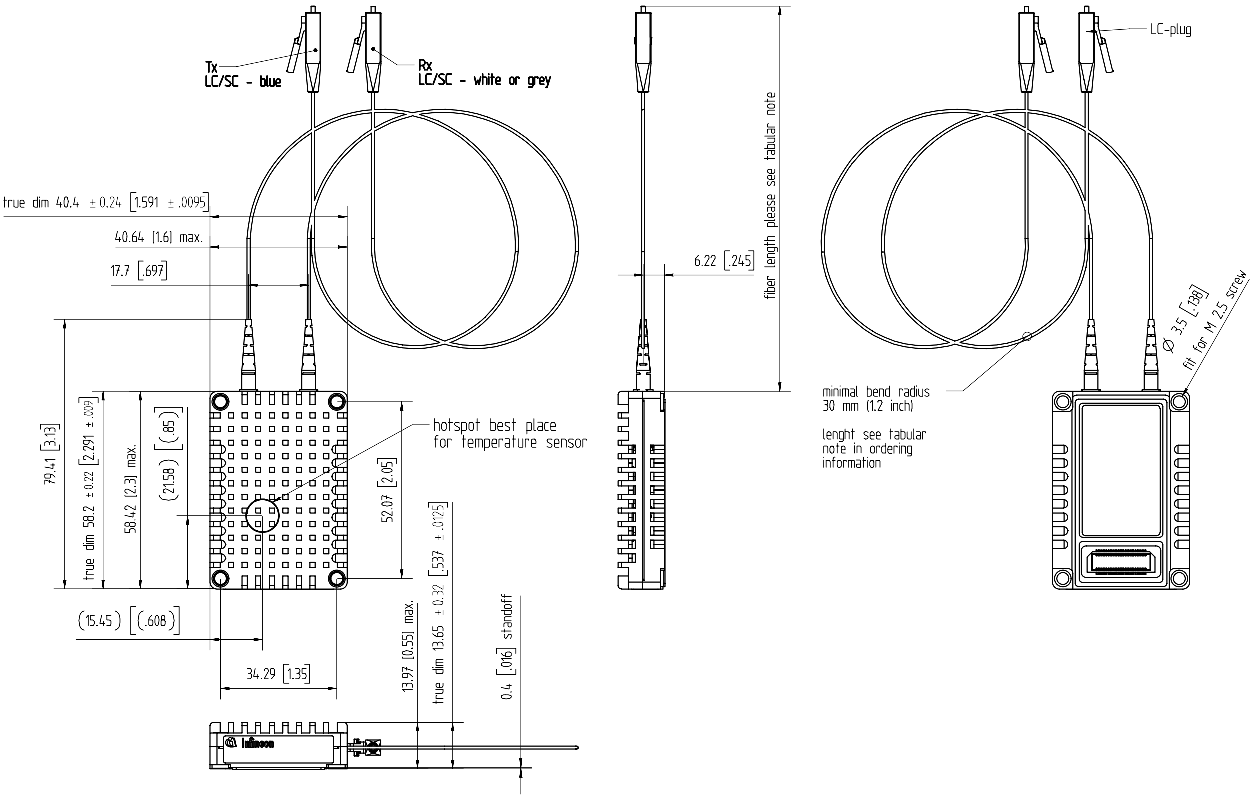


3. Tighten the four screws with a torque wrench
   10 ±2 Ncm = 0.1 ±0.02 Nm
   14.16 ±2.83 oz-in in the following order:



Package Outlines

V23816-N1018-L312-A



Dimensions in mm [inches]

Figure 13

V23816-N1018-C312-A
V23816-N1018-L312-A

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Previous Version:

Page	**Subjects (major changes since last revision)**
	Document's layout has been changed: 2002-Aug.

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