DUAL 10-Ω SPDT ANALOG SWITCH

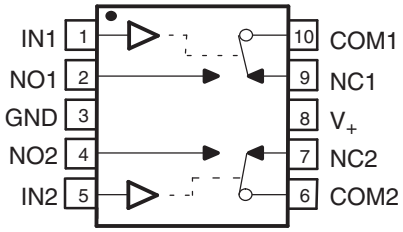
FEATURES

- Specified Break-Before-Make Switching
- Low ON-State Resistance (10 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion
- 1.8-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

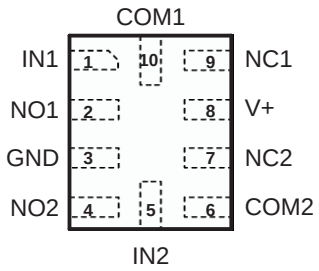
APPLICATIONS

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

DGS PACKAGE
(TOP VIEW)



RSE PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS5A23157 is a dual single-pole double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to 5.5 V (peak) can be transmitted in either direction.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	VSSOP (MSOP-10) – DGS	Tape and reel	TS5A23157DGSR	JBR
	QFN – RSE	Tape and reel	TS5A23157RSER	JB_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) RSE: The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

SUMMARY OF CHARACTERISTICS

Configuration	2:1 Multiplexer/Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance (r_{on})	10 Ω
ON-state resistance match between channels (Δr_{on})	0.15 Ω
ON-state resistance flatness ($r_{on(flat)}$)	4 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	5.7 ns/3.8 ns
Break-before-make time (t_{BBM})	0.5 ns
Charge injection (Q_C)	7 pC
Bandwidth (BW)	220 MHz
OFF isolation (OSIO)	–65 dB at 10 MHz
Crosstalk 9XTALK)	–66 dB at 10 MHz
Total harmo nic distortion (THD)	0.01%
Leakage current ($I_{COM(OFF)}/I_{NC(OFF)}$)	±1 µA
Package options	10-pin DGS and RSE

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(2)		–0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage range(2)(3)(4)		–0.5	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NC}, V_{NO}, V_{COM} > V_+		±50	mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+		±50	mA
V_{IN}	Digital input voltage range(2)(3)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_{IN} < 0		–50	mA
	Continuous current through V_+ or GND			±100	mA
θ_{JA}	Package thermal impedance(5)	DGS package		56.5	°C/W
		RSE package		243	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –30 mA,	Switch ON, See Figure 10	Full	4.5 V			10	Ω
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 3.15 V, I_{COM} = –30 mA,	Switch ON, See Figure 10	25°C	4.5 V		0.15		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –30 mA,	Switch ON, See Figure 10	25°C	4.5 V		4		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, See Figure 11	25°C	5.5 V	–1	0.05	1	µA
				Full		–1		1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See Figure 11	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 11	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
Digital Inputs (IN12, IN2)(2)									
Input logic high	V_{IH}			Full		V_+ × 0.7			V
Input logic low	V_{IL}			Full				V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	5.5 V	–1	0.05	1	µA
				Full		–1		1	

(1) T_A = 25°C
(2) All unused digital inputs of the device must be held at V+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See Figure 13	Full	4.5 V to 5.5 V	1.7		5.7	ns
Turn-off time	t_{OFF}	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See Figure 13	Full	4.5 V to 5.5 V	0.8		3.8	ns
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	Full	4.5 V to 5.5 V	0.5			ns
Charge injection	Q_C	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	See Figure 18	25°C	5 V		7		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND,	Switch OFF, See Figure 12	25°C	5 V		5.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND,	Switch ON, See Figure 12	25°C	5 V		17.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND,	Switch ON, See Figure 12	25°C	5 V		17.5		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See Figure 12	25°C	5 V		2.8		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 15	25°C	4.5 V		220		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 16	25°C	4.5 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 17	25°C	4.5 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 19	25°C	4.5 V		0.01		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	5.5 V			1	µA
				Full				10	
Change in supply current	ΔI_+	V_{IN} = V_+ – 0.6 V		Full	5.5 V			500	µA

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 10	Full	3 V			18	Ω
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.1 V, I_{COM} = –24 mA,	Switch ON, See Figure 10	25°C	3 V		0.2		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 12	25°C	3 V		9		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, See Figure 11	25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See Figure 11	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 11	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
Digital Inputs (IN12, IN2)(2)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$			V
Input logic low	V_{IL}			Full				$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
Dynamic									
Turn-on time	t_{ON}	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See Figure 13	Full	3 V to 3.6 V	2.5		7.6	ns
Turn-off time	t_{OFF}	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See Figure 13	Full	3 V to 3.6 V	1.5		5.3	ns
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	Full	3 V to 3.6 V	0.5			ns
Charge injection	Q_C	R_L = 50 Ω, CL = 0.1 nF,	See Figure 18	25°C	3.3 V		3		pC
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 15	25°C	3 V		220		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 16	25°C	3 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 17	25°C	3 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 19	25°C	3 V		0.015		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	3.6 V			1	µA
				Full				10	
Change in supply current	ΔI_+	V_{IN} = V_+ – 0.6 V		Full	3.6 V			500	µA

(1) T_A = 25°C
(2) All unused digital inputs of the device must be held at V+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 10	Full	2.3 V			45	Ω
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.6 V, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V		0.5		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V		27		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, See Figure 11	25°C	2.7 V	–1	0.05	1	µA
				Full		–1		1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See Figure 11	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 11	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
Digital Inputs (IN12, IN2)(2)									
Input logic high	V_{IH}			Full		V_+ × 0.7			V
Input logic low	V_{IL}			Full				V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	2.7 V	–1	0.05	1	µA
				Full		–1		1	
Dynamic									
Turn-on time	t_{ON}	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See Figure 13	Full	2.3 V to 2.7 V	3.5		14	ns
Turn-off time	t_{OFF}	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See Figure 13	Full	2.3 V to 2.7 V	2		7.5	ns
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	Full	2.3 V to 2.7 V	0.5			ns
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 15	25°C	2.3 V		220		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 16	25°C	2.3 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 17	25°C	2.3 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 19	25°C	2.3 V		0.025		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	2.7 V			1	µA
				Full				10	
Change in supply current	ΔI_+	V_{IN} = V_+ – 0.6 V		Full	2.7 V			500	µA

(1) T_A = 25°C
(2) All unused digital inputs of the device must be held at V+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –4 mA,	Switch ON, See Figure 10	Full	1.65 V			140	Ω
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.15 V, I_{COM} = –4 mA,	Switch ON, See Figure 10	25°C	1.65 V		1		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –4 mA,	Switch ON, See Figure 10	25°C	1.65 V		110		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = 0 to V_+,	Switch OFF, See Figure 11	25°C	1.95 V	–1	0.05	1	µA
				Full		–1		1	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See Figure 11	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 11	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
Digital Inputs (IN12, IN2)(2)									
Input logic high	V_{IH}			Full		V_+ × 0.75			V
Input logic low	V_{IL}			Full				V_+ × 0.25	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	1.95 V	–1	0.05	1	µA
				Full		–1		1	
Dynamic									
Turn-on time	t_{ON}	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See Figure 13	Full	1.65 V to 1.95 V	7		24	ns
Turn-off time	t_{OFF}	V_{NC} = GND and V_{NO} = V_+ or V_{NC} = V_+ and V_{NO} = GND,	R_L = 500 Ω, C_L = 50 pF, See Figure 13	Full	1.65 V to 1.95 V	3		13	ns
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 14	Full	1.65 V to 1.95 V	0.5			ns
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 15	25°C	1.8 V		220		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 16	25°C	1.8 V		–60		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 17	25°C	1.8 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 19	25°C	1.8 V		0.015		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	1.95 V			1	µA
				Full				10	
Change in supply current	ΔI_+	V_{IN} = V_+ – 0.6 V		Full	1.95 V			500	µA

(1) T_A = 25°C
(2) All unused digital inputs of the device must be held at V+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TYPICAL CHARACTERISTICS

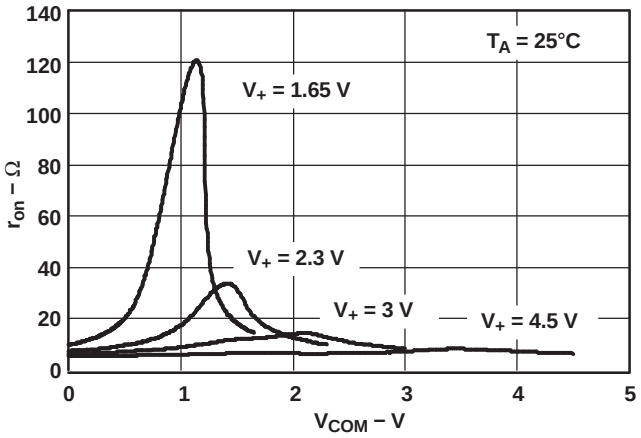


Figure 1. r_{on} vs V_{COM}

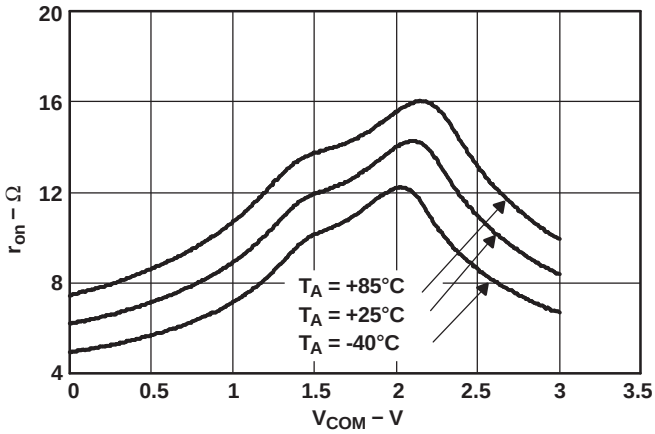


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

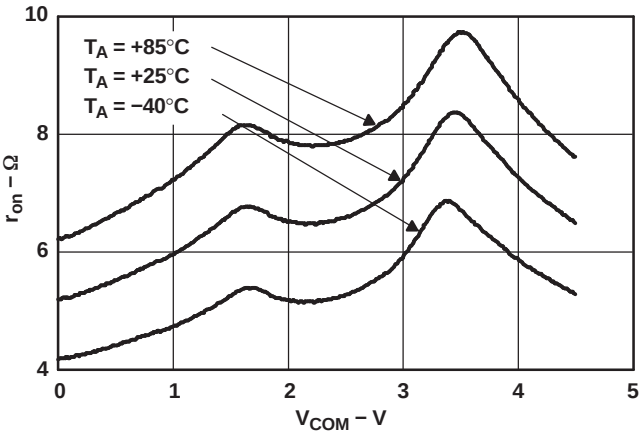


Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)

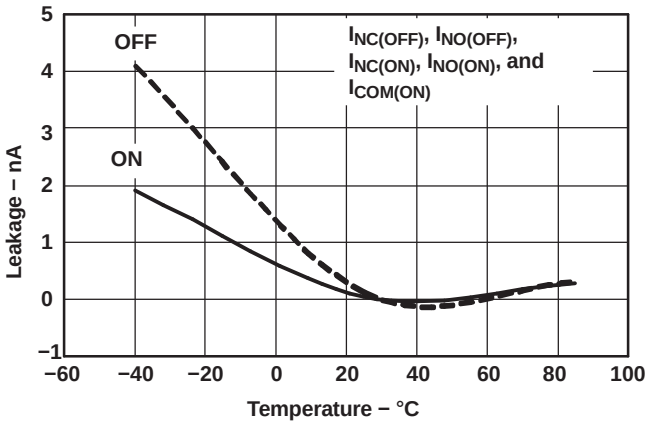


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

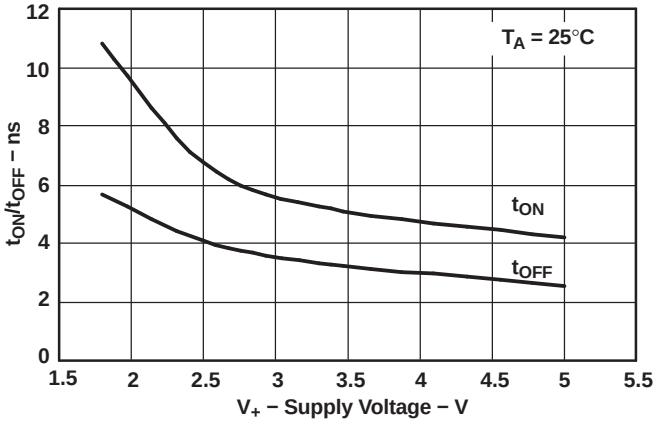


Figure 5. t_{ON} and t_{OFF} vs V_+

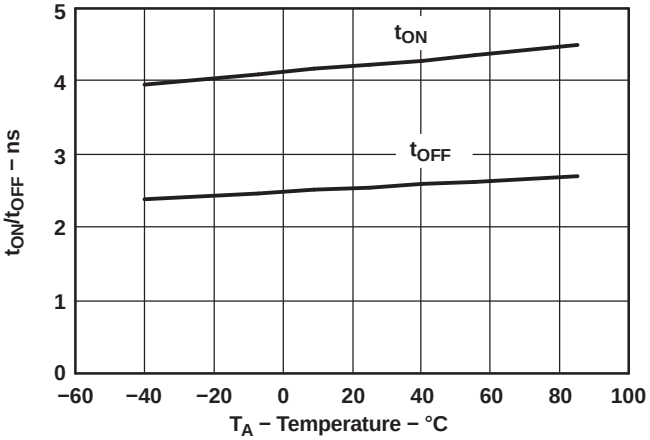


Figure 6. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

TYPICAL CHARACTERISTICS (continued)

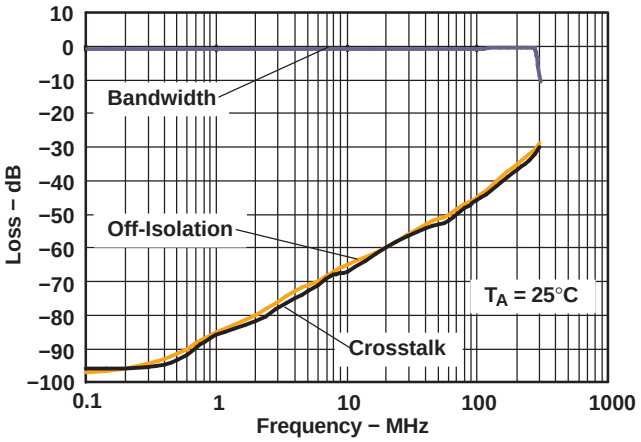


Figure 7. Frequency Response (V_+ = 3 V)

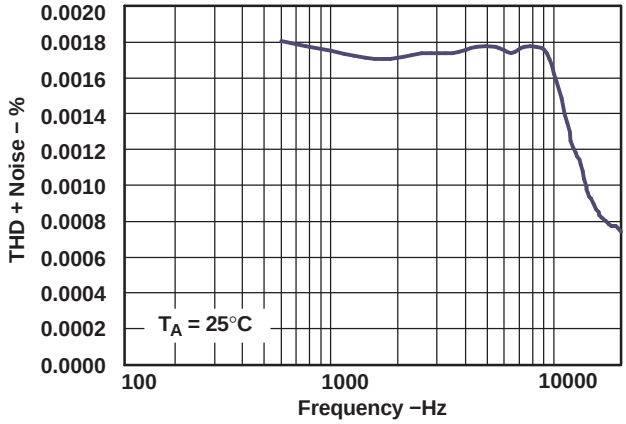


Figure 8. Total Harmonic Distortion (THD) vs Frequency (V_+ = 3 V)

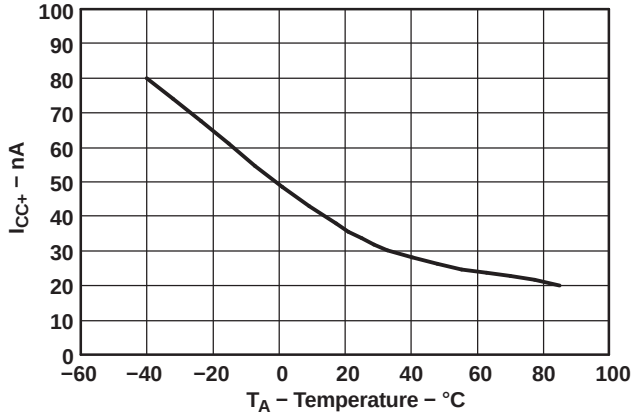


Figure 9. Power-Supply Current vs Temperature (V_+ = 5 V)

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	IN1	Digital control to connect COM to NO or NC
2	NO1	Normally open
3	GND	Digital ground
4	NO2	Normally open
5	IN2	Digital control to connect COM to NO or NC
6	COM2	Common
7	NC2	Normally closed
8	V_+	Power supply
9	NC1	Normally closed
10	COM1	Common

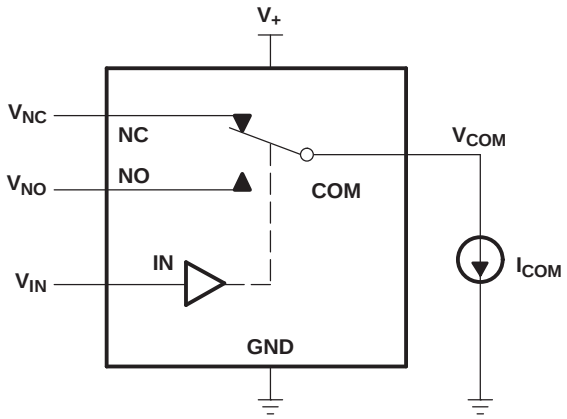
PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (NO to COM or NC to COM) in the ON state and the output (NC or NO) being open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Minimum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at IN
I_{IH}, I_{IL}	Leakage current measured at IN
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulombs) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance and ΔV_O is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NC to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_{IN}	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. OFF isolation, O_{ISO} = 20 LOG (V_{NC}/V_{COM}) dB, V_{COM} is the input and V_{NC} is the output.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured at a specific frequency and in dB. Crosstalk, X_{TALK} = 20 log (V_{NC1}/V_{NO1}), V_{NO1} is the input and V_{NC1} is the output.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the dc gain. Gain is measured from the equation, 20 log (V_{NC}/V_{COM}) dB, where V_{NC} is the output and V_{COM} is the input.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

PARAMETER MEASUREMENT INFORMATION

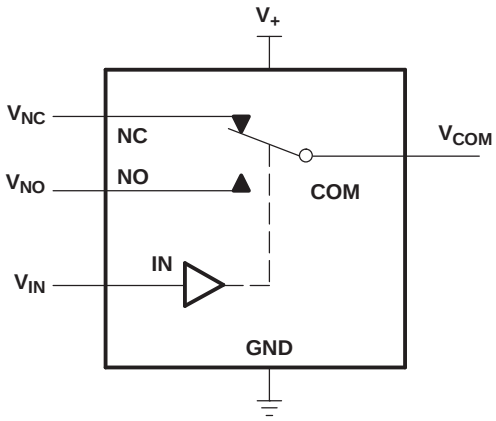


Channel ON

$$r_{on} = \frac{V_{COM} - V_{NO/NC}}{I_{COM}} \Omega$$

$V_{IN} = V_{IH}$ or V_{IL}

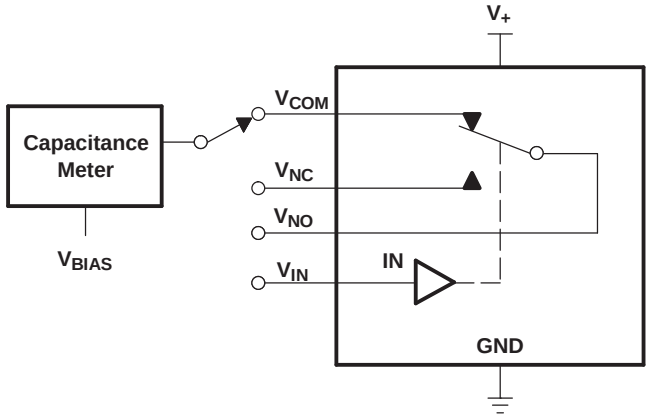
Figure 10. ON-State Resistance ($_{on}$)



OFF-State Leakage Current
Channel OFF
$V_{IN} = V_{IH}$ or V_{IL}
V_{NC} or V_{NO} = 0 to V_+
or
V_{COM} = 0 to V_+

ON-State Leakage Current
Channel ON
$V_{IN} = V_{IH}$ or V_{IL}
V_{NC} or V_{NO} = 0 to V_+, V_{COM} = Open
or
V_{NC} or V_{NO} = Open, V_{COM} = 0 to V_+

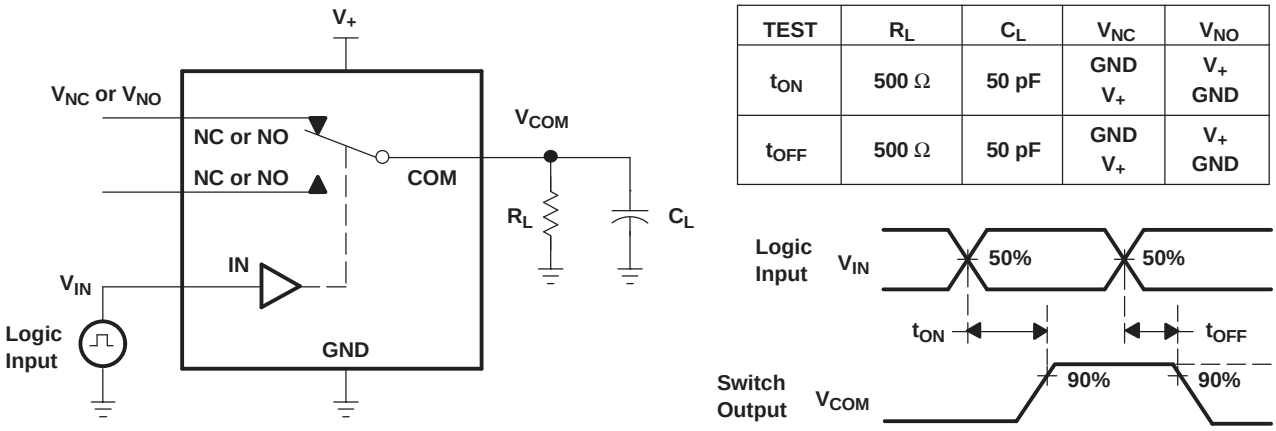
Figure 11. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)



$V_{BIAS} = V_+$ or GND
$V_{IN} = V_{IH}$ or V_{IL}
Capacitance is measured at NC, NO, COM, and IN inputs during ON and OFF conditions.

Figure 12. Capacitance $_{IN}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)



TEST	R_L	C_L	V_{NC}	V_{NO}
t_{ON}	500 Ω	50 pF	GND V_+	V_+ GND
t_{OFF}	500 Ω	50 pF	GND V_+	V_+ GND

Figure 13. Turn-On (t_{ON}) and Turn-Off (t_{OFF}) Time

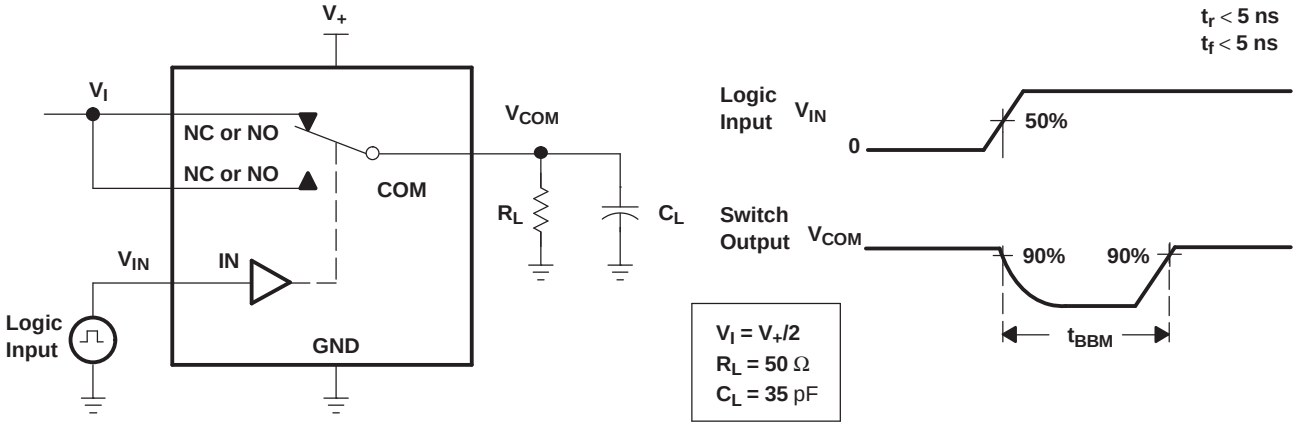


Figure 14. Break-Before-Make (t_{BBM}) Time

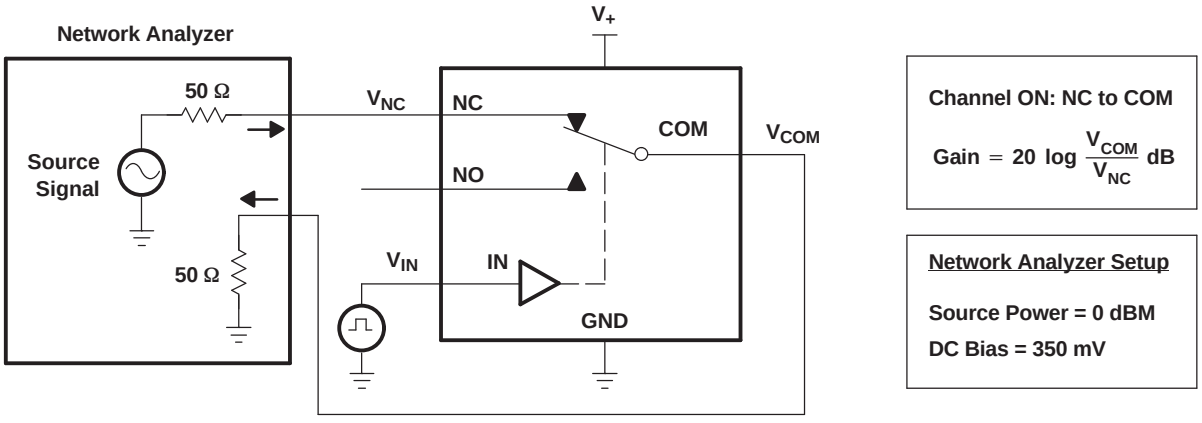
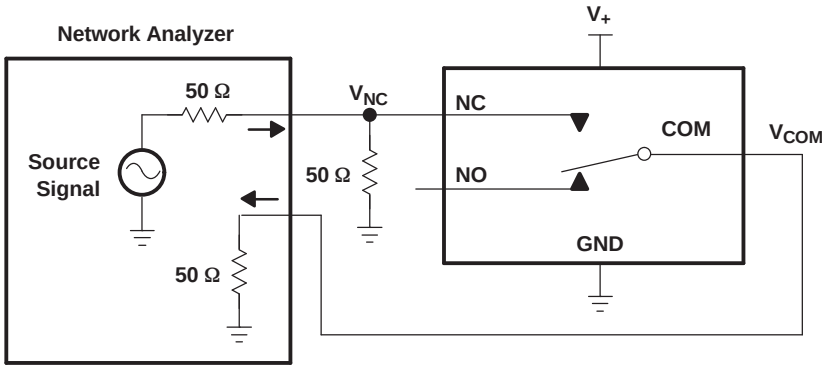


Figure 15. Frequency Response (BW)

PARAMETER MEASUREMENT INFORMATION (continued)



Channel OFF: NC to COM

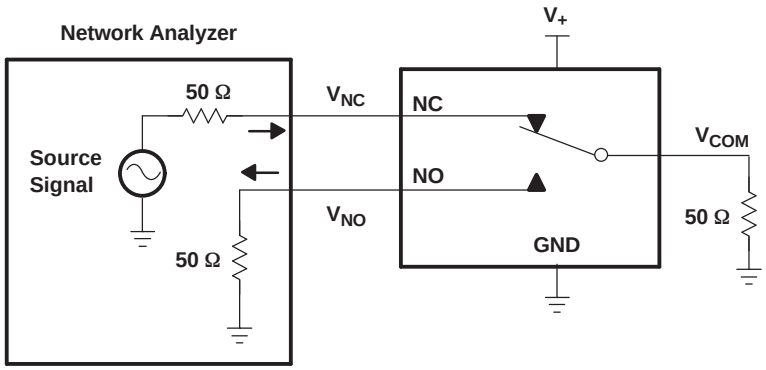
$$\text{OFF Isolation} = 20 \log \frac{V_{COM}}{V_{NC}} \text{ dB}$$

Network Analyzer Setup

Source Power = 0 dBM

DC Bias = 350 mV

Figure 16. OFF Isolation (O_{ISO})



Channel ON: NC to COM

Channel OFF: NO to COM

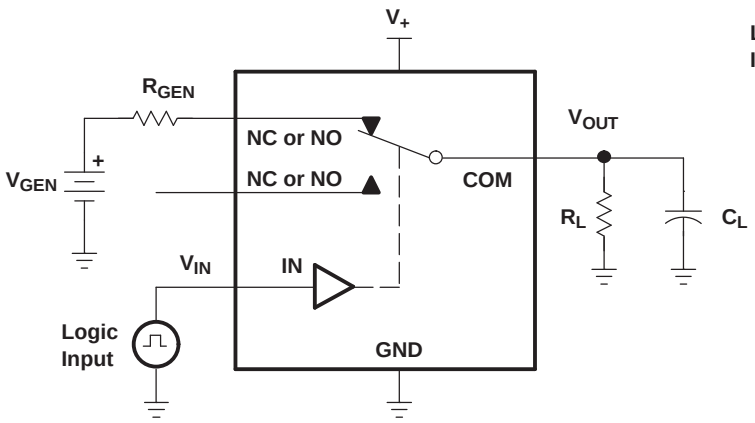
$$\text{Crosstalk} = 20 \log \frac{V_{NO}}{V_{NC}} \text{ dB}$$

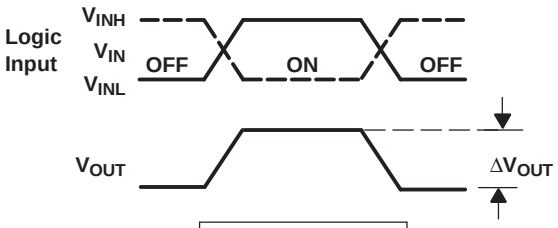
Network Analyzer Setup

Source Power = 0 dBM

DC Bias = 350 mV

Figure 17. Crosstalk (X_{TALK})





V_{GEN} = 0
R_{GEN} = 0
R_L = 1 MΩ
C_L = 35 pF
$Q_C = C_L \times \Delta V_{OUT}$
$V_{IN} = V_{IH}$ or V_{IL}

Figure 18. Charge Injection (Q_C)

PARAMETER MEASUREMENT INFORMATION (continued)

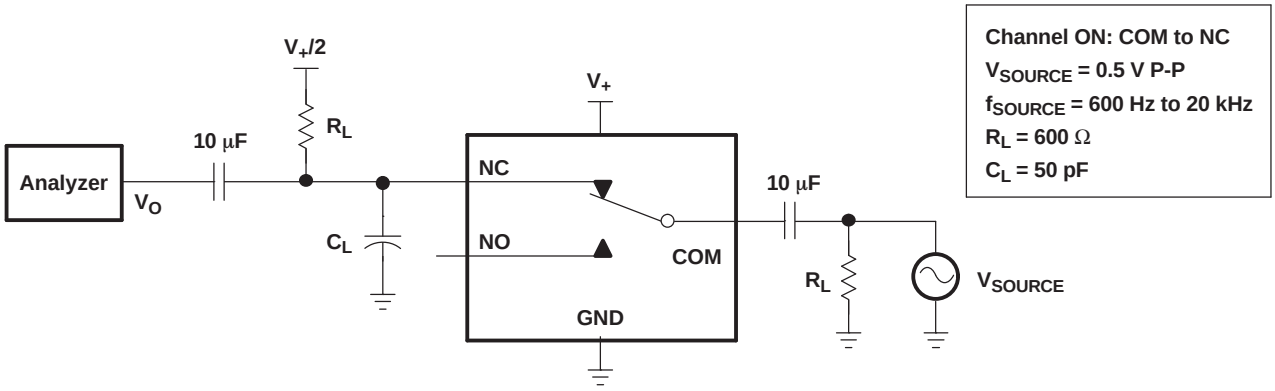


Figure 19. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A23157DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBR	Samples
TS5A23157DGSRE4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBR	Samples
TS5A23157DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBR	Samples
TS5A23157DGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBR	Samples
TS5A23157DGSTE4	ACTIVE	VSSOP	DGS	10		TBD	Call TI	Call TI	-40 to 85		Samples
TS5A23157DGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBR	Samples
TS5A23157RSER	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBO	Samples
TS5A23157RSERG4	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TS5A23157 :

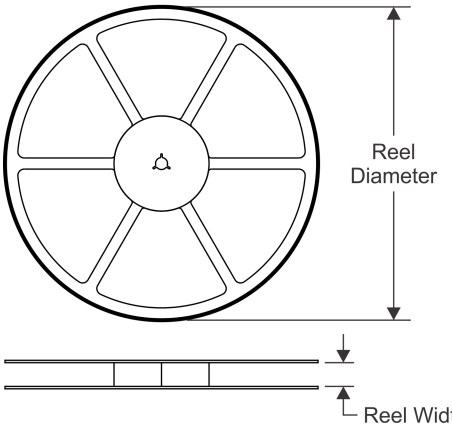
- Automotive: TS5A23157-Q1

NOTE: Qualified Version Definitions:

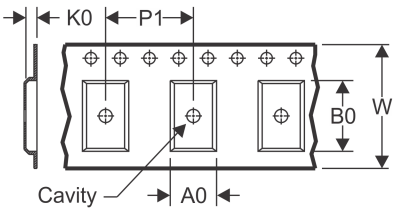
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

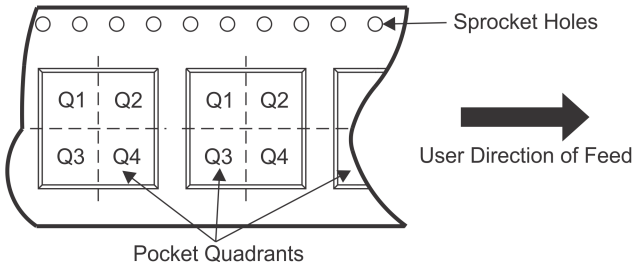


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

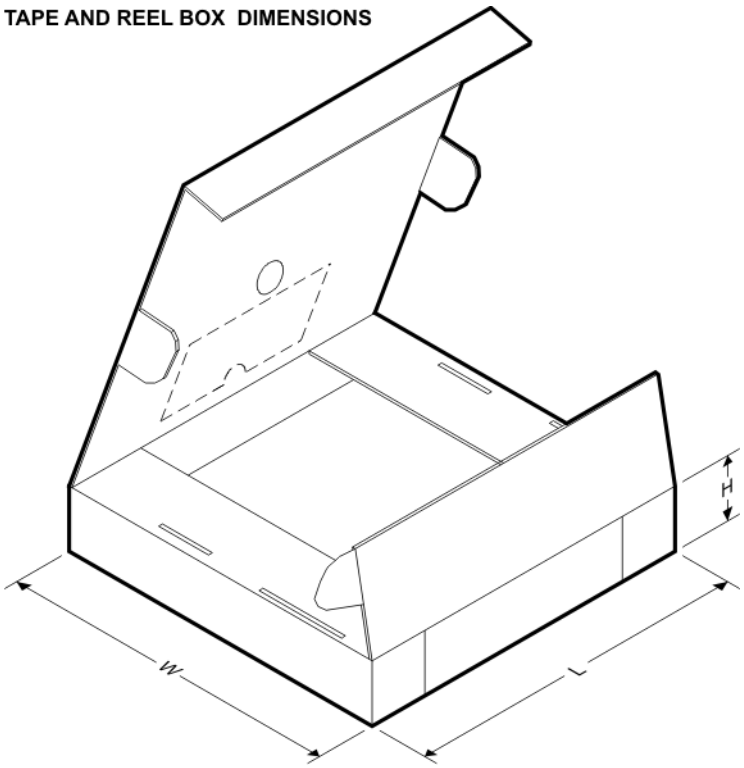
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23157DGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23157RSER	UQFN	RSE	10	3000	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1

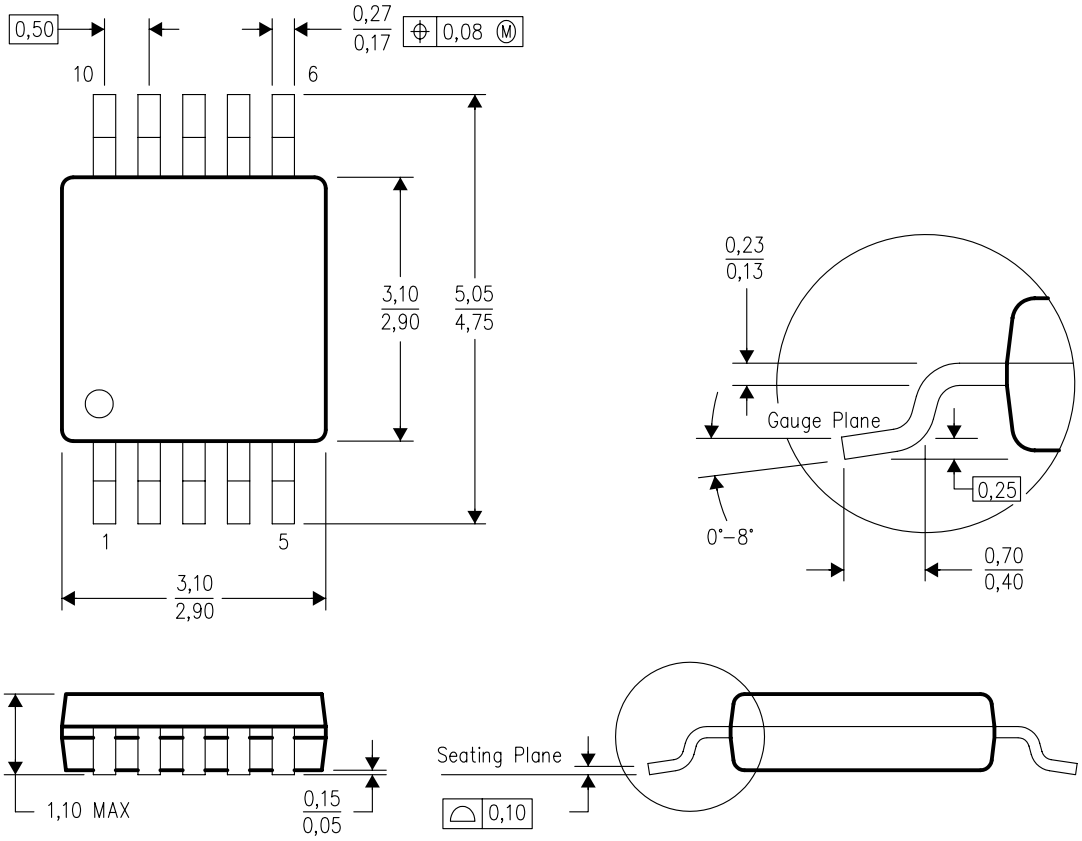
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23157DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS5A23157DGST	VSSOP	DGS	10	250	358.0	335.0	35.0
TS5A23157RSER	UQFN	RSE	10	3000	203.0	203.0	35.0

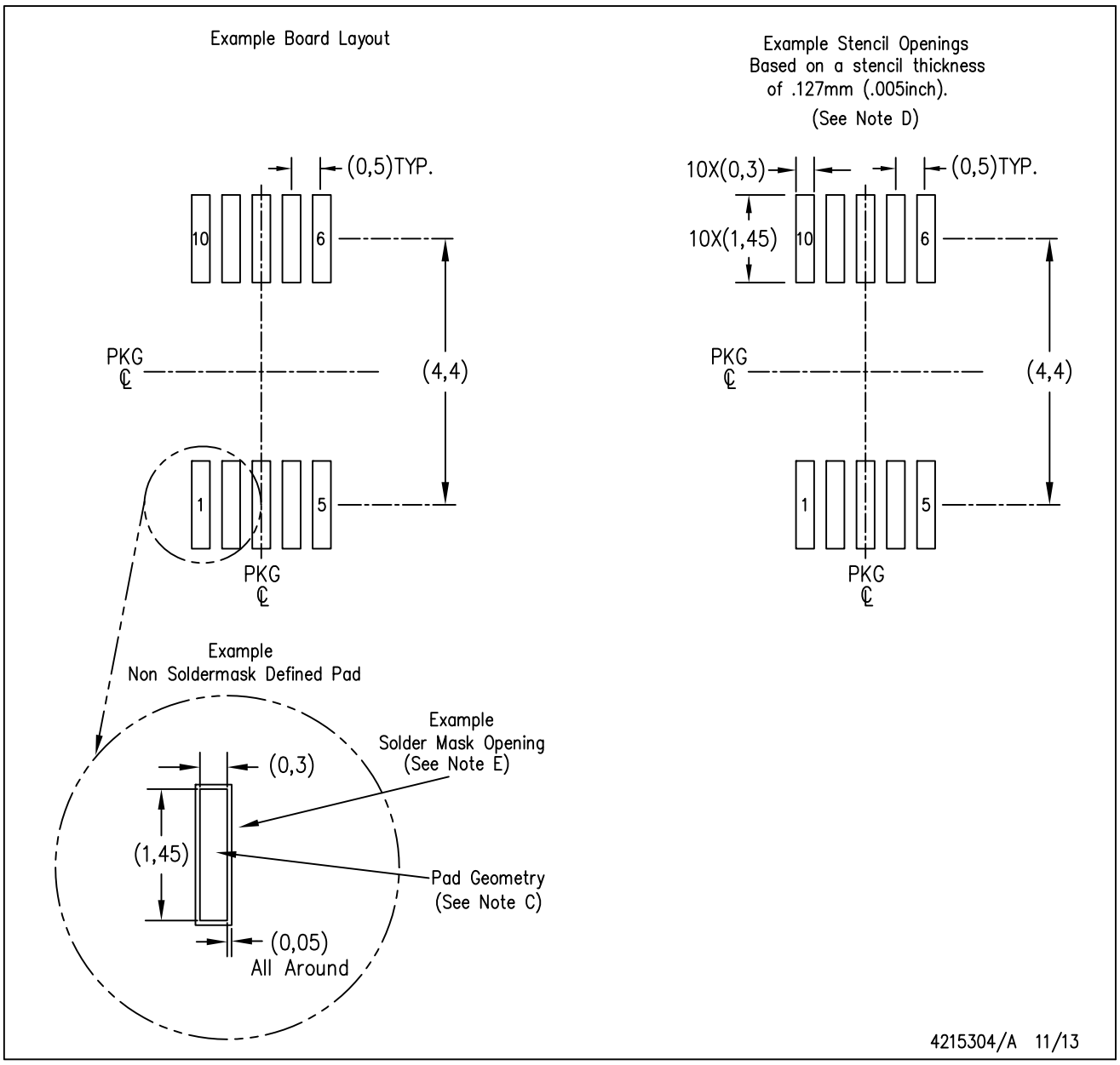
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

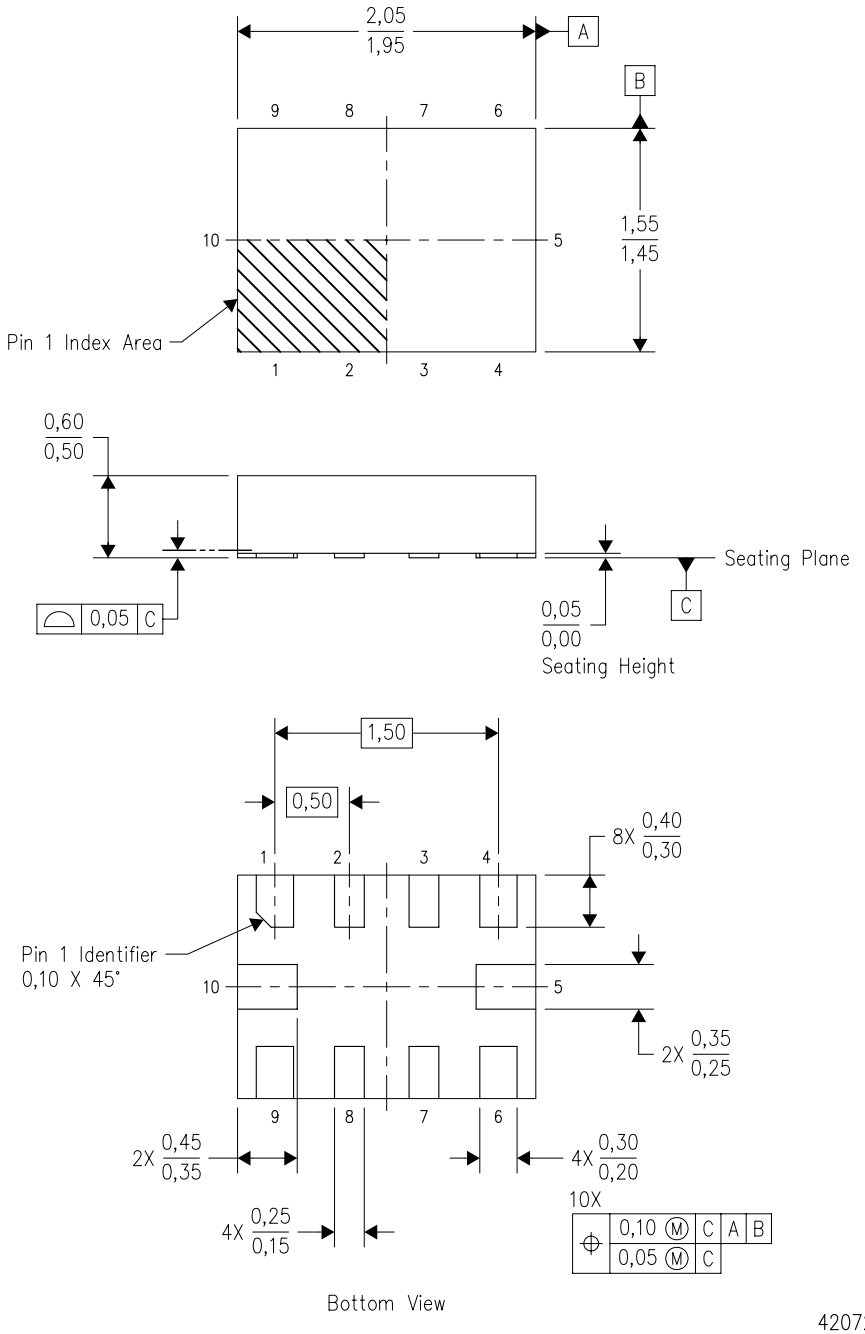
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

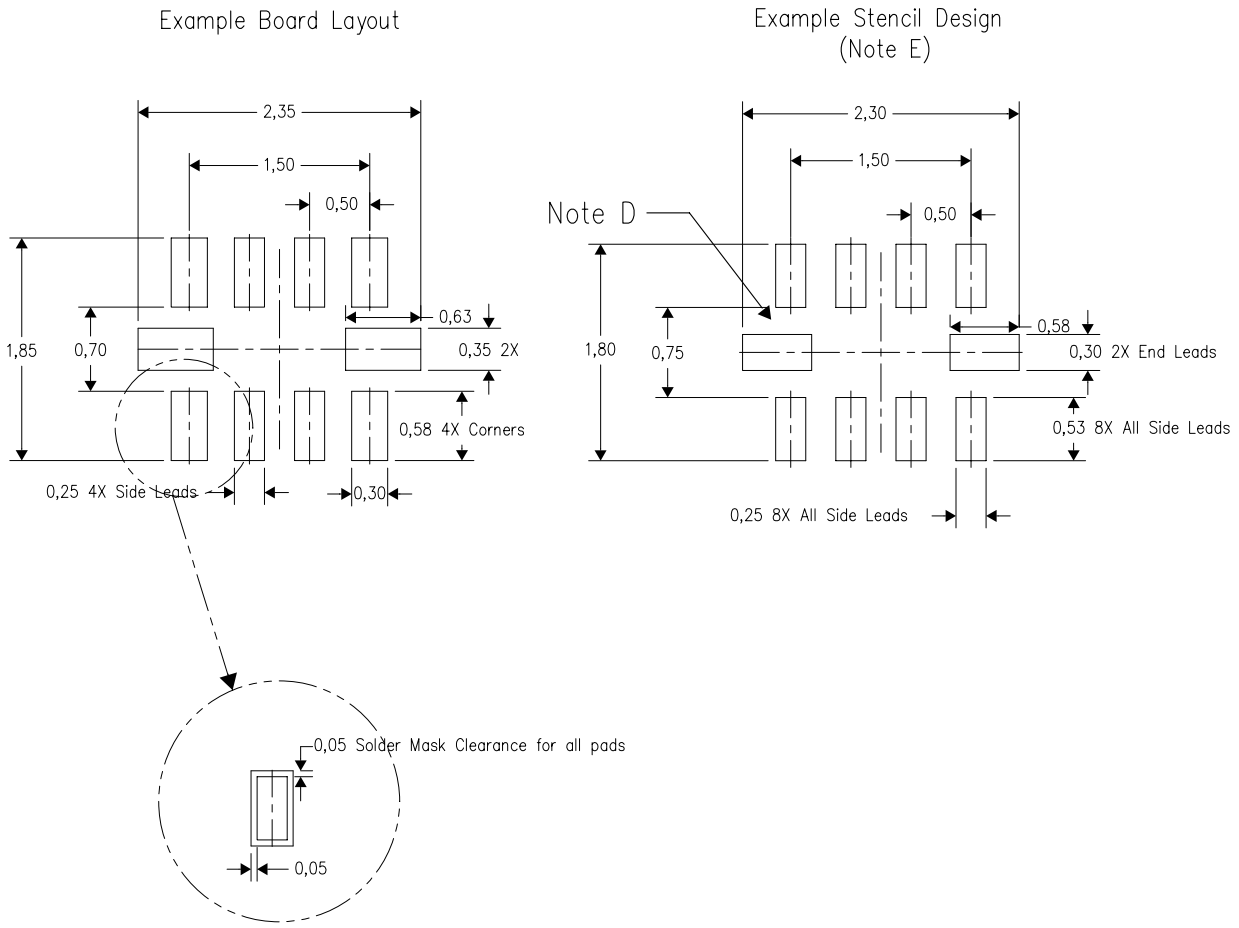
RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



4207268–3/D 01/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UEFD.

RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



4208106–3/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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