LM3554 Synchronous Boost Converter With 1.2-A Dual High-Side LED Drivers and I²C-Compatible Interface

1 Features

- Input Voltage: 2.5 V to 5.5 V
- Programmable 4.5-V or 5-V Constant Output Voltage
- Dual High-Side Current Sources
- Grounded Cathode Allowing for Better Heat Sinking and LED Routing
- > 90% Efficiency
- Ultra-Small Solution Size: < 23 mm^2
- Four Operating Modes: Torch, Flash, LED Indicator, and Voltage Output
- Accurate and Programmable LED Current from 37.5 mA to 1.2 A
- Hardware Flash and Torch Enable
- LED Thermal Sensing and Current Scaleback
- Software Selectable Input Voltage Monitor
- Programmable Flash Timeout
- Dual Synchronization Inputs for RF Power-Amplifier Pulse Events
- Open and Short LED Detection
- Active High Hardware Enable for Protection Against System Faults
- 400-kHz I²C-Compatible Interface

2 Applications

- Camera Phone LED Flash Controller
- Class D Audio Amplifier Power
- LED Current Source Biasing

3 Description

The LM3554 is a 2-MHz fixed-frequency, current-mode synchronous boost converter. The device is designed to operate as a dual 600-mA (1.2 A total) constant-current driver for high-current white LEDs, or as a regulated 4.5-V or 5-V voltage source.

The main features include: an I²C-compatible interface for controlling the LED current or the desired output voltage, a hardware flash enable input for direct triggering of the flash pulse, and dual TX inputs which force the flash pulse into a low-current torch mode allowing for synchronization to RF power amplifier events or other high-current conditions. Additionally, an active high hardware enable (HWEN) input provides a hardware shutdown during system software failures.

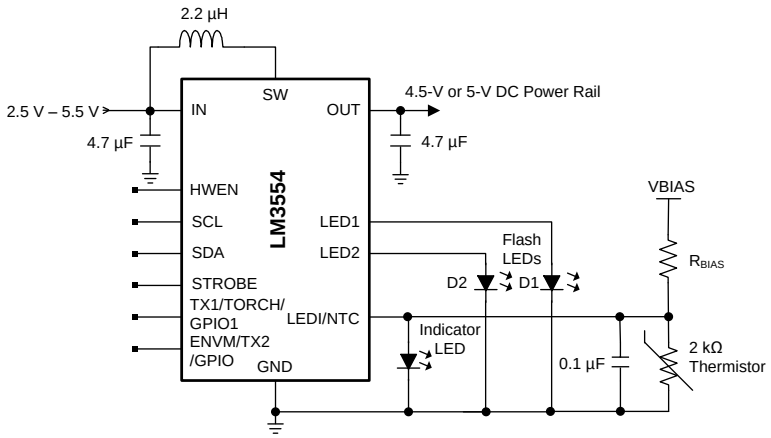
Five protection features are available within the LM3554 including a software selectable input voltage monitor, an internal comparator for interfacing with an external temperature sensor, four selectable current limits to ensure the battery current is kept below a predetermined peak level, an overvoltage protection feature to limit the output voltage during LED open circuits, and an output short circuit protection which limits the output current during shorts to GND.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3554	DSBGA (16)	1.685 mm × 1.685 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2013) to Revision C — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

Changes from Revision A (May 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 40

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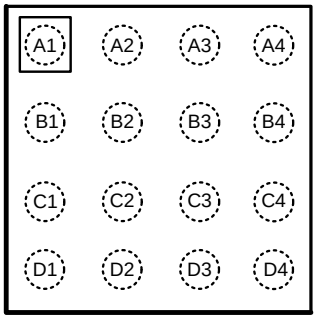
5 Pin Configuration and Functions

YFQ Package
16-Pin DSBGA
Top View



Pin Descriptions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
A1	LED1	Power	High-side current source output for flash LED.
A2, B2	OUT	Power	Step-up DC-DC converter output.
A3, B3	SW	Power	Drain connection for internal NMOS and synchronous PMOS switches.
A4, B4	GND	Ground	Ground
B1	LED2	Power	High-side current source output for flash LED.
C1	LEDI/NTC	Input/Output	Configurable as a high-side current source output for indicator LED or threshold detector for LED temperature sensing.
C2	TX1/TORCH/GPIO1	Input/Output	Configurable as a RF power amplifier synchronization control input (TX1), a hardware torch enable (TORCH), or a programmable general-purpose logic input/output (GPIO1).
C3	STROBE	Input	Active high hardware flash enable. Drive STROBE high to turn on flash pulse.
C4	IN	Power	Input voltage connection. Connect IN to the input supply, and bypass to GND with a minimum 4.7-µF ceramic capacitor.
D1	ENVM/TX2/GPIO2/INT	Input/Output	Configurable as an active high voltage mode enable (ENVM), dual polarity power amplifier synchronization input (TX2), or programmable general purpose logic input/output (GPIO2).
D2	SDA	Input/Output	Serial data input output
D3	SCL	Input	Serial clock input
D4	HWEN	Input	Active low hardware reset

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
V_{IN}, V_{SW}, V_{OUT}	–0.3	6	V
V_{SCL}, V_{SDA}, V_{HWEN}, V_{STROBE}, $V_{TX1/TORCH}$, $V_{ENVM/TX2}$, V_{LED1}, V_{LED2}, $V_{LEDI/NTC}$	0.3 V to (V_{IN} + 0.3 V) w/ 6 V max		
Continuous power dissipation(4)	Internally limit		
Junction temperature, T_{J-MAX}		150	°C
Maximum lead temperature (soldering)	See(5)		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=150°C (typical) and disengages at T_J=135°C (typical).
(5) For detailed soldering specifications and information, refer to *AN1112 DSBGA Wafer Level Chip-Scale Package* (SNVA009).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Input voltage, V_{IN}	2.5		5.5	V
Junction temperature, T_J	–30		125	°C
Ambient temperature, T_A(2)	–30		85	°C

(1) All voltages are with respect to the potential at the GND pin.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LM3554 YFQ (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Unless otherwise specified, typical limits are for T_A = 25°C, minimum and maximum limits in apply over the full operating ambient temperature range (–30°C ≤ T_A ≤ +85°C), V_{IN} = 3.6 V, and V_{HWEN} = V_{IN}. (1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT SOURCE SPECIFICATIONS							
I_{LED}	Current source accuracy	600-mA flash LED setting, V_{OUT} = V_{IN}	I_{LED1} and I_{LED2}	1128	1200	1284	mA
			I_{LED1} or I_{LED2}	541	600	657	
		17-mA torch current setting V_{HR} = 500 mV	I_{LED1} and I_{LED2}	30.4	33.8	37.2	
V_{HR}	Current source regulation voltage (V_{OUT} – V_{LED})	600-mA setting, V_{OUT} = 3.75 V			300		mV
I_{MATCH}	LED Current Matching	600-mA setting, V_{LED} = 3.2 V			0.35%		
STEP-UP DC-DC CONVERTER							
V_{REG}	Output voltage accuracy	2.7 V ≤ V_{IN} ≤ 4.2 V, I_{OUT} = 0 mA V_{ENVM} = V_{IN}, OV bit = 0		4.8	5	5.2	V
V_{OVP}	Output overvoltage protection trip point(3)	On threshold, 2.7 V ≤ V_{IN} ≤ 5.5 V		5.4	5.6	5.7	V
		Off threshold			5.3		
R_{PMOS}	PMOS switch on-resistance	I_{PMOS} = 1 A			150		mΩ
R_{NMOS}	NMOS switch on-resistance	I_{NMOS} = 1 A			150		mΩ
I_{CL}	Switch current limit(4)	CL bits = 00		0.711	1.05	1.373	A
		CL bits = 01		1.295	1.51	1.8	
		CL bits = 10		1.783	1.99	2.263	
		CL bits = 11		2.243	2.45	2.828	
I_{OUT_SC}	Output short-circuit current limit	V_{OUT} < 2.3 V			550		mA
$I_{LED/NTC}$	Indicator current	LEDI/NTC bit = 0	IND1, IND0 bits = 00		2.3		mA
			IND1, IND0 bits = 01		4.6		
			IND1, IND0 bits = 10		6.9		
			IND1, IND0 bits = 11		8.2		
V_{TRIP}	Comparator trip threshold	LEDI/NTC bit = 1, 2.7 V ≤ V_{IN} ≤ 5.5 V		0.947	1.052	1.157	V
f_{SW}	Switching frequency	2.7 V ≤ V_{IN} ≤ 5.5 V		1.75	2	2.23	MHz
I_Q	Quiescent supply current	Device not switching			630		µA
I_{SHDN}	Shutdown supply current	2.7 V ≤ V_{IN} ≤ 5.5 V			3.5	6.6	µA
t_{TX}	Flash-to-torch LED current settling time	TX_ Low to High, I_{LED1} + I_{LED2} = 1.2 A to 180 mA			20		µs

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum (MIN) and maximum (MAX) limits are ensured by design, test, or statistical analysis. Typical (TYP) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = 3.6 V and T_A = 25°C.
(3) The typical curve for overvoltage protection (OVP) is measured in closed loop using the *Typical Application Circuit*. The OVP value is found by forcing an open circuit in the LED1 and LED2 path and recording the peak value of V_{OUT}. The value given in *Electrical Characteristics* is found in an open-loop configuration by ramping the voltage at OUT until the OVP comparator trips. The closed loop data can appear higher due to the stored energy in the inductor being dumped into the output capacitor after the OVP comparator trips. At worst case is an open circuit condition where the output voltage can continue to rise after the OVP comparator trips by approximately I_{IN}× sqrt (L/C_{OUT}).
(4) The typical curve for Current Limit is measured in closed loop using the *Typical Application Circuit* by increasing I_{OUT} until the peak inductor current stops increasing. The value given in *Electrical Characteristics* is measured open loop and is found by forcing current into SW until the current limit comparator threshold is reached. Closed loop data appears higher due to the delay between the comparator trip point and the NFET turning off. This delay allows the closed-loop inductor current to ramp higher after the trip point by approximately 20 ns × V_{IN} / L.

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Electrical Characteristics (continued)

Unless otherwise specified, typical limits are for T_A = 25°C, minimum and maximum limits in apply over the full operating ambient temperature range (–30°C ≤ T_A ≤ +85°C), V_{IN} = 3.6 V, and V_{HWEN} = V_{IN}. (1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN_TH}	VIN monitor trip threshold	V_{IN} falling, VIN monitor register = 0x01 (enabled with V_{IN_TH} = 3.1 V)	2.95	3.09	3.23	V
TX1/TORCH/GPIO1, STROBE, HWEN, ENVM/TX2/GPIO2 VOLTAGE						
V_{IL}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
V_{IH}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V	1.2		V_{IN}	V
V_{OL}	Output logic low	I_{LOAD} = 3 mA, 2.7 V ≤ V_{IN} ≤ 5.5 V			400	mV
$R_{TX1/TORCH}$	Internal pulldown resistance at TX1/TORCH			300		kΩ
R_{STROBE}	Internal pulldown resistance at STROBE			300		kΩ
I²C-COMPATIBLE VOLTAGE SPECIFICATIONS (SCL, SDA)						
V_{IL}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
V_{IH}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V	1.22		V_{IN}	V
V_{OL}	Output logic low (SCL)	I_{LOAD} = 3 mA, 2.7 V ≤ V_{IN} ≤ 5.5 V			400	mV

6.6 Timing Requirements

See Figure 1.

		MIN	NOM	MAX	UNIT
1 / t_1	SCL clock frequency		400		kHz
t_2	Data in setup time to SCL high	100			ns
t_3	Data out stable after SCL low	0			ns
t_4	SDA low setup time to SCL low (start)	160			ns
t_5	SDA high hold time after SCL high (stop)	160			ns

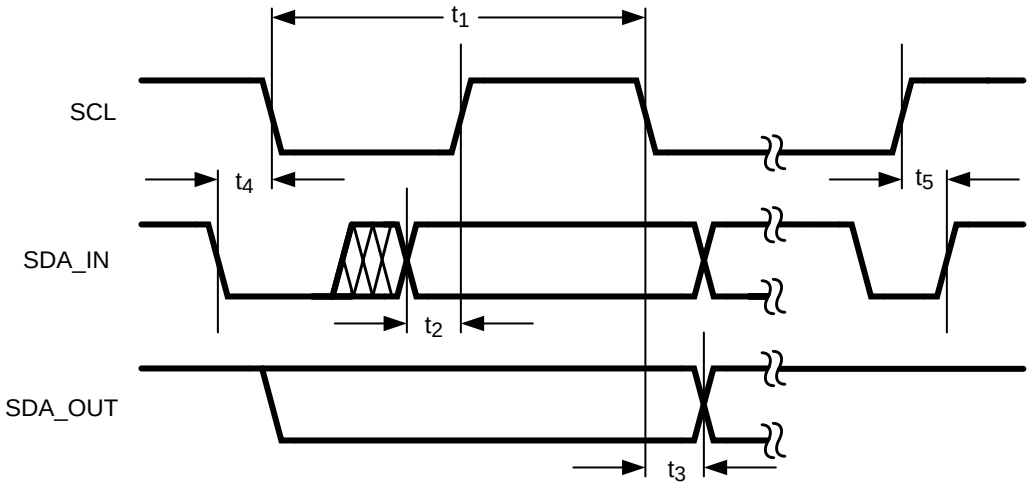

Figure 1. I²C Timing

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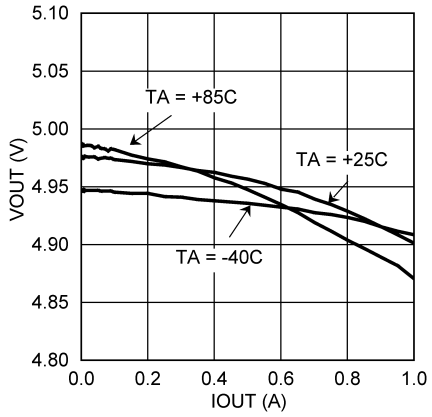
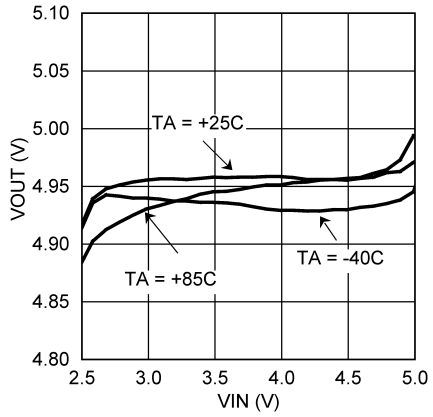
6.7 Typical Characteristics

V_{IN} = 3.6 V, LEDs are Lumiled PWF-4, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, L = FDSE0312-2R2 (2.2 µH, R_L = 0.15 Ω), T_A = 25°C, unless otherwise specified.



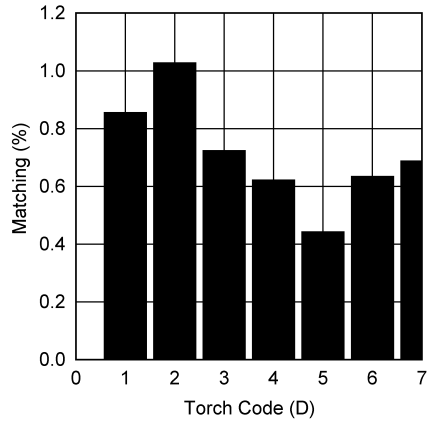
V_{OUT} = 5 V Voltage-Output Mode

Figure 2. V_{OUT} vs I_{OUT}



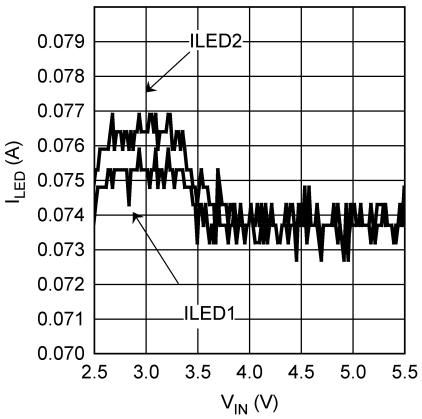
V_{OUT} = 5 V Voltage-Output Mode

Figure 3. V_{OUT} vs V_{IN}



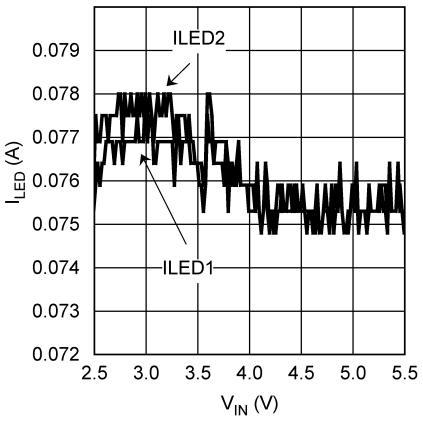
V_{IN} = 3.6 V V_{LED1}, V_{LED2} = 3.2 V T_A = –40°C to +85°C
Current Matching = Abs Value $((I_{LED1}–I_{LED2})÷(I_{LED1}+I_{LED2}))×100$

Figure 4. Torch Current Matching vs Code



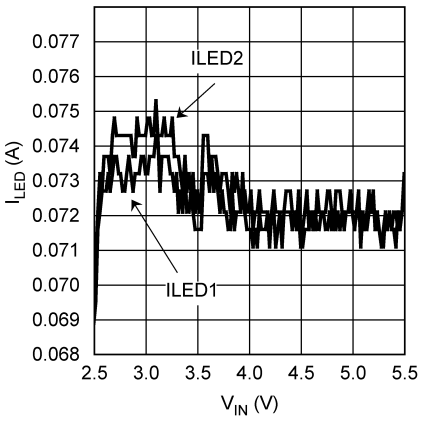
V_{LED1}, V_{LED2} = 3.2 V 75-mA Setting T_A = 25°C

Figure 5. Torch Current vs V_{IN}



V_{LED1}, V_{LED2} = 3.2 V 75-mA Setting T_A = 85°C

Figure 6. Torch Current vs V_{IN}



V_{LED1}, V_{LED2} = 3.2 V 75-mA Setting T_A = –40°C

Figure 7. Torch Current vs V_{IN}

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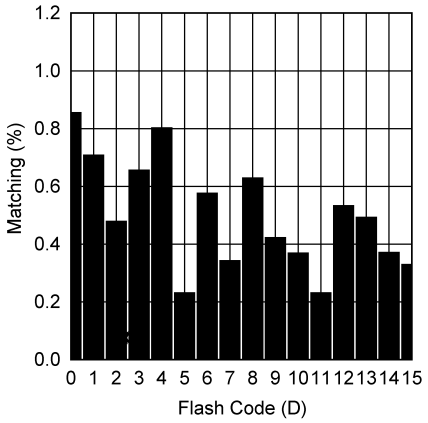
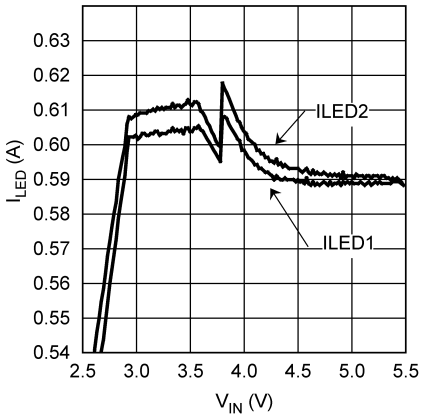
Typical Characteristics (continued)

V_{IN} = 3.6 V, LEDs are Lumiled PWF-4, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, L = FDSE0312-2R2 (2.2 µH, R_L = 0.15 Ω), T_A = 25°C, unless otherwise specified.



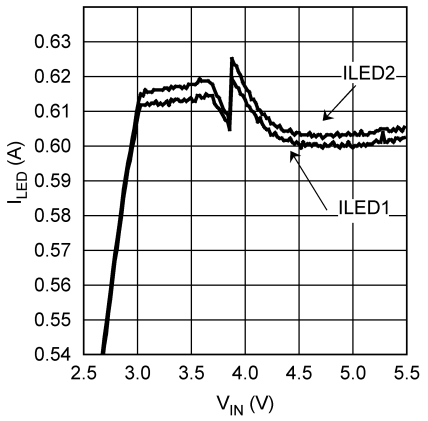
V_{IN} = 3.6 V V_{LED1}, V_{LED2} = 3.2 V T_A = –40°C To +85°C
Current Matching = Abs Value ((I_{LED1}–I_{LED2})÷(I_{LED1}+I_{LED2}))×100

Figure 8. Flash Current Matching vs Code



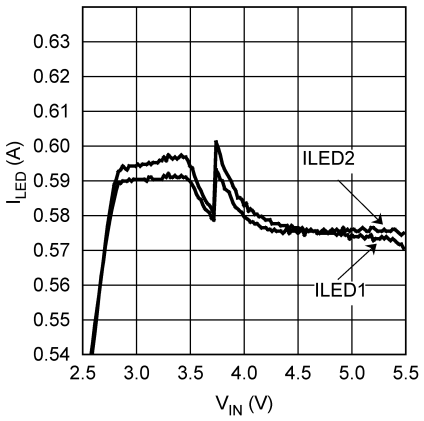
V_{LED1}, V_{LED2} = 3.2 V 600-mA Setting T_A = 25°C

Figure 9. Flash Current vs V_{IN}



V_{LED1}, V_{LED2} = 3.2 V 600-mA Setting T_A = 85°C

Figure 10. Flash Current vs V_{IN}



V_{LED1}, V_{LED2} = 3.2 V 600-mA Setting T_A = –40°C

Figure 11. Flash Current vs V_{IN}

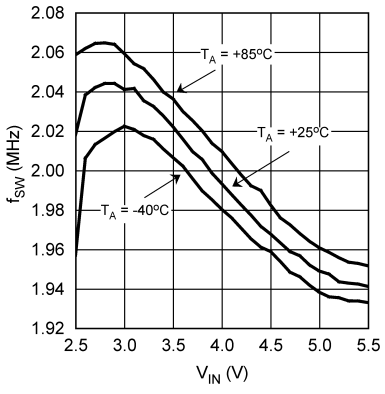
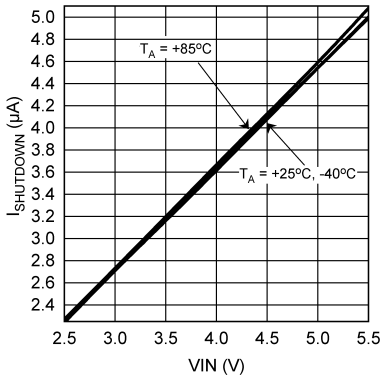


Figure 12. Switching Frequency vs V_{IN}



V_{HWEN} = 0 V

Figure 13. Shutdown Current vs V_{IN}

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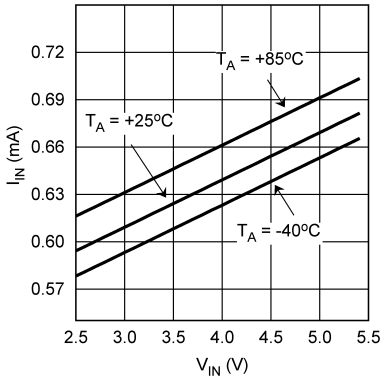
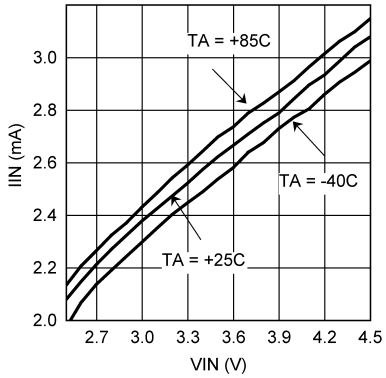
Typical Characteristics (continued)

V_{IN} = 3.6 V, LEDs are Lumiled PWF-4, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, L = FDSE0312-2R2 (2.2 µH, R_L = 0.15 Ω), T_A = 25°C, unless otherwise specified.



V_{LED} = 1.5 V

Figure 14. Active (Non-Switching) Supply Current vs V_{IN}



V_{OUT} = 5 V I_{OUT} = 400 mA

Figure 15. Active (Switching) Supply Current vs V_{IN}

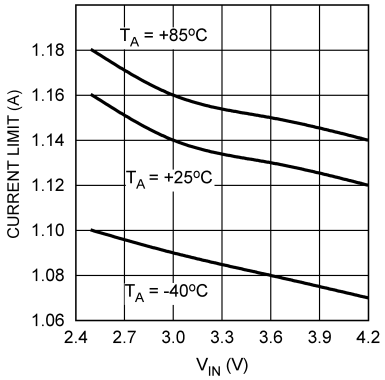


Figure 16. Closed Loop Current Limit vs V_{IN} (Flash Duration Register Bits [6:5] = 00)(1)

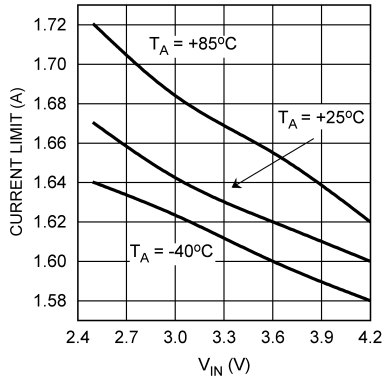


Figure 17. Closed Loop Current Limit vs V_{IN} (Flash Duration Register Bits [6:5] = 01)(1))

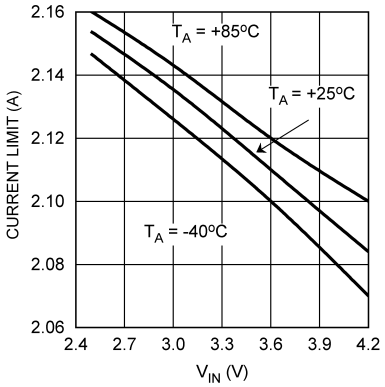


Figure 18. Closed Loop Current Limit vs V_{IN} (Flash Duration Register Bits [6:5] = 10)(1)

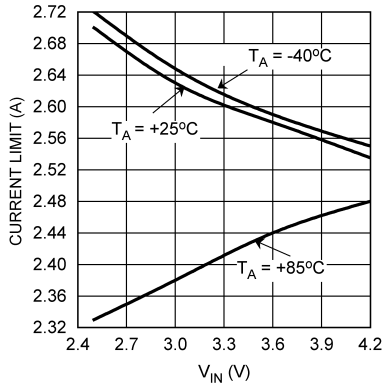


Figure 19. Closed Loop Current Limit vs V_{IN} (Flash Duration Register Bits [6:5] = 11)(1)

(1) The typical curve for Current Limit is measured in closed loop using the *Typical Application Circuit* by increasing I_{OUT} until the peak inductor current stops increasing. The value given in *Electrical Characteristics* is measured open loop and is found by forcing current into SW until the current limit comparator threshold is reached. Closed loop data appears higher due to the delay between the comparator trip point and the NFET turning off. This delay allows the closed-loop inductor current to ramp higher after the trip point by approximately 20 ns × V_{IN} / L.

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Typical Characteristics (continued)

V_{IN} = 3.6 V, LEDs are Lumiled PWF-4, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, L = FDSE0312-2R2 (2.2 µH, R_L = 0.15 Ω), T_A = 25°C, unless otherwise specified.

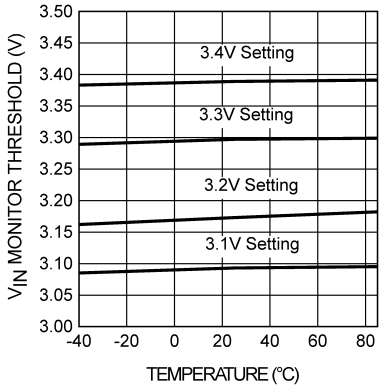


Figure 20. V_{IN} Monitor Thresholds vs Temperature

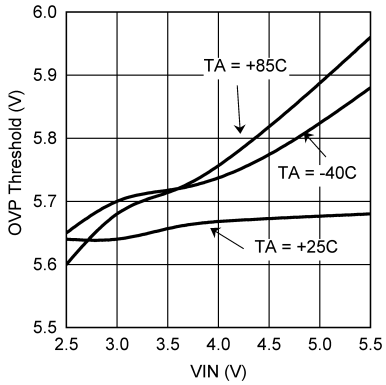


Figure 21. OVP Thresholds vs V_{IN} (1)

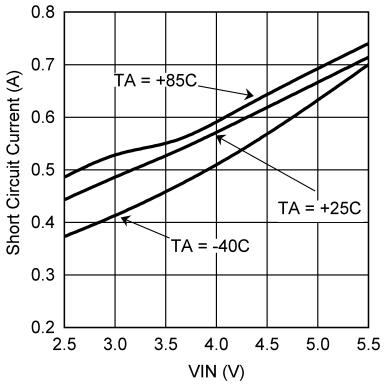
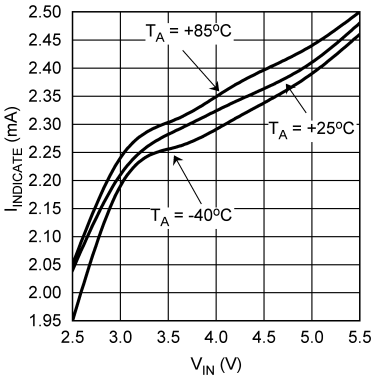
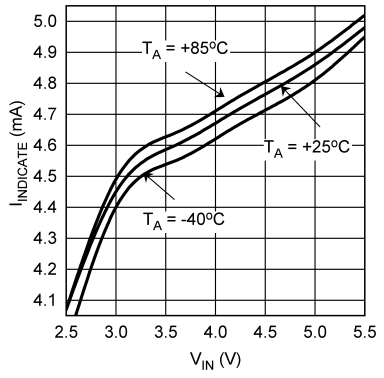


Figure 22. Short Circuit Current Limit vs V_{IN}



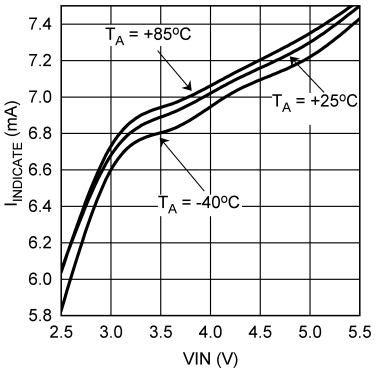
V_{LEDI} = 2 V

Figure 23. Indicator Current vs V_{IN} (Torch Brightness Register Bits[7:6] = 00)



V_{LEDI} = 2 V

Figure 24. Indicator Current vs V_{IN} (Torch Brightness Register Bits[7:6] = 01)



V_{LEDI} = 2 V

Figure 25. Indicator Current vs V_{IN} (Torch Brightness Register Bits[7:6] = 10)

(1) The typical curve for overvoltage protection (OVP) is measured in closed loop using the *Typical Application Circuit*. The OVP value is found by forcing an open circuit in the LED1 and LED2 path and recording the peak value of V_{OUT}. The value given in *Electrical Characteristics* is found in an open-loop configuration by ramping the voltage at OUT until the OVP comparator trips. The closed loop data can appear higher due to the stored energy in the inductor being dumped into the output capacitor after the OVP comparator trips. At worst case is an open circuit condition where the output voltage can continue to rise after the OVP comparator trips by approximately I_{IN}× sqrt (L/C_{OUT}).

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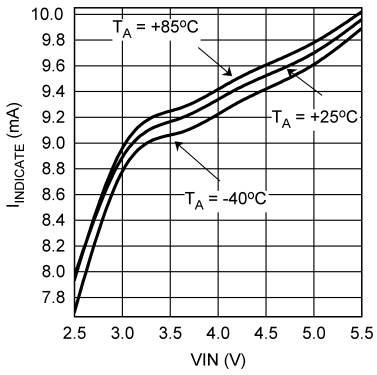
Typical Characteristics (continued)

V_{IN} = 3.6 V, LEDs are Lumiled PWF-4, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, L = FDSE0312-2R2 (2.2 µH, R_L = 0.15 Ω), T_A = 25°C, unless otherwise specified.



V_{LEDI} = 2 V

Figure 26. Indicator Current vs V_{IN} (Torch Brightness Register Bits[7:6] = 11)

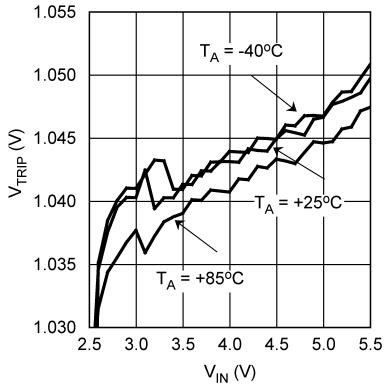


Figure 27. NTC Comparator Trip Threshold vs V_{IN}

7 Detailed Description

7.1 Overview

The LM3554 is a high-power white-LED flash driver capable of delivering up to 1.2-A of LED current into a single LED, or up to 600 mA into two parallel LEDs. The device incorporates a 2-MHz constant frequency, synchronous, current mode PWM boost converter, and two high-side current sources to regulate the LED current over the 2.5-V to 5.5-V input voltage range.

The LM3554 operates in two modes: LED mode or constant voltage-output mode. In LED mode when the output voltage is greater than V_{IN} – 150 mV, the PWM converter switches and maintains at least 300 mV (V_{HR}) across both current sources (LED1 and LED2). This minimum headroom voltage ensures that the current sinks remain in regulation. When the input voltage is above V_{LED} + V_{HR}, the device operates in pass mode with the device not switching and the PFET on continuously. In pass mode the difference between (V_{IN} – I_{LED} × R_{ON_P}) and V_{LED} is dropped across the current sources. If the device is operating in pass mode, and V_{IN} drops to a point that forces the device into switching, the device goes into switching mode one time. The LM3554 remains in switching mode until the device is shut down and re-enabled. This is true even if V_{IN} rises back above V_{LED} + 300 mV during the current flash or torch cycle. This prevents the LED current from oscillating when V_{IN} is operating close to V_{OUT}.

In voltage-output mode the LM3554 operates as a voltage output boost converter with selectable output voltages of 4.5 V and 5 V. In this mode the LM3554 is able to deliver up to typically 5 W of output power. At light loads and in voltage-output mode the PWM switching converter changes over to a pulsed frequency regulation mode and only switches as necessary to ensure proper LED current or output voltage regulation. This allows for improved light load efficiency compared to converters that operate in fixed-frequency PWM mode at all load currents.

Additional features of the LM3554 include four logic inputs, an internal comparator for LED thermal sensing, and a low-power indicator LED current source. The STROBE input provides a hardware flash mode enable. The ENVM/TX2/GPIO2 input is configurable as a hardware voltage-output mode enable (ENVM), an active high flash interrupt that forces the device from flash mode to a low-power TORCH mode (TX2), or as a programmable logic input/output (GPIO2). The TX1 input is configurable as an active high flash interrupt that forces the device from flash mode to a low-power torch mode (TX1), as a hardware torch mode enable (TORCH), or as a programmable logic input/output (GPIO1) . The HWEN input provides for an active low hardware shutdown of the device. Finally, the LEDI/NTC pin is configurable as a low-power indicator LED driver (LEDI), or as a threshold detector for thermal sensing (NTC). In NTC mode when the threshold (V_{TRIP}) at the LEDI/NTC pin is crossed ($V_{LEDI/NTC}$ falling), the flash pulse is forced to the torch current setting, or into shutdown depending on the NTC shutdown bit setting.

The device is controlled via an I^2C-compatible interface. This includes switchover from LED to voltage-output mode, adjustment of the LED current in torch mode, adjustment of the LED current in flash mode, adjustment of the indicator LED currents, changing the flash LED current duration, changing the switch current limit. Additionally, there are 5 flag bits that can be read back indicating flash current timeout, overtemperature condition, LED failure (open or short), LED thermal failure, and an input voltage fault.

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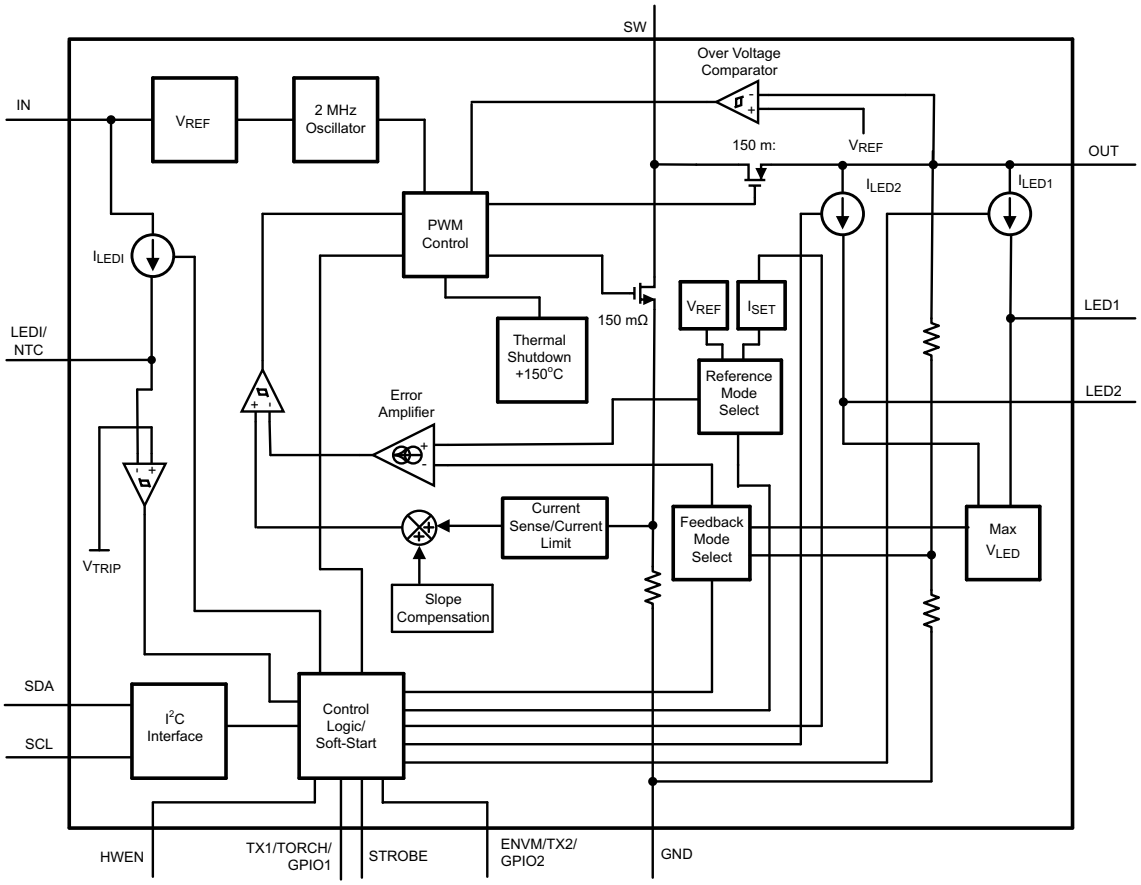
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Start-Up

The device is turned on through bits [2:0] of the Torch Brightness Register (0xA0), bits [2:0] of the Flash Brightness Register (0xB0), the ENVM input, or the STROBE input. Bits [1:0] of the Torch Brightness Register or Flash Brightness Register enables/disables the current sources (LED1, LED2, and LEDI). Bit [2] enables/disables the voltage-output mode. A logic high at STROBE enables flash mode. A logic high on the ENVM input forces the LM3554 into voltage-output mode.

On start-up, when V_{OUT} is less than V_{IN} the internal synchronous PFET turns on as a current source and delivers typically 350 mA to the output capacitor. During this time all current sources (LED1, LED2, and LEDI) are off. When the voltage across the output capacitor reaches 2.2 V, the current sources can turn on. At turnon the current sources step through each flash or torch level until the target LED current is reached (16 µs/step). This gives the device a controlled turnon and limits inrush current from the V_{IN} supply.

7.3.2 Overvoltage Protection

The output voltage is limited to typically 5.6 V (5.7 V maximum). In situations such as the current source open, the LM3554 raises the output voltage in order to keep the LED current at its target value. When V_{OUT} reaches 5.6 V the overvoltage comparator trips and turns off both the internal NFET and PFET. When V_{OUT} falls below 5.4 V (typical), the LM3554 begins switching again.

7.3.3 Current Limit

The LM3554 features four selectable current limits: 1 A, 1.5 A, 2 A, and 2.5 A. These are selectable through the I^2C-compatible interface via bits 5 (CL0) and 6 (CL1) of the Flash Duration Register. When the current limit is reached, the LM3554 device stops switching for the remainder of the switching cycle.

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Feature Description (continued)

Because the current limit is sensed in the NMOS switch there is no mechanism to limit the current when the device operates in pass mode. In situations where there could potentially be large load currents at OUT, and the LM3554 is operating in Pass mode, the load current must be limited to 2.5 A. In boost mode or pass mode if V_{OUT} falls below approximately 2.3 V, the device stops switching, and the PFET operates as a current source limiting the current to typically 350 mA. This prevents damage to the LM3554 and excessive current draw from the battery during output short circuit conditions.

7.3.4 Flash Termination (Strobe-Initiated Flash)

Bit [7] of the Flash Brightness Register (STR bit) determines how the flash pulse terminates with STROBE-initated flash pulses. With the STR bit = 1 the Flash current pulseonly terminates by reaching the end of the flash-timeout period. With STR = 0, Flash mode can be terminated by pulling STROBE low, or by allowing the flash-timeout period to elapse. If STR = 0 and STROBE is toggled before the end of the flash-timeout period, the timeout period resets on the rising edge of STROBE. See LM3554 Timing Diagrams regarding the flash pulse termination for the different STR bit settings.

After the flash pulse terminates, either by a flash timeout, or pulling STROBE low, LED1 and LED2 turn completely off. This happens even when Torch is enabled via the I^2C-compatible interface, and the flash pulse is turned on by toggling STROBE. After a flash event ends the EN1, EN0 bits (bits [1:0] of the Torch Brightness Register, or Flash Brightness Register) are automatically re-written with (0, 0).

7.3.5 Flash Termination (I^2C-Initiated Flash)

For I^2C-initiated flash pulses, the flash LED current can be terminated by either waiting for the timeout duration to expire or by writing a (0, 0) to bits [1:0] of the Torch Brightness Register, or Flash Brightness Register. If the timeout duration is allowed to elapse, the flash enable bits of the Torch Brightness and Flash Brightness Registers are automatically reset to 0.

7.3.6 Flash Timeout

The flash timeout period sets the duration of the flash current pulse. Bits [4:0] of the Flash Duration Register programs the 32 different flash timeout levels in steps of 32 ms giving a flash timeout range of 32 ms to 1024 ms (see Table 4).

7.3.7 Torch Mode

In torch mode the current sources LED1 and LED2 each provide 8 different current levels (see Table 2). The torch currents are adjusted by writing to bits [5:3] of the Torch Brightness Register. Torch mode is activated by setting Torch Brightness Register bits [1:0] to (1, 0) or Flash Brightness bits [1:0] to (1, 0). Once the torch mode is enabled the current sources ramp up to the programmed torch current level by stepping through all of the torch currents at 16 µs/step until the programmed torch current level is reached.

7.3.8 TX1/Torch

The TX1/TORCH/GPIO1 input has a triple function. With Configuration Register 1 Bit [7] = 0 (default), TX1/TORCH/GPIO1 is a power amplifier synchronization input (TX1 mode). This is designed to reduce the current pulled from the battery during an RF power amplifier transmit event. When the LM3554 is engaged in a flash event, and the TX1 pin is pulled high, both LED1 and LED2 are forced into torch mode at the programmed torch current setting. If the TX1 pin is then pulled low before the flash pulse terminates the LED current ramps back to the previous flash current level. At the end of the flash timeout whether the TX1 pin is high or low, the LED current turns off.

With the Configuration Register Bit [7] = 1, TX1/TORCH/GPIO1 is configured as a hardware torch mode enable (TORCH). In this mode a high at TORCH turns on the LED current sources in torch mode. STROBE (or I^2-initiated flash) takes precedence over the TORCH mode input. Figure 37 details the functionality of the hardware TORCH mode. Additionally, when a flash pulse is initiated during hardware TORCH mode, the hardware torch mode bit is reset at the end of the flash pulse. In order to re-enter hardware torch mode, bit [7] of Configuration Register 1 would have to be re-written with a 1.

The TX1/TORCH/GPIO1 input can also be configured as a GPIO input/output. for details on this, refer to the GPIO Register section of the datasheet.

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Feature Description (continued)

7.3.9 ENVM/TX2/GPIO2

The ENVM/TX2/GPIO2/INT pin has four functions. In ENVM mode (Configuration Register 1 bit [5] = 0), the ENVM/TX2/GPIO2/INT pin is an active high logic input that forces the LM3554 into voltage-output mode. In TX2 mode (Configuration Register 1 bit [5] = 1), the ENVM/TX2/GPIO2/INT pin is a Power Amplifier Synchronization input that forces the LM3554 from Flash mode into Torch mode. In GPIO2 mode (GPIO Register Bit [3] = 1) the ENVM/TX2/GPIO2/INT pin is configured as a general purpose logic input/output and controlled via bits[3:5] of the GPIO Register. In INT mode the ENVM/TX2/GPIO2/INT pin is a hardware interrupt output which pulls low when the LM3554 is in NTC mode, and the voltage at LEDI/NTC falls below V_{TRIP}.

In TX2 mode, when Configuration Register 1 bit [6] = 0 the ENVM/TX2/GPIO2 pin is an active low transmit interrupt input. Under this condition, when the LM3554 is engaged in a flash event, and ENVM/TX2/GPIO2 is pulled low, both LED1 and LED2 are forced into either torch mode or LED shutdown depending on the logic state of Configuration Register 2 bit [0]. In TX2 mode with Configuration Register 1 bit [6] = 1, the ENVM/TX2/GPIO2 pin is an active high transmit interrupt. Under this condition when the LM3554 is engaged in a Flash event, and the TX2 pin is driven high, both LED1 and LED2 are forced into torch mode or LED shutdown, depending on the logic state of Configuration Register 2 bit [0]. After a TX2 event, if the ENVM/TX2/GPIO2 pin is disengaged, and the TX2 Shutdown bit is set to force Torch mode, the LED current ramps back to the previous Flash current level. If the TX2 shutdown bit is programmed to force LED shutdown upon a TX2 event the Flags Register must be read to resume normal LED operation. Table 5, Figure 33, and Figure 34 detail the Functionality of the ENVM/TX2 input.

7.3.9.1 ENVM/TX2/GPIO2/INT as an Interrupt Output

In GPIO2 mode the ENVM/TX2/GPIO2 pin can be made to reflect the inverse of the LED Thermal Fault flag (bit[5] in the Flags Register). To configure the LM3554 for this feature:

set GPIO Register Bit [6] = 1 (NTC External Flag)

set GPIO Register Bit [3] = 1 (GPIO2 mode)

set GPIO Register Bit [4] = 1 (GPIO2 is an output)

set Configuration Register 1 Bit [3] = 1 (NTC mode)

When the voltage at the LEDI/NTC pin falls below V_{TRIP} (1.05 V typical), the LED Thermal Fault Flag (bit [5] in the Flags Register) is set, and the ENVM/TX2/GPIO2/INT pin is forced low. In this mode the interrupt can only be reset to the open-drain state by reading back the Flags register.

7.3.10 Indicator LED/Thermistor (LEDI/NTC)

The LEDI/NTC pin serves a dual function: either as an LED indicator driver or as a threshold detector for a negative temperature coefficient (NTC) thermistor.

7.3.10.1 LED Indicator Mode (LEDI)

LEDI/NTC is configured as an LED indicator driver by setting Configuration Register 1 bit [3] = (0) and Torch Brightness Register bits [1:0] = (0, 1), or Flash Brightness Register bits [1:0] = (0, 1). In Indicator mode there are 4 different current levels available (2.3 mA, 4.6 mA, 6.9 mA, 8.2 mA). Bits [7:6] of the Torch Brightness Register set the 4 different indicator current levels. The LEDI current source has a 1-V typical headroom voltage.

7.3.10.2 Thermal Comparator Mode (NTC)

Writing a 1 to Configuration Register 1 bit [3] disables the indicator current source and configures the LEDI/NTC pin as a detector for an NTC thermistor. In this mode LEDI/NTC becomes the negative input of an internal comparator with the positive input internally connected to a reference (V_{TRIP} = 1.05 V typical). Additionally, Configuration Register 2 bit [1] determines the action the device takes if the voltage at LEDI/NTC falls below V_{TRIP} (while the device is in NTC mode). With the Configuration Register 2 bit [1] = 0, the LM3554 is forced into torch mode when the voltage at LEDI/NTC falls below V_{TRIP}. With the Configuration Register 2 bit [1] = 1 the

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Feature Description (continued)

device shuts down the current sources when $V_{LEDI/NTC}$ falls below V_{TRIP}. When the LM3554 is forced from flash into torch (by $V_{LEDI/NTC}$ falling below V_{TRIP}), normal LED operation (during the same flash pulse) can only be re-started by reading from the Flags Register (0xD0) *and* ensuring the voltage at $V_{LEDI/NTC}$ is above V_{TRIP}. When VLEDI/NTC falls below VTRIP, and the Flags register is cleared, the LM3554 goes through a 250-µs deglitch time before the flash current falls to either torch mode or goes into shutdown.

7.3.11 Alternative External Torch (AET Mode)

Configuration Register 2 bit [2] programs the LM3554 for AET mode. With this bit set to 0 (default) TX1/TORCH is a transmit interrupt that forces torch mode only during a flash event. For example, if TX1/TORCH goes high during a flash event then the LEDs is forced into torch mode only for the duration of the timeout counter. At the end of the timeout counter the LEDs turn off.

With Configuration Register 2 bit [2] set to (1) the operation of TX1/TORCH becomes dependent on its occurrence relative to STROBE. In this mode if TX1/TORCH goes high first, then STROBE goes high, the LEDs are forced into torch mode with no timeout. In this mode if TX1/TORCH goes high after STROBE has gone high then the TX1/TORCH pin operates as a normal TX interrupt, and the LEDs turn off at the end of the timeout duration. (See LM3554 Timing Diagrams, Figure 35, and Figure 36.)

7.3.12 Input Voltage Monitor

The LM3554 has an internal comparator that monitors the voltage at IN, which can force the LED current into torch mode or into shutdown if V_{IN} falls below the programmable VIN monitor threshold. Bit 0 in the VIN Monitor Register (0x80) enables or disables this feature. When enabled, bits 1 and 2 program the four adjustable thresholds of 3.1 V, 3.2 V, 3.3 V, and 3.4 V. Bit 3 in Configuration Register 2 (0xF0) selects whether an undervoltage event forces torch mode or forces the LEDs off. See /Table 7 and /Table 9 for additional information.

There is a set 100-mV hysteresis for the input voltage monitor. When the input voltage monitor is active, and V_{IN} falls below the programmed VIN monitor threshold, the LEDs either turn off or their current is reduced to the programmed torch current setting. To reset the LED current to its previous level, two things must occur. First, V_{IN} must go at least 100 mV above the UVLO threshold and secondly, the Flags Register must be read back.

7.3.13 LM3554 Timing Diagrams

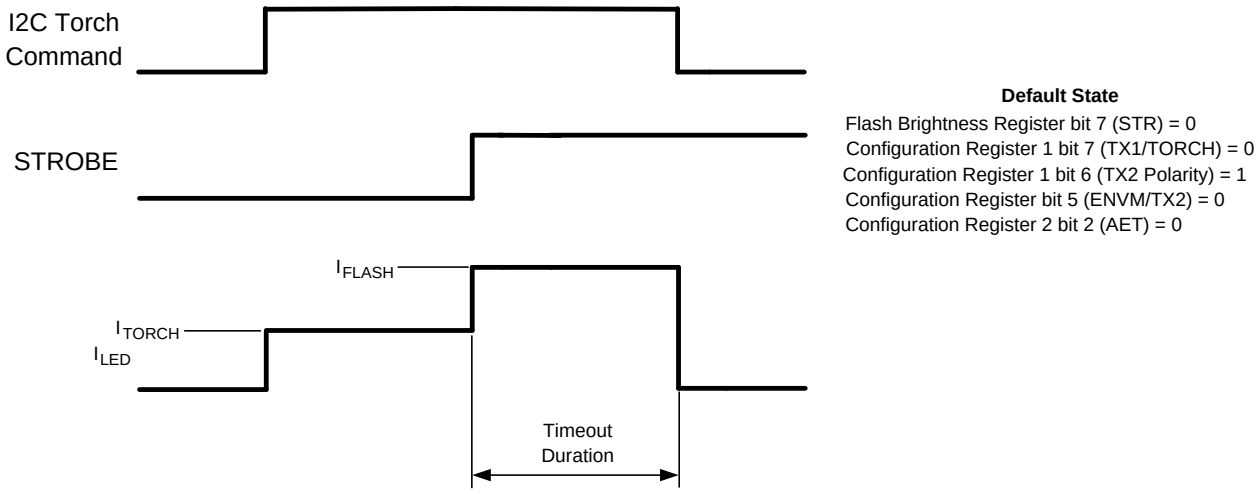

Figure 28. Normal Torch-to-Flash Operation (Default, Power On or LM3554 Reset State)

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Feature Description (continued)

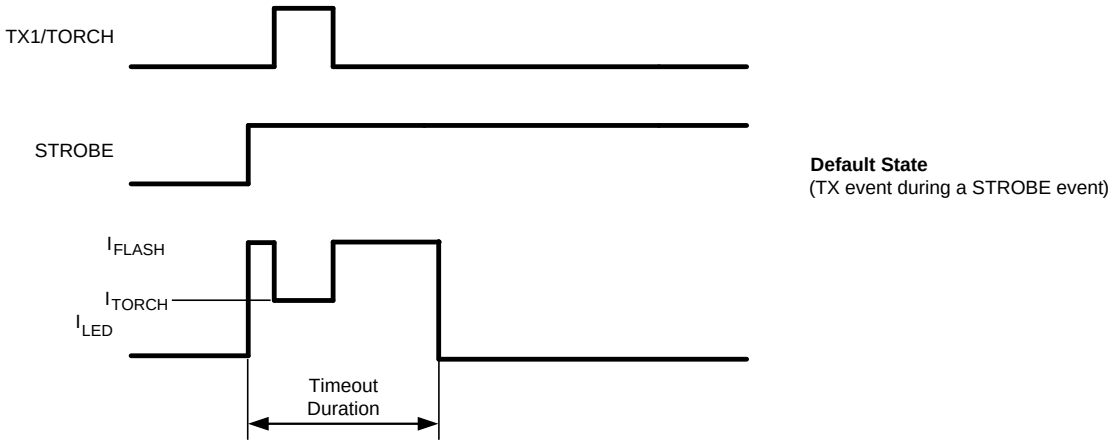


Figure 29. TX1 Event During A Flash Event (Default State,TX1/Torch is an Active High TX Input)

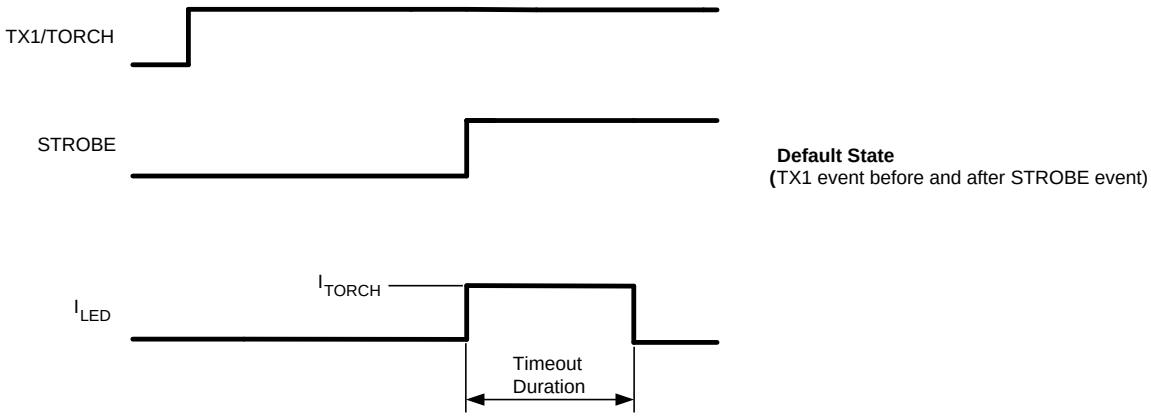


Figure 30. TX1 Event Before and After Flash Event (Default State, TX1/Torch is an Active High TX Input)

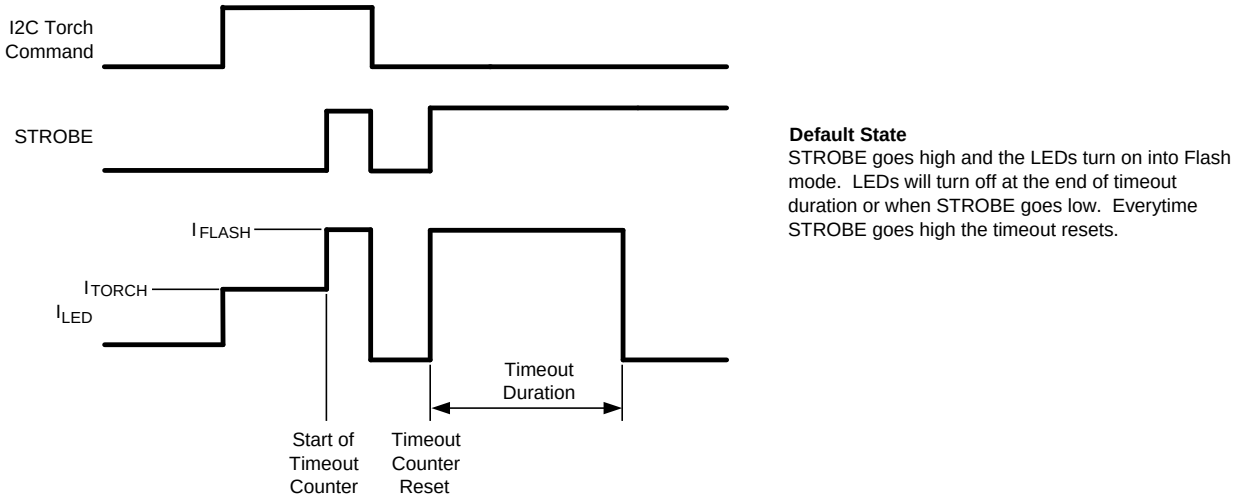
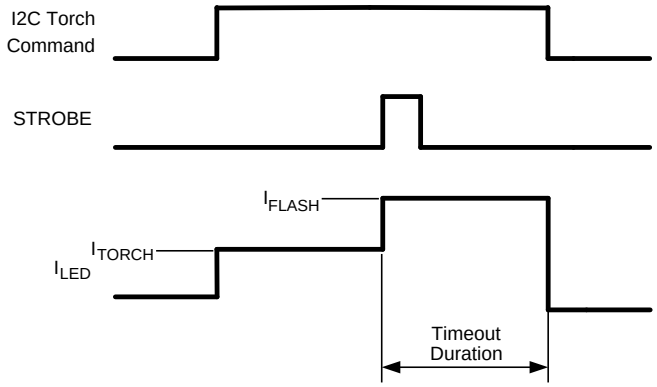


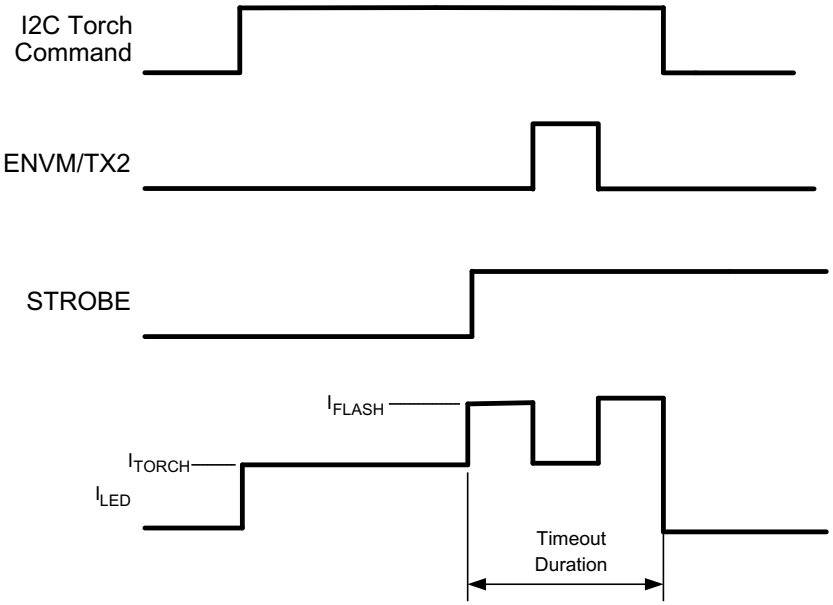
Figure 31. Strobe Input is Level Sensitive (Default State, STR Bit = 0)

Feature Description (continued)



Flash Brightness Register bit 7 (STR) = 1
STROBE goes high and the LEDs turn on into Flash mode. LEDs will stay on for the timeout duration even if STROBE goes low before.

Figure 32. Strobe Input is Edge Sensitive (STR Bit = 1)



ENVM/TX2 as a transmit interrupt
Configuration Register 1 bit 5 (ENVM/TX2) = 1
(ENVM/TX2 operates as a transmit interrupt)

Figure 33. ENVM/TX2 Pin is Configured as an Active High TX Input

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Feature Description (continued)

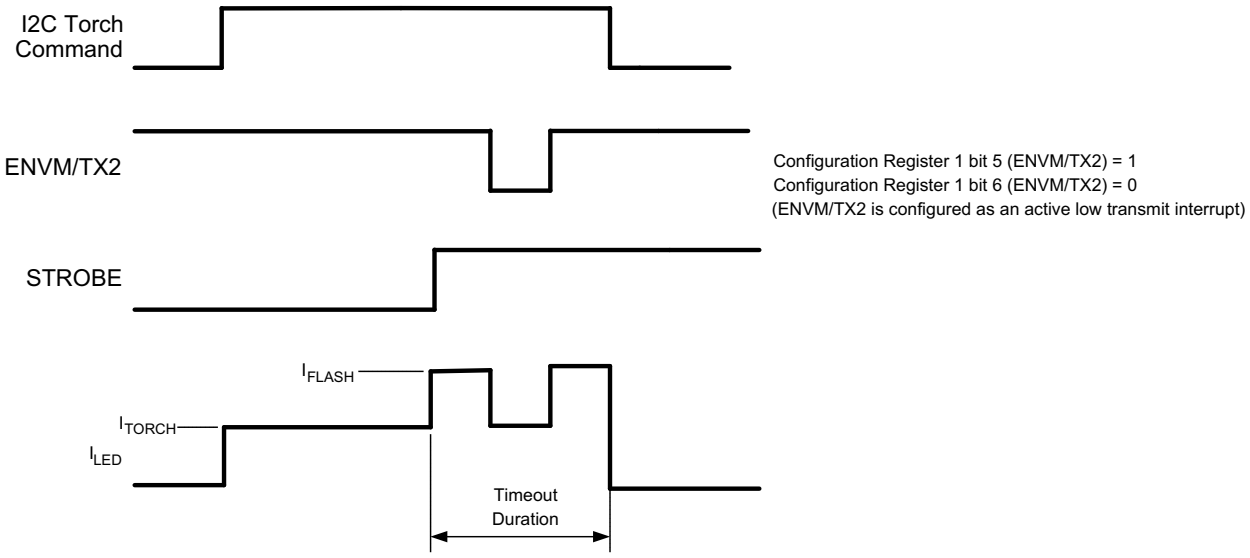

Figure 34. ENVM/TX2 Pin is Configured as an Active Low TX Input

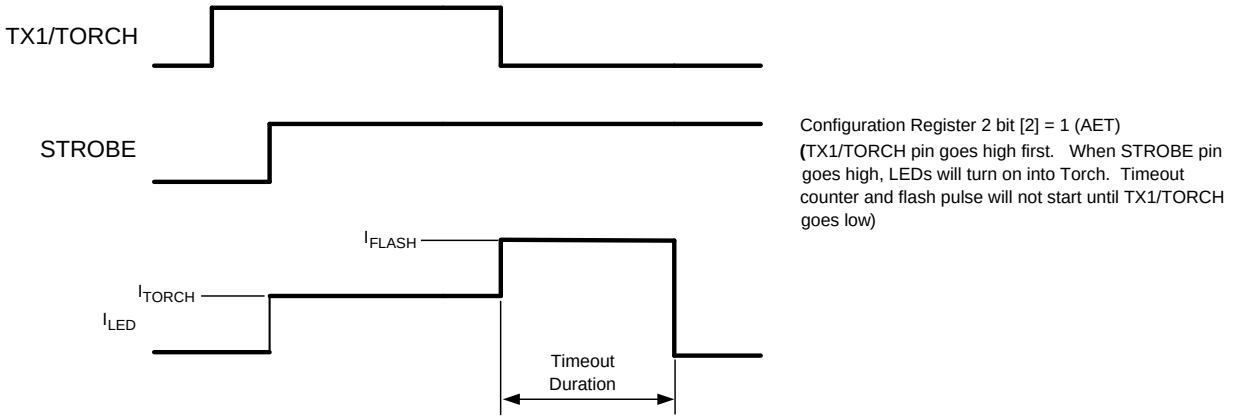

Figure 35. Alternative External Torch Mode (TX1/Torch Turns on Before Strobe)

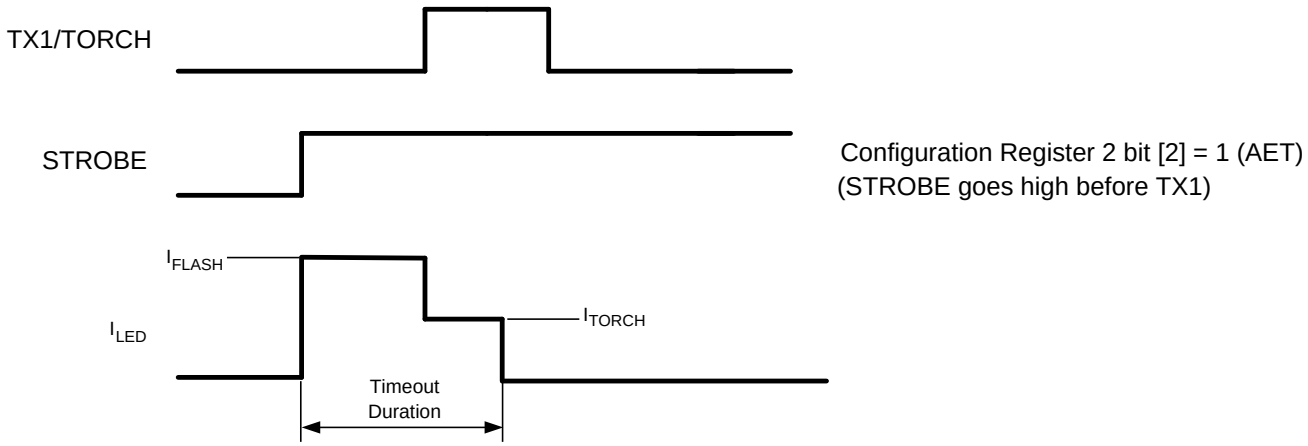

Figure 36. Alternative External Torch Mode (Strobe Goes High Before TX1/Torch, Same As Default With SEM = 0)

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Feature Description (continued)

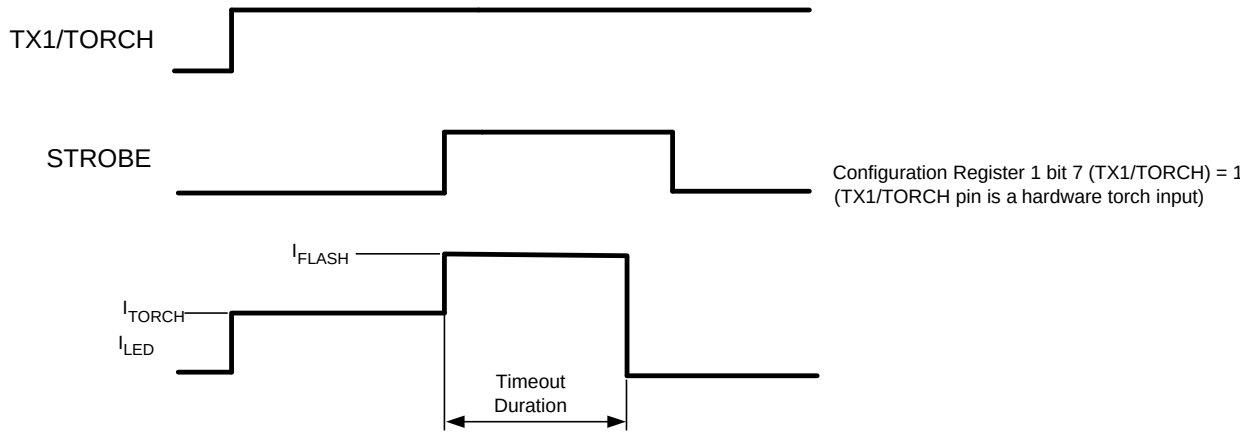

Figure 37. TX1/Torch Configured as a Hardware Torch Input

7.3.14 Flags Register and Fault Indicators

The Flags Register (0xD0) contains the Interrupt and fault indicators. Five fault flags are available in the LM3554. These include a thermal shutdown, an LED failure flag (LEDF) , a Timeout indicator Flag (TO), a LED Thermal Flag (NTC), and a VIN Monitor Flag. Additionally, two interrupt flag bits TX1 interrupt and TX2 interrupt indicate a change of state of the TX1/TORCH pin (TX1 mode) and ENVM/TX2 pin (TX2 mode). Reading back a 1 indicates the TX lines have changed state since the last read of the Flags Register. A read of the Flags Register resets these bits.

7.3.15 Thermal Shutdown

When the device die temperature reaches 150°C the boost converter shuts down, and the NFET and PFET turn off. Additionally, all three current sources (LED1, LED2, and LEDI) turn off. When the thermal shutdown threshold is tripped a 1 is written to bit [1] of the Flag Register (Thermal Shutdown bit). The LM3554 starts up again when the die temperature falls to below 135°C.

During heavy load conditions when the internal power dissipation in the device causes thermal shutdown, the device turns off and starts up again after the die temperature cools, resulting in a pulsed on/off operation. The OVT bit, however, is only written once. To reset the OVT bit pull HWEN low, power down the LM3554, or read the Flags Register.

7.3.16 LED Fault

The LED Fault flag (bit 2 of the Flags Register) reads back a 1 if the part is active in flash or torch mode and either LED1 or LED2 experience an open or short condition. An LED open condition is signaled if the OVP threshold is crossed at OUT while the device is in flash or torch mode. An LED short condition is signaled if the voltage at LED1 or LED2 goes below 500 mV while the device is in torch or flash mode.

There is a delay of 250 µs before the LEDF flag is valid on a LED short. This is the time from when VLED falls below the LED short threshold of 500 mV (typical) to when the fault flag is valid. There is a delay of 2 µs from when the LEDF flag is valid on an LED open. This delay is the time between when the OVP threshold is triggered and when the fault flag is valid. The LEDF flag can only be reset to 0 by pulling HWEN low, removing power to the LM3554, or reading the Flags Register.

7.3.17 Flash Timeout

The TO flag (bit [0] of the Flags Register) reads back a 1 if the LM3554 is active in flash mode and the timeout period expires before the flash pulse is terminated. The flash pulse can be terminated before the timeout period expires by pulling the STROBE pin low (with STR bit 0), or by writing a 0 to bit 0 or 1 of the Torch Brightness Register or the Flash Brightness Register. The TO flag is reset to 0 by pulling HWEN low, removing power to the LM3554 device, reading the Flags Register, or when the next flash pulse is triggered.

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Feature Description (continued)

7.3.18 LED Thermal Fault

The NTC flag (bit [5] of the Flags Register) reads back a 1 if the LM3554 is active in flash or torch mode, the device is in NTC mode, and the voltage at LEDI/NTC has fallen below V_{TRIP} (1.05 V typical). When this has happened and the LM3554 has been forced into torch or LED shutdown (depending on the state of Configuration Register 2 bit [1], the Flags Register must be read in order to place the device back in normal operation. (See *Thermal Comparator Mode (NTC)* for more details.)

7.3.19 Input Voltage Monitor Fault

The V_{IN} Monitor Flag (bit [6] of the Flag Register) reads back a 1 when the Input Voltage Monitor is enabled and V_{IN} falls below the programmed VIN Monitor threshold. This flag must be read back in order to resume normal operation after the LED current has been forced to Torch mode or turned off due to a VIN Monitor event.

7.3.20 TX1 And TX2 Interrupt Flags

The TX1 and TX2 interrupt flags (bits [3] and [4]) indicate a TX event on the TX1/TORCH and ENVM/TX2 pins. Bit 3 is read back a 1 if TX1/TORCH is in TX1 mode and the pin has changed from low to high since the last read of the Flags Register. Bit 4 reads back a 1 if ENVM/TX2 is in TX2 mode and the pin has had a TX event since the last read of the Flags Register. A read of the Flags Register automatically resets these bits.

The ENVM/TX2/GPIO2 pin, when configured in TX2 mode, has a TX event that can be either a high-to-low transition or a low-to-high transition depending on the setting of the TX2 polarity bit (see Table 6).

7.3.21 Light Load Disable

Configuration Register 1 bit [0] = 1 disables the light load comparator. With this bit set to 0 (default) the light load comparator is enabled. Light load mode only applies when the LM3554 is active in voltage-output mode. In LED mode the light load comparator is always disabled. When the light load comparator is disabled the LM3554 operates at a constant frequency down to I_{LOAD} = 0. Disabling light load can be useful when a more predictable switching frequency across the entire load current range is desired.

7.4 Device Functional Modes

7.4.1 Flash Mode

In flash mode the LED current sources (LED1 and LED2) each provide 16 different current levels from typically 34 mA to approximately 600 mA. The flash currents are set by writing to bits [6:3] of the Flash Brightness Resister. Flash mode is activated by either writing a (1, 1) to bits [1:0] of the Torch Brightness Register, writing a (1, 1) to bit [1:0] of the Flash Brightness Register, or by pulling the STROBE pin high. Once the Flash sequence is activated, both current sinks (LED1 and LED2) ramps up to the programmed Flash current by stepping through all Flash levels (16 µs/step) until the programmed current is reached.

7.4.2 Pass Mode

Once the output voltage charges up to V_{IN} – 150 mV the the device operates either in pass mode or boost mode. If the voltage difference between V_{OUT} and V_{LED} is less than 300 mV, the device transitions in boost mode. If the difference between V_{OUT} and V_{LED} is greater than 300 mV, the device operates in pass mode. In pass mode the boost converter stops switching, and the synchronous PFET turns fully on bringing V_{OUT} up to $V_{IN} – I_{IN} \times R_{PMOS}$ (R_{PMOS} = 150 mΩ). In pass mode the inductor current is not limited by the peak current limit. In this situation the output current must be limited to 2.5A.

7.4.3 Voltage-Output Mode

Bit 2 (VM) of the Torch Brightness Register, bit 2 (VM) of the Flash Brightness Register, or the ENVM input enables or disables the voltage-output mode. In voltage-output mode the device operates as a simple boost converter with two selectable voltage levels (4.5 V and 5 V). Write a 1 to bit 1 (OV) of Configuration Register 1 to set V_{OUT} to 5 V. Write a 0 to this bit to set V_{OUT} to 4.5 V. In voltage-output mode the LED current sources can continue to operate; however, the difference between V_{OUT} and V_{LED} is dropped across the current sources. (See *Maximum Output Power*.) In voltage-output mode when V_{IN} is greater than V_{OUT} the LM3554 device operates in pass mode (see *Pass Mode*).

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Device Functional Modes (continued)

At light loads the LM3554 switches over to a pulsed frequency mode operation (light load comparator enabled). In this mode the device only switches as necessary to maintain V_{OUT} within regulation. This mode provides a better efficiency due to the reduction in switching losses which become a larger portion of the total power loss at light loads.

7.5 Programming

7.5.1 I²C-Compatible Interface

7.5.1.1 Start and Stop Conditions

The LM3554 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

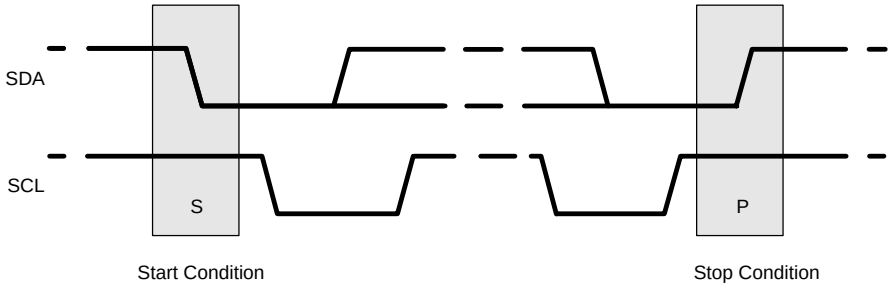

Figure 38. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. Figure 1 and Figure 39 show the SDA and SCL signal timing for the I²C-Compatible Bus. See *Electrical Characteristics* for timing values.

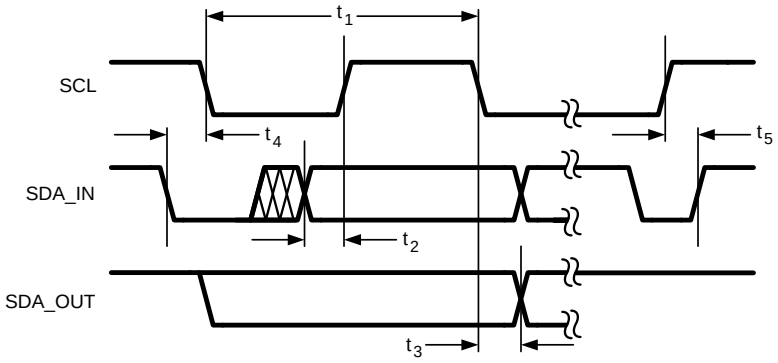

Figure 39. I²C-Compatible Timing

7.5.1.2 I²C-Compatible Chip Address

The device address for the LM3554 is 1010011 (53). After the START condition, the I²C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.

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Programming (continued)

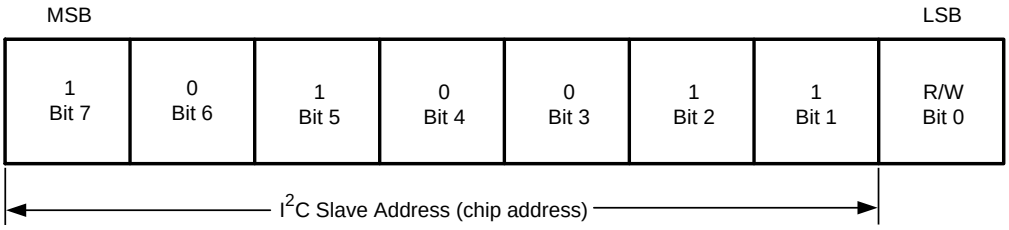


Figure 40. Device Address

7.5.1.3 Transferring Data

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master releases SDA (HIGH) during the 9th clock pulse (write mode). The LM3554 pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received.

7.6 Register Maps

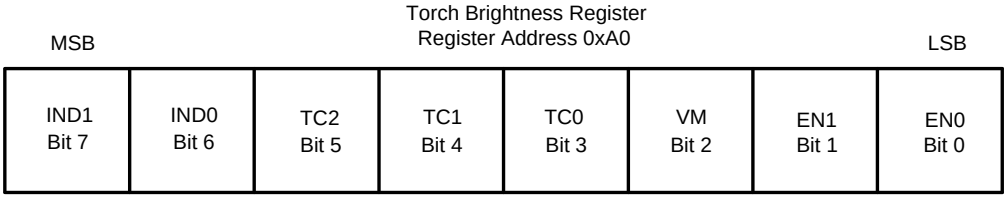
7.6.1 Register Descriptions

Table 1. LM3554 Internal Registers

REGISTER NAME	INTERNAL HEX ADDRESS	POWER ON OR RESET VALUE
Torch Brightness	0xA0	0x50
Flash Brightness	0xB0	0x68
Flash Duration	0xC0	0x4F
Flag Register	0xD0	0x40
Configuration Register 1	0xE0	0x42
Configuration Register 2	0xF0	0xF0
GPIO Register	0x20	0x80
VIN Monitor Register	0x80	0xF0

7.6.1.1 Torch Brightness Register

Bits [2:0] of the Torch Brightness Register, or bits [2:0] of the Flash Brightness Register place the device in shutdown or control the on/off state of Torch, Flash, the Indicator LED and the voltage-output mode (see Table 2). Writing to Torch Brightness Register bits [2:0] automatically updates the Flash Brightness Register bits [2:0]; writing to bits [2:0] of the Flash Brightness Register automatically updates bits [2:0] of the Torch Brightness Register. Bits [5:3] set the current level in Torch mode (see Table 2). Bits [7:6] set the LED Indicator current level (see Table 2).



Torch Brightness Register Description

Table 2. Torch Brightness Register Bit Settings

Bit 7 (IND1)	Bit 6 (IND0)	Bit 5 (TC2)	Bit 4 (TC1)	Bit 3 (TC0)	Bit 2 (VM)	Bit 1 (EN1)	Bit 0 (EN0)
Indicator Current Select Bits 00 = 2.3 mA 01 = 4.6 mA (**default state**) 10 = 6.9 mA 11 = 8.2 mA		Torch Current Select Bits 000 = 17 mA (34 mA total) 001 = 35.5 mA (71 mA total) **010 = 54 mA (108 mA total) default state** 011 = 73 mA (146mA total) 100 = 90 mA (180mA total) 101 = 109 mA (218 mA total) 110 = 128 mA (256 mA total) 111 = 147.5 mA (295 mA total)			Enable Bits 000 = Shutdown (**default**) 001 = Indicator Mode 010 = Torch Mode 011 = Flash Mode (bits reset at timeout) 100 = voltage-output mode 101 = Voltage Output + Indicator Mode 110 = Voltage Output + Torch Mode 111 = Voltage Output + Flash Mode (bits [1:0] are reset at end of timeout)		

7.6.1.2 Flash Brightness Register

Bits [2:0] of the Torch Brightness Register, or bits [2:0] of the Flash Brightness Register place the device in shutdown or control the on/off state of Torch, Flash, the Indicator LED and the voltage-output mode. Writing to the Flash Brightness Register bits [2:0] automatically updates the Torch Brightness Register bits [2:0]. Bits [6:3] set the current level in Flash mode (see Table 3). Bit [7] sets the STROBE Termination select bit (STR) (see Table 3).

Flash Brightness Register
Register Address 0xB0

MSB							LSB
STR Bit 7	FC3 Bit 6	FC2 Bit 5	FC1 Bit 4	FC0 Bit 3	VM Bit 2	EN1 Bit 1	EN0 Bit 0

Flash Brightness Register Description

Table 3. Flash Brightness Register Bit Settings

Bit 7 (STR)	Bit 6 (FC3)	Bit 5 (FC2)	Bit 4 (FC1)	Bit 3 (FC0)	Bit 2 (VM)	Bit 1 (EN1)	Bit 0 (EN0)
STROBE Edge or Level Select 0 = (Level Sensitive) When STROBE goes high, flash current turns on and remain on for the duration the STROBE pin is held high or when flash timeout occurs, whichever comes first.(**default**) 1 = (Edge Triggered) When STROBE goes high, flash current turns on and remain on for the duration of the Flash Timeout.	Flash Current Select Bits 0000 = 35.5 mA (71 mA total) 0001 = 73 mA (146 mA total) 0010 = 109 mA (218 mA total) 0011 = 147.5 mA (295 mA total) 0100 = 182.5 mA (365 mA total) 0101 = 220.5 mA (441 mA total) 0110 = 259 mA (518 mA total) 111 = 298 mA (596 mA total) 1000 =326 mA (652 mA total) 1001 = 364.5 mA (729 mA total) 1010 = 402.5 mA (805 mA total) 1011 = 440.5 mA (881 mA total) 1100 = 480 mA (960 mA total) **1101 = 518.5 mA (1037 mA total) Default** 1110 = 556.5 mA (1113 mA total) 1111 = 595.5 mA (1191 mA total)				Enable Bits 000 = Shutdown (**default**) 001 = Indicator mode 010 = Torch mode 011 = Flash mode (bits reset at timeout) 100 = Voltage-output mode 101 = Voltage output + indicator mode 110 = Voltage output + torch mode 111 = Voltage output + flash mode (bits [1:0] are reset at end of timeout)		

7.6.1.3 Flash Duration Register

Bits [4:0] of the Flash Duration Register set the Flash Timeout duration. Bits [6:5] set the switch current limit. Bit [7] defaults as a 1 and is not used (see Table 4).

Flash Duration Register
Register Address 0xC0

MSB							LSB
N/A Bit 7	CL1 Bit 6	CL0 Bit 5	T4 Bit 4	T3 Bit 3	T2 Bit 2	T1 Bit 1	T0 Bit 0

Flash Duration Register Description

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Table 4. Flash Duration Register Bit Settings

Bit 7 (Not used)	Bit 6 (CL1)	Bit 5 (CL0)	Bit 4 (T4)	Bit 3 (T3)	Bit 2 (T2)	Bit 1 (T1)	Bit 0 (T0)
Reads Back '0'	Current Limit Select Bits 00 = 1-A peak current limit 01 = 1.5-A peak current limit **10 = 2-A peak current limit (default)** 11 = 2.5-A peak current limit		Flash Timeout Select Bits 00000 = 32-ms timeout 00001 = 64-ms timeout 00010 = 96-ms timeout 00011 = 128-ms timeout 00100 = 160-ms timeout 00101 = 192-ms timeout 00110 = 224-ms timeout 00111 = 256-ms timeout 01000 = 288-ms timeout 01001 = 320-ms timeout 01010 = 352-ms timeout 01011 = 384-ms timeout 01100 = 416-ms timeout 01101 = 448-ms timeout 01110 = 480-ms timeout **01111 = 512-ms timeout (default)** 10000 = 544-ms timeout 10001 = 576-ms timeout 10010 = 608-ms timeout 10011 = 640-ms timeout 10100 = 672-ms timeout 10101 = 704-ms timeout 10110 = 736-ms timeout 10111 = 768-ms time-out 11000 = 800-ms timeout 11001 = 832-ms timeout 11010 = 864-ms timeout 11011 = 896-ms timeout 11100 = 928-ms timeout 11101 = 960-ms timeout 11110 = 992-ms timeout 11111 = 1024-ms timeout				

7.6.1.4 Flags Register

The Flags Register holds the status of the flag bits indicating LED Failure, Over-Temperature, the Flash Timeout expiring, VIN Monitor Fault, LED over temperature (NTC), and a TX interrupt. (See and Table 5.)

Flags Register
Register Address 0xD0

MSB LSB

V_{IN} Monitor Fault Bit 7	N/A Bit 6	LED Thermal Fault Bit 5	TX2 Interrupt Bit 4	TX1 Interrupt Bit 3	LED Fault Bit 2	Thermal Shutdown Bit 1	Flash Timeout Bit 0

Flags Register Description

Table 5. Flags Register Bit Settings

Bit 7 (V_{IN} Monitor Fault Fault)	Bit 6 (Unused)	Bit 5 (LED Thermal Fault)	Bit 4 (TX2 Interrupt)	Bit 3 (TX1 Interrupt)	Bit 2 (Led Fault)	Bit 1 (Thermal Shutdown)	Bit 0 (Flash Timeout)
0 = No Fault at VIN (**default**)	Not Used (Reads Back 1)	0 = LEDI/NTC pin is above V_{TRIP} (**default**)	0 = ENVM/TX2 has not changed state (**default**)	0 = TX1/TORCH has not changed state (**default**)	0 = Proper LED Operation (**default**)	0 = Die Temperature below Thermal Shutdown Limit (**default**)	0 = Flash TimeOut did not expire (**default**)
1 = Input Voltage Monitor is enabled and VIN has fallen below the programmed threshold		1 = LEDI/NTC has fallen below V_{TRIP}(NTC mode only)	1 = ENVM/TX2 has changed state (TX2 mode only)	1 = TX1/TORCH pin has changed state (TX1 mode only)	1 = LED Failed (Open or Short	1 = Die Temperature has crossed the Thermal Shutdown Threshold	1 = Flash TimeOut Expired

7.6.1.5 Configuration Register 1

Configuration Register 1 holds the light load disable bit, the voltage mode select bit (OV), the external flash inhibit bit, the control bit for the LEDI/NTC pin, the control bit for ENVM to TX2 mode, the polarity selection bit for the TX2 input, and the control bit for the TX1/TORCH bit (see and Table 6).

Configuration Register 1
Register Address 0xE0

MSB LSB

TX1/ TORCH Bit 7	TX2 Polarity Bit 6	ENVM/TX2 Bit 5	HYST Bit 4	LEDI/NTC Bit 3	Ext Flash Inhibit Bit 2	OV Bit 1	LL Disable Bit 0

Configuration Register 1 Description

Table 6. Configuration Register 1 Bit Settings

Bit 7 (Hardware Torch Mode Enable)	Bit 6 (TX2 Polarity)	Bit 5 (ENVM/TX2)	Bit 4 (N/A)	Bit 3 (LEDI/NTC)	Bit 2 (External Flash Inhibit)	Bit 1 (OV, Output Voltage Select)	Bit 0 (Disable Light Load)
0 = TX1/TORCH is a TX1 flash interrupt input **(default)**	0 = ENVM/TX2 pin is an active low Flash inhibit	0 = ENVM Mode The ENVM/TX2 pin is a logic input to enable Voltage Mode. A high on ENVM/TX2 forces voltage-output mode (**default**)	Reads Back '0'	0 = LEDI/NTC pin in Indicator mode **(default)**	0 = STROBE Input Enabled **(default)**	0 = Voltage Mode output voltage is 4.5 V	0 = Light load comparator is enabled. The LM3554 goes into PFM mode at light load **(default)**.
1 = TX1/TORCH pin is a hardware TORCH enable	1 = ENVM/TX2 pin is an active high Flash inhibit **(default)**	1 = TX2 Mode The ENVM/TX2 is a Power Amplifier Synchronization input. A high on ENVM/TX2 forces the LM3554 from flash to torch mode.		1 = LEDI/NTC pin in Thermal Comparator Mode. Indicator current is disabled.	1 = STROBE Input Disabled	1 = Voltage Mode output voltage is 5 V (**default**)	1 = Light load comparator is disabled. The LM3554 does not go into PFM mode at light load.

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7.6.1.6 Configuration Register 2

Configuration Register 2 contains the bits to select if TX2, NTC, and the VIN monitor force torch mode or force the flash LEDs into shutdown. Additionally, bit [2] (AET bit) selects the AET mode (see and Table 7).

Configuration Register 2
Register Address 0xF0

MSB							LSB
N/A Bit 7	N/A Bit 6	N/A Bit 5	N/A Bit 4	VIN Monitor Mode Bit 3	AET Mode Bit 2	NTC Shutdown Bit 1	TX2 Shutdown Bit 0

Configuration Register 2 Description

Table 7. Configuration Register 2 Bit Settings

Bit 7 (Not used)	Bit 6 (Not used)	Bit 5 (Not used)	Bit 4 (Not used)	Bit 3 (V_{IN} Monitor Shutdown)	Bit 2 (AET mode)	Bit 1 (NTC Shutdown)	Bit 0 (TX2 Shutdown)
Reads Back 1	Reads Back 1	Reads Back 1	Reads Back 1	0 = If IN drops below the programmed threshold and the VIN Monitor feature is enabled, the LED's are forced into Torch mode (**default**)	0 = Normal operation for TX1/TORCH high before STROBE (TX1 mode only) **default**	0 = LEDI/NTC pin going below V_{TRIP} forces the LEDs into Torch mode (NTC mode only) **default**	0 = TX2 event forces the LEDs into Torch mode (TX2 mode only) **default**
				1 = If IN drops below the programmed threshold and the VIN Monitor feature is enabled, the LED's turn off	1 = Alternative External Torch operation. TX1/TORCH high before STROBE forces Torch mode with no timeout (TX1 mode only)	1 = LEDI/NTC pin going below V_{TRIP} forces the LEDs into shutdown (NTC mode only)	1 = TX2 event forces the LEDs into shutdown (TX2 mode only)

7.6.1.7 GPIO Register

The GPIO register contains the control bits which change the state of the TX1/TORCH/GPIO1 pin and the ENVM/TX2/GPIO2 pin to general purpose I/O's (GPIO's). Additionally, bit[6] of this register configures the ENVM/TX2/GPIO2 as a hardware interrupt output reflecting the NTC flag bit in the Flags Register. and Table 8 describe the bit description and functionality of the GPIO register.

GPIO Register
Register Address 0x20

MSB							LSB
Not Used Bit 7	NTC External Flag Bit 6	Data Bit 5	Data Direction Bit 4	ENVM/ TX2/GPIO2 Bit 3	Data Bit 2	Data Direction Bit 1	TX1/TORCH/ GPIO1 Bit 0

GPIO Register Description

Table 8. GPIO Register Bit Settings

Bit 7 (Not Used)	Bit 6 (NTC External Flag)	Bit 5 (ENVM/TX2/GPIO2 data)	Bit 4 (ENVM/TX2/GPIO2 data direction)	Bit 3 (ENVM/TX2/GPIO2 Control)	Bit 2 (TX1/TORCH/GPIO1 data)	Bit 1 (TX1/TORCH/GPIO1 data direction)	Bit 0 (TX1/TORCH/GPIO1 Control)
Reads Back 1	0 = NTC External Flag mode is disabled (**default**)	This bit is the read or write data for the ENVM/TX2/GPIO2 pin in GPIO mode (**default is 0**)	0 = ENVM/TX2/GPIO2 is a GPIO Input (**default**)	0 = ENVM/TX2/GPIO2 is configured according to the Configuration Register bit 5 (**default**)	This bit is the read or write data for the TX1/TORCH/GPIO1 pin in GPIO mode (**default is 0**)	0 = TX1/TORCH/GPIO1 is a GPIO input (**default**)	0 = TX1/TORCH/GPIO1 pin is configured as an active low reset input (**default**)
	1 = When ENVM/TX2/GPIO2 is configured as a GPIO output the ENVM/TX2/GPIO2 pin pulls low when the LED Thermal Fault Flag is set		1 = ENVM/TX2/GPIO2 is a GPIO Output	1 = ENVM/TX2/GPIO2 is configured as a GPIO		1 = TX!/TORCH/GPIO1 is an output	1 = TX1/TORCH/GPIO1 pin is configured as a GPIO

7.6.1.8 V_{IN} Monitor Register

The V_{IN} Monitor Register controls the on/off state of the V_{IN} Monitor comparator as well as selects the 4 programmable thresholds. and Table 9 describe the bit settings of the V_{IN} Monitor feature.

V_{IN} Monitor Register
Register Address 0x80

MSB							LSB
N/A Bit 7	N/A Bit 6	N/A Bit 5	N/A Bit 4	N/A Bit 3	V_{IN} Threshold Bit 2	V_{IN} Threshold Bit 1	V_{IN} Monitor Enable Bit 0

V_{IN} Monitor Register Description

Table 9. V_{IN} Monitor Register Bit Settings

Bit 7 (Not used)	Bit 6 (Not used)	Bit 5 (Not used)	Bit 4 (Not used)	Bit 3 (Not used)	Bit 2 (VIN Threshold)	Bit 1 (V_{IN} Threshold)	Bit 0 (V_{IN} Monitor Enable)
Reads Back 1	Reads Back 1	Reads Back 1	Reads Back 1	Reads Back '0'	00 = 3.1-V threshold (V_{IN} falling) **Default** 01=3.2-V threshold (V_{IN} falling) 10 = 3.3-V threshold (V_{IN} falling) 11 = 3.4-V threshold (V_{IN} falling)		0 = V_{IN} Monitoring Comparator is disabled (**default**)
							1 = V_{IN} Monitoring Comparator is enabled.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3554 is a dual-string white-LED driver for LED camera flash applications. The dual high-side current sources allow for grounded cathode LEDs. The integrated boost provides the power for the current sources and can source up to 1.2 A from a single-cell Li+ voltage range.

8.2 Typical Application

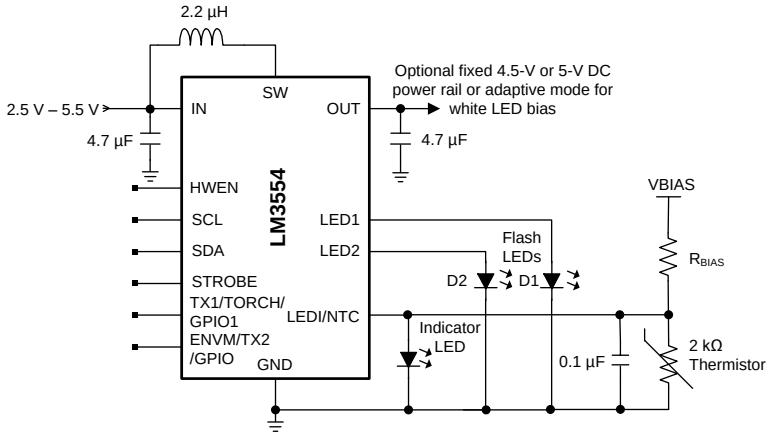

Figure 41. LM3554 Typical Application

8.2.1 Design Requirements

For typical LM3554 device applications, use the parameters listed in Table 10.

Table 10. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.5 V
Programmable output voltage	4.5 V or 5 V
Programmable output current	37.5 mA to 1.2 A

Table 11. Application Circuit Component List

COMPONENT	MANUFACTURER	VALUE	PART NUMBER	SIZE (mm)	RATING
L	TOKO	2.2 µH	FDSE0312-2R2M	3 × 3 × 1.2	2.3 A (0.2 Ω)
COUT	Murata	4.7 µF/10 µF	GRM188R60J475M, or GRM188R60J106M	0603 (1.6 × 0.8 ×0.8)	6.3 V
CIN	Murata	4.7 µF	GRM185R60J475M	0603 (1.6 × 0.8 × 0.8)	6.3 V
LEDs	Lumiled		LXCL-PWF4		1.5 A

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8.2.2 Detailed Design Procedure

8.2.2.1 Output Capacitor Selection

The LM3554 is designed to operate with a at least a 4.7-µF ceramic output capacitor in LED mode and a 10-µF output capacitor in voltage-output mode. When the boost converter is running the output capacitor supplies the load current during the boost converters on-time. When the NMOS switch turns off the inductor energy is discharged through the internal PMOS switch supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on time and a rise in the output voltage during the off time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

For proper LED operation the output capacitor must be at least a 4.7-µF ceramic (10-µF in voltage-output mode). Larger capacitors such as 10 µF or 22 µF can be used if lower output voltage ripple is desired. To estimate the output voltage ripple considering the ripple due to capacitor discharge (ΔV_Q) and the ripple due to equivalent series resistance (ESR) of the capacitor (ΔV_{ESR}) use Equation 1 and Equation 2:

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_Q = \frac{I_{LED} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times C_{OUT}} \quad (1)$$

The output voltage ripple due to the output capacitors ESR is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{I_{LED} \times V_{OUT}}{V_{IN}} \right) + \Delta I_L$$

where

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (2)$$

In ceramic capacitors the ESR is very low, thus the assumption is that that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR. Table 12 lists different manufacturers for various output capacitors and their case sizes suitable for use with the LM3554.

8.2.2.2 Input Capacitor Selection

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the device boost converter switching and reduces noise on the devices input terminal that can feed through and disrupt internal analog signals. In the Figure 41 a 4.7-µF ceramic input capacitor works well. It is important to place the input capacitor as close to the device input (IN) terminals as possible. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents. Table 12 lists various input capacitors that or recommended for use with the LM3554.

Table 12. Recommended Input/Output Capacitors (X5R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE (mm)	VOLTAGE RATING
TDK Corporation	C1608JB0J475K	4.7 µF	0603 (1.6 × 0.8 × 0.8)	6.3 V
TDK Corporation	C1608JB0J106M	10 µF	0603 (1.6 × 0.8 × 0.8)	6.3 V
TDK Corporation	C2012JB1C475K	4.7 µF	0805 (2 ×1.25 ×1.25)	16 V
TDK Corporation	C2012JB1A106M	10 µF	0805 (2 ×1.25 ×1.25)	10 V
TDK Corporation	C2012JB0J226M	22 µF	0805 (2 ×1.25 ×1.25)	6.3 V
Murata	GRM188R60J475KE19	4.7 µF	0603 (1.6 × 0.8 × 0.8)	6.3 V
Murata	GRM21BR61C475KA88	4.7 µF	0805 (2 ×1.25 ×1.25)	16 V
Murata	GRM21BR61A106KE19	10 µF	0805 (2 ×1.25 ×1.25)	10 V
Murata	GRM21BR60J226ME39L	22 µF	0805 (2 ×1.25 ×1.25)	6.3 V

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8.2.2.3 Inductor Selection

The LM3554 is designed to use a 2.2-µH inductor. Table 13 lists various inductors and their manufacturers that can work well with the LM3554. When the device is boosting (V_{OUT} > V_{IN}) the inductor is typically the biggest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor must be greater than the maximum operating peak current of the LM3554. This prevents excess efficiency loss that can occur with inductors that operate in saturation and prevents over heating of the inductor and possible damage. For proper inductor operation and circuit performance ensure that the inductor saturation and the peak current limit setting of the LM3554 is greater than I_{PEAK} can be calculated by:

$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad \text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

where

- f_{SW} = 2 MHz
- η can be found in *Typical Characteristics* (3)

Table 13. Recommended Inductors

MANUFACTURER	L	PART NUMBER	DIMENSIONS (L×W×H)(mm)	I_{SAT}
TOKO	2.2 µH	FDSE0312-2R2M	3 × 3 ×1.2	2 A
TDK	2.2 µH	VLS252012T-2R2M1R3	2 × 2.5 ×1.2 mm	1.5 A
Coilcraft	2. 2µH	LPS4018-222ML	3.9 × 3.9 × 1.7 mm	2.3 A

8.2.2.4 NTC Thermistor Selection

NTC thermistors have a temperature to resistance relationship of:

$$R(T) = R_{25°C} \times e^{\left[\beta\left(\frac{1}{T°C+273} - \frac{1}{298}\right)\right]}$$

where

- β is given in the thermistor datasheet
- R_{25C} is the thermistors value at 25°C (4)

Figure 43 is chosen so that it is equal to:

$$R3 = \frac{R_{T(TRIP)} (V_{BIAS} - V_{TRIP})}{V_{TRIP}}$$

where

- $R(T)_{TRIP}$ is the thermistor value at the temperature trip point
- V_{BIAS} is shown in Figure 43
- V_{TRIP} = 1.05V (typical) (5)

Choosing R3 here gives a more linear response around the temperature trip voltage. For example, with V_{BIAS} = 2.5 V, a thermistor whose nominal value at 25°C is 100 kΩ and a β = 4500 K, the trip point is chosen to be 93°C. The value of R(T) at 93°C is:

$$R(T) = 100\,k\Omega \times e^{\left[\beta\left(\frac{1}{93+273} - \frac{1}{298}\right)\right]} = 6.047\,k\Omega$$

$$\text{R3 is then: } \frac{6.047\,k\Omega \times (2.5V - 1V)}{1V} = 9.071\,k\Omega \quad (6)$$

Figure 42 shows the linearity of the thermistor resistive divider of the previous example.

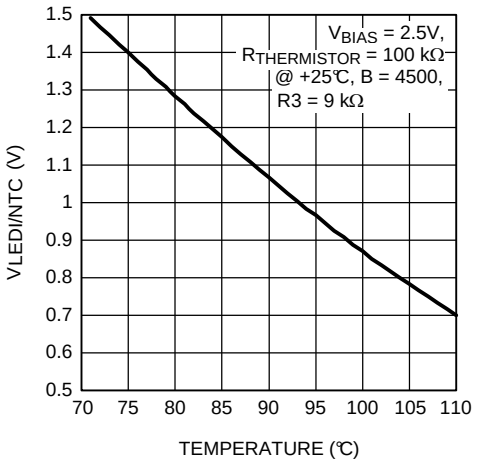

Figure 42. Thermistor Resistive Divider Response vs Temperature

Another useful equation for the thermistor resistive divider is developed by combining the equations for R3, and R(T) and solving for temperature. This is shown in Equation 7:

$$T(°C) = \frac{\beta \times 298°C}{298°C \times LN\left[\frac{V_{TRIP} \times R3}{(V_{BIAS} - V_{TRIP}) \times R_{25°C}}\right] + \beta} - 273°C \quad (7)$$

Using, for example, Excel® spreadsheet software, different curves for the temperature trip point T (°C) can be created vs R3, Beta, or V_{BIAS} in order to help better choose the thermal components for practical values of thermistors, series resistors (R3), or reference voltages V_{BIAS}.

Programming bit [3] of the Configuration Register with a 1 selects thermal comparator mode making the LEDI/NTC pin a comparator input for flash LED thermal sensing. Figure 43 shows the internal block diagram of the thermal sensing circuit which is OR'd with both the TX1 and ENVM/TX2 (TX2 mode) to force the LM3554 from flash to torch mode. This is intended to prevent LED overheating during flash pulses.

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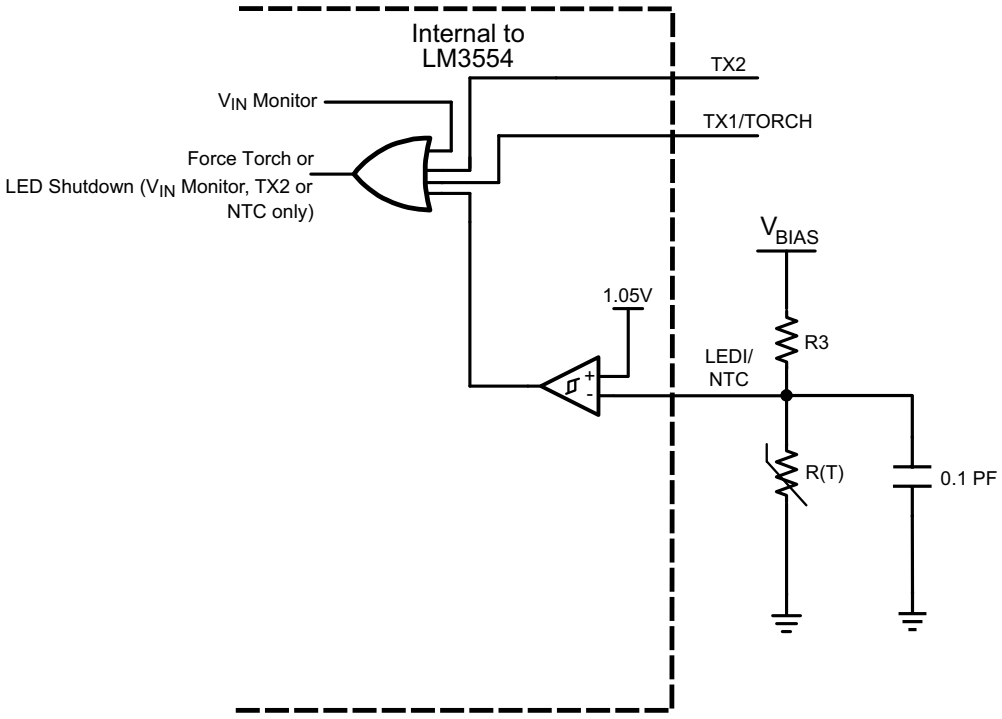

Figure 43. Thermistor Voltage Divider and Sensing Circuit

8.2.2.5 NTC Thermistor Placement

The termination of the thermistor must be done directly to the cathode of the flash LED in order to adequately couple the heat from the LED into the thermistor. Consequently, the noisy environment generated from the boost converter switching can introduce noise from GND into the thermistor sensing input. To filter out this noise it is necessary to place a 0.1-µF or larger ceramic capacitor close to the LEDI/NTC pin. The filter capacitor's return must also connect with a low-impedance trace, as close to the PGND pin of the device as possible.

8.2.2.6 Maximum Load Current (Voltage Mode)

Assuming the power dissipation in the LM3554 and the ambient temperature are such that the device does not hit thermal shutdown, the maximum load current as a function of I_{PEAK} is:

$$I_{LOAD} = \frac{(I_{PEAK} - \Delta I_L) \times \eta \times V_{IN}}{V_{OUT}} \quad (8)$$

where

- η is efficiency and is found in the efficiency curves in the *Typical Characteristics*

and

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (9)$$

Figure 44 shows the theoretical maximum output current vs theoretical efficiency at different input and output voltages using Equation 8 and Equation 9 for ΔI_L and I_{LOAD} with a peak current of 2.5 A. Figure 44 represents the theoretical maximum output current (for the LM3554 in voltage-output mode) that the device can deliver just before hitting current limit.

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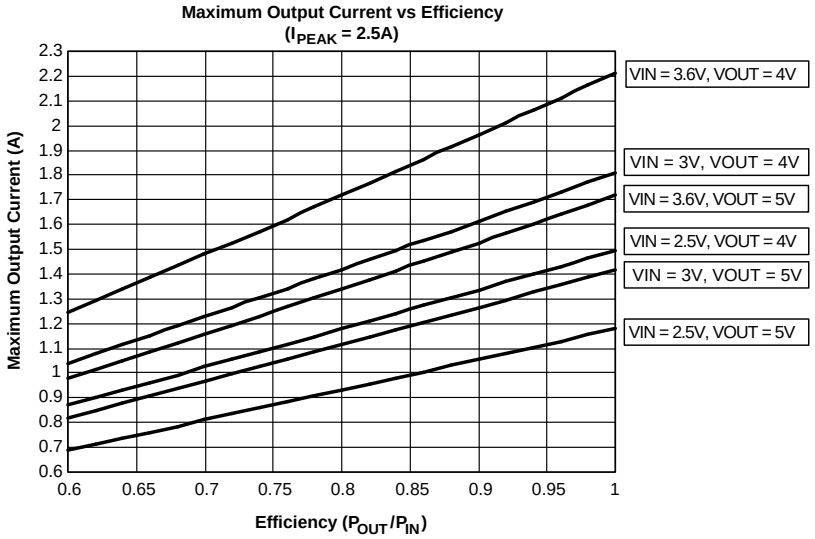

Figure 44. LM3554 Maximum Output Current

8.2.2.7 Maximum Output Power

Output power is limited by three things: the peak current limit, the ambient temperature, and the maximum power dissipation in the package. If the LM3554's die temperature is below the absolute maximum rating of 125°C, the maximum output power can be over 6 W. However, any appreciable output current causes the internal power dissipation to increase and therefore increase the die temperature. This can be additionally compounded if the LED current sources are operating while the device is in voltage-output mode because the difference between V_{OUT} and V_{LED} is dropped across the current sources. Any circuit configuration must ensure that the die temperature remains below 125°C taking into account the ambient temperature derating.

8.2.2.7.1 Voltage-Output Mode

In voltage-output mode the total power dissipated in the LM3554 can be approximated as:

$$P_{DISS} = P_N + P_P + P_{LED1} + P_{LED2} + P_{IND}$$

where

- P_N is the power lost in the NFET
- P_P is the PFET power loss
- P_{LED1}, P_{LED2}, and P_{IND} are the losses across the current sink (10)

An approximate calculation of these losses gives:

$$P_{DISS} = \left[\left(\frac{(V_{OUT} - V_{IN}) \times V_{OUT}}{V_{IN}^2} \right) \times I_{LOAD}^2 \times R_{NFET} + \left(\frac{V_{OUT}}{V_{IN}} \right) \times I_{LOAD}^2 \times R_{PFET} + (V_{OUT} - V_{LED}) \times I_{LED} + (V_{OUT} - V_{IND}) \times I_{IND} \right]$$

$$I_{LOAD} = I_{OUT} + I_{LED} + I_{IND}$$

$$I_{LED} = I_{LED1} + I_{LED2} \quad (11)$$

Equation 11 consider the average current through the NFET and PFET. The actual power losses are higher due to the RMS currents and the quiescent power into IN. These, however, can give a decent approximation.

8.2.2.7.2 LED Boost Mode

In LED mode with $V_{OUT} > V_{IN}$ the device boost converter switches and make $V_{OUT} = V_{LED} + 0.3$ V. In this situation the total power dissipated in the LM3554 is approximated as:

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$$P_{DISS} = \left[\left(\frac{(V_{LED} + 0.3V - V_{IN}) \times V_{LED} + 0.3V)}{V_{IN}^2} \right) \times I_{LOAD}^2 \times R_{NFET} + \left(\frac{V_{LED} + 0.3V}{V_{IN}} \right) \times I_{LOAD}^2 \times R_{PFET} + 0.3V \times I_{LED} + (V_{LED} + 0.3V - V_{IND}) \times I_{IND} \right]$$

$$I_{LOAD} = I_{LED} + I_{IND}$$

$$I_{LED} = I_{LED1} + I_{LED2} \quad (12)$$

8.2.2.7.3 LED Pass Mode

In LED mode with $V_{IN} - I_{LOAD} \times R_{PFET} > V_{LED} + 0.3$ V, the LM3554 operates in pass mode. In this case, the NFET is off, and the PFET is fully on. The difference between $V_{IN} - I_{LOAD} \times R_{PMOS}$ and V_{LED} are dropped across the current sources. In this situation the total power dissipated in the LM3554 is approximated as:

$$P_{DISS} = [I_{LOAD}^2 \times R_{PFET} + (V_{IN} - R_{PFET} \times I_{LOAD} - V_{LED}) \times I_{LED} + (V_{IN} - R_{PFET} \times I_{LOAD} - V_{IND}) \times I_{IND}]$$

$$I_{LOAD} = I_{LED} + I_{IND}$$

$$I_{LED} = I_{LED1} + I_{LED2} \quad (13)$$

Once the total power dissipated in the LM3554 is calculated the ambient temperature and the thermal resistance of the 16-pin DSBGA (YFQ package) are used to calculate the total die temperature (or junction temperature T_J).

As an example, assume the LM3554 is operating at V_{IN} = 3.6 V and configured for voltage-output mode with V_{OUT} = 5 V and I_{OUT} = 0.7 A. The LED currents are then programmed in torch mode with 150 mA each at V_{LED} = 3.6 V. Additionally, the indicator LED has 10 mA at V_{IND} = 3.6 V. Using Equation 12 and Equation 13 above, the approximate total power dissipated in the device is:

$$P_{DISS} = 139 \text{ mW} + 357 \text{ mW} + 420 \text{ mW} + 14 \text{ mW} = 930 \text{ mW} \quad (14)$$

The die temperature approximation is:

$$T_J = 0.93\text{W} \times 75.8°\text{C/W} + 25°\text{C} = 95.5°\text{C} \quad (15)$$

In this case the device can operate at these conditions. If then the ambient temperature is increased to 85°C, the die temperature would be 140.8°C; thus, the die temperature would be above the absolute maximum ratings, and the load current would need to be scaled back. This example demonstrates the steps required to estimate the amount of current derating based upon operating mode, circuit parameters, and the device's junction-to-ambient thermal resistance. In this example a thermal resistance of 75.8°C/W was used (JESD51-7 standard). Because thermal resistance from junction-to-ambient is largely PCB layout dependent, the actual number used likely may be different and must be taken into account when performing these calculations.

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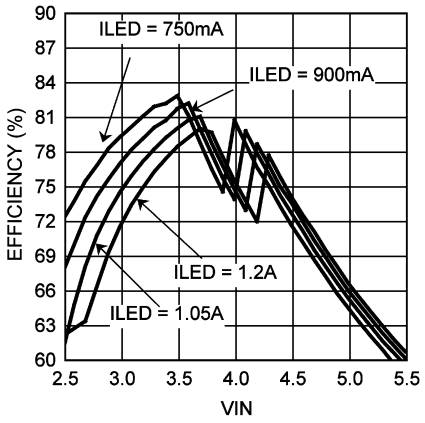
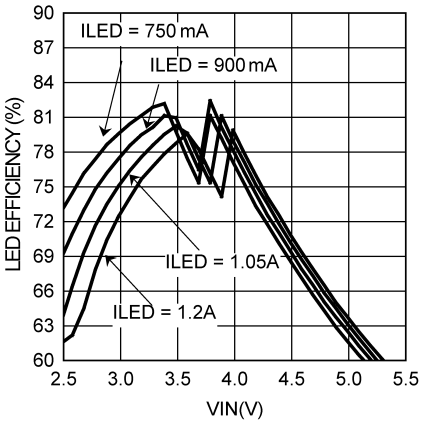
8.2.3 Application Curves



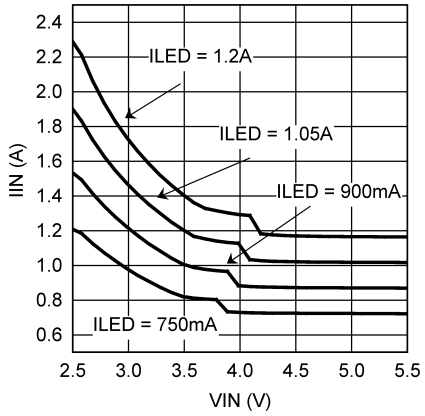
Single LED

Figure 45. LED Efficiency vs V_{IN}



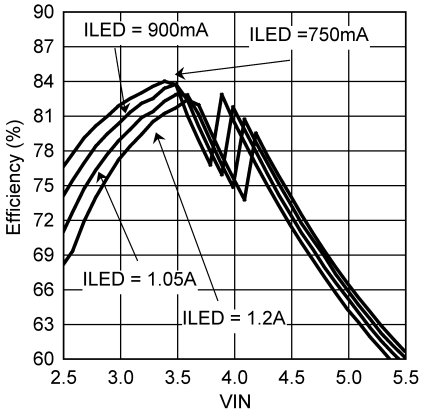
Dual LEDs

Figure 46. LED Efficiency vs V_{IN}



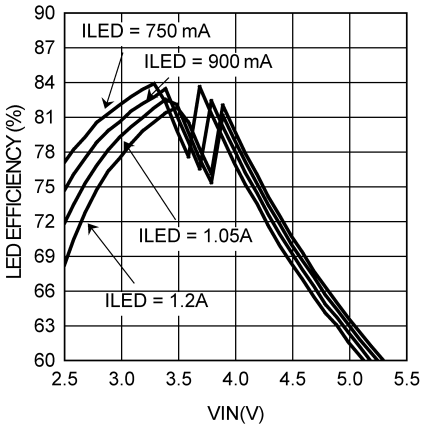
Single LED

Figure 47. Input Current vs V_{IN}



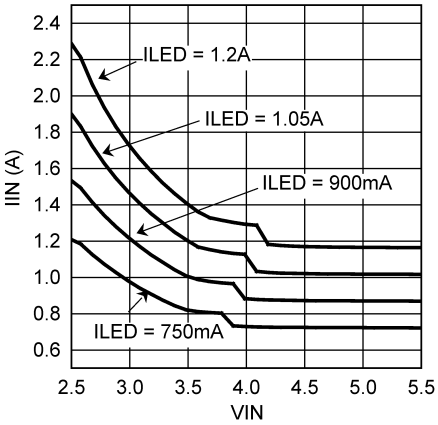
Single LED L = Coilcraft LPS4018-222

Figure 48. LED Efficiency vs V_{IN}



Dual LEDs L = Coilcraft LPS4018-222

Figure 49. LED Efficiency vs V_{IN}



Single LED L = Coilcraft LPS4018-222

Figure 50. Input Current vs V_{IN}

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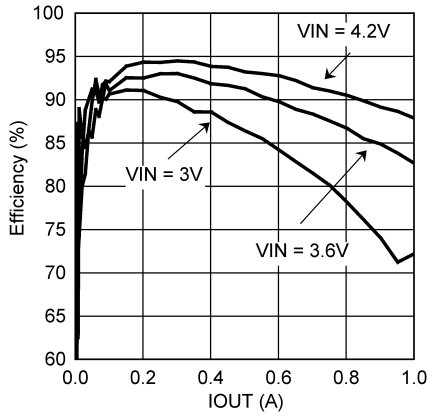
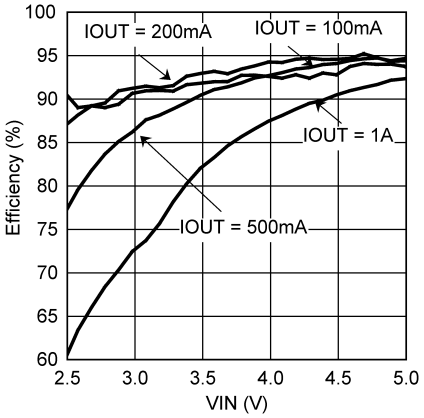


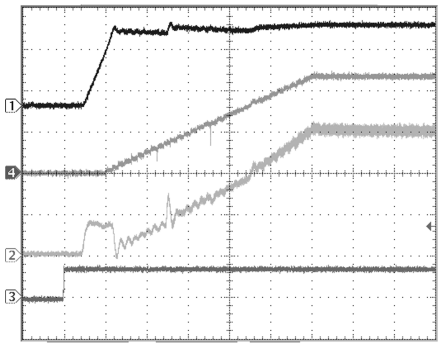
V_{OUT} = 5 V Voltage-Output Mode

Figure 51. Efficiency vs I_{OUT}



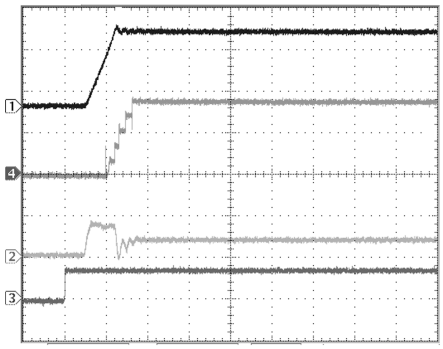
V_{OUT} = 5 V Voltage-Output Mode

Figure 52. Efficiency vs V_{IN}



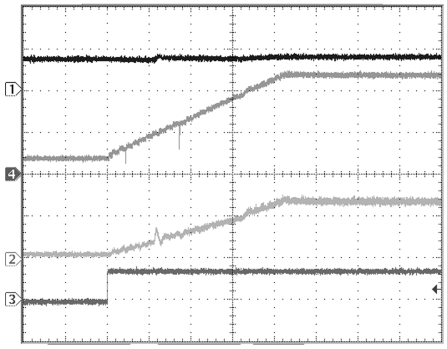
Time Base: 100 µs/div I_{FLASH} = 1.2 A Single LED
Ch 1: V_{OUT} (2 V/div) Ch 2: I_L (500 mA/div)
Ch 4: I_{LED} (500 mA/div) Ch 3: STROBE (5 V/div)

Figure 53. Start-Up Into Flash Mode



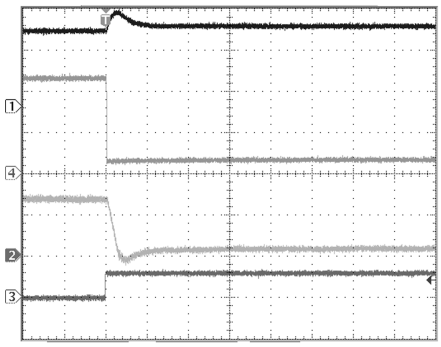
Time Base: 100 µs/div I_{TORCH} = 180 mA
90-mA Torch Setting Single LED
Chl 1: V_{OUT} (2 V/div) Ch 2: I_L (500 mA/div)
Ch 4: I_{LED} (100 mA/div) Ch 3: TX1 (5 V/div)

Figure 54. Start-Up Into Hardware Torch Mode



Time Base: 100 µs/div I_{FLASH} = 1.2 A I_{TORCH} = 295 mA
Ch 1: V_{OUT} (5 V/div) Ch 2: I_L (1 A/div) Single LED
Ch 4: I_{LED} (500 mA/div) Ch 3: STROBE (5 V/div)

Figure 55. Torch Mode to Flash Mode Transition



Time Base: 20 µs/div I_{FLASH} = 1.2 A I_{TORCH} = 180 mA
Ch 1: V_{OUT} (2 V/div) Ch 2: I_L (1 A/div) Single LED
Ch 4: I_{LED} (500 mA/div) Ch 3: TX1 (5 V/div)

Figure 56. TX1 Interrupt Operation, TX1 Rising

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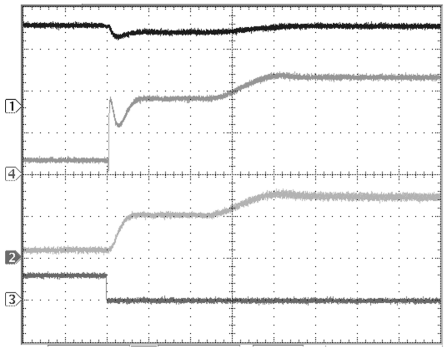
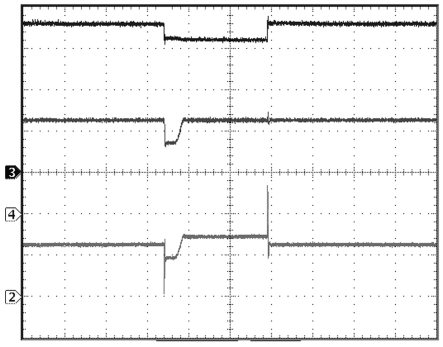


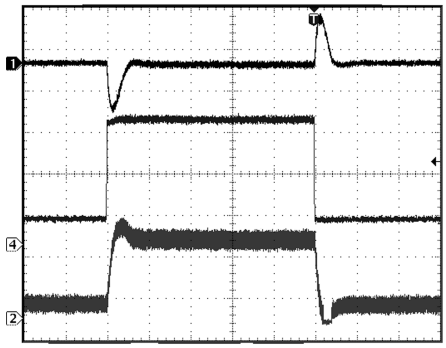
Time Base: 20 µs/div I_{FLASH} = 1.2 A I_{TORCH} = 180 mA
Ch 1: V_{OUT} (2 V/div) Ch 2: I_L (1 A/div) Single LED
Ch 4: I_{LED} (500 mA/div)
Ch 3: TX1 (5 V/div)

Figure 57. TX1 Interrupt Operation, TX1 Falling



Time Base: 400 µs/div I_{FLASH} = 1.2 A Single LED
Ch 3: V_{IN} (5 V/div) Ch 2: I_L (1 A/div)
Ch 4: I_{LED} (500 mA/div)

Figure 58. Line Transient (LED Mode)

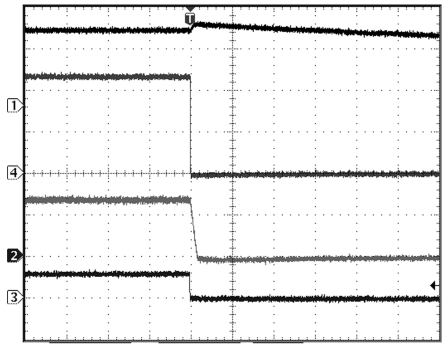


Time Base: 40 µs/div V_{IN} = 3.6 V V_{OUT} = 5 V
Ch 1: V_{OUT} (500 mV/div) Ch 2: I_L (500 mA/div)
Ch 4: I_{OUT} (500 mA/div)

Figure 59. Load Transient (Voltage Output Mode)

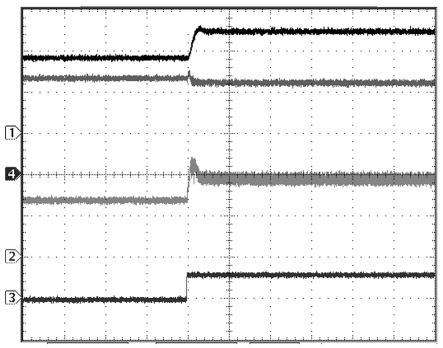
Time Base: 200 µs/div V_{OUT} = 5 V I_{OUT} = 500 mA
Ch 1: V_{OUT} = (5 V/div) Ch 2: $I_L + I_{IN}$ (500 mA/div)
Ch 3 (Top Trace): V_{IN} (1 V/div)

Figure 60. Line Transient (Voltage Output Mode)



Time Base: 20 µs/div I_{LED} = 1.2 A Single LED
Ch 1: V_{OUT} (2 V/div) Ch 3: HWEN (5 V/div)
Ch 4: I_{LED} (500 mA/div)

Figure 61. Flash Pulse to HWEN Low



Time Base: 100 µs/div V_{OUT} = 5 V I_{LED} = 1.2 A
Ch 1: V_{OUT} (2 V/div) Ch 2: I_L (1 A/div) Single LED
Ch 4: I_{LED} (500 mA/div) Ch 3: ENVM (5 V/div)

Figure 62. Flash Pulse to Flash Pulse + V_{OUT} Mode

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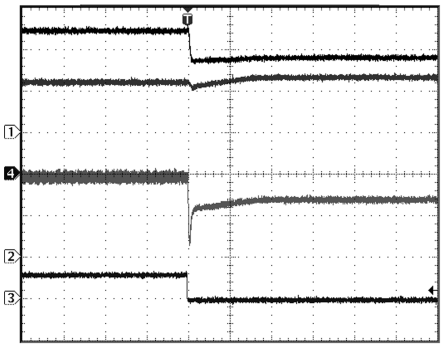
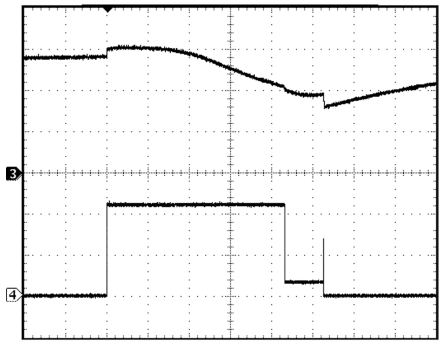


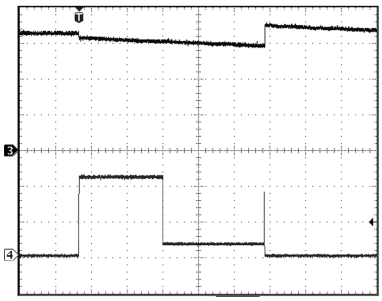
Time Base: 100 µs/div
Ch 1: V_{OUT} (2 V/div)
Ch 4: I_{LED} (500mA/div)
I_{LED} = 1.2 A
Ch 2: I_L (1 A/div)
Ch 3: ENVM (5 V/div)
V_{OUT} = 5 V
Single LED

Figure 63. Flash Pulse and V_{OUT} to Flash Pulse



Time Base: 200 µs/div
Single LED
Ch 3: NTC pin voltage (5 V/div)
R(T) = 100 kΩ at 25°C
Circuit of Figure 43
I_{LED} = 1.2 A
Ch 4: I_{LED} (500 mA/div)
R3 = 9 kΩ

Figure 64. NTC Mode Response



Time Base: 100 ms/div
Ch 3: V_{IN} (1V/div)
I_{LED} = 1.2 A
Ch 4: I_{LED} (500 mA/div)
3.1-V UVLO Setting
Single LED

Figure 65. V_{IN} Monitor Response

9 Power Supply Recommendations

The LM3554 is designed to operate from an input supply range of 2.5 V to 5.5 V. This input supply must be well regulated and provide the peak current required by the LED configuration and inductor selected.

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10 Layout

10.1 Layout Guidelines

The high frequency and large switching currents of the LM3554 make the choice of layout important. Use the following steps as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place C_{IN} on the top layer (same layer as the LM3554) and as close to the device as possible. The input capacitor conducts the driver currents during the low-side MOSFET turnon and turnoff and can see current spikes over 1 A in amplitude. Connecting the input capacitor through short wide traces on both the IN and GND terminals reduces the inductive voltage spikes that occur during switching and which can corrupt the V_{IN} line.
2. Place C_{OUT} on the top layer (same layer as the LM3554) and as close to the OUT and GND pins as possible. The returns for both C_{IN} and C_{OUT} must come together at one point, and as close to the GND pin as possible. Connecting C_{OUT} through short wide traces reduces the series inductance on the OUT and GND pins that can corrupt the V_{OUT} and GND lines and cause excessive noise in the device and surrounding circuitry.
3. Connect the inductor on the top layer close to the SW pin. There must be a low impedance connection from the inductor to SW due to the large DC inductor current, and at the same time the area occupied by the SW node must be small to reduce the capacitive coupling of the high dV/dt present at SW that can couple into nearby traces.
4. Avoid routing logic traces near the SW node to avoid any capacitively coupled voltages from SW onto any high-impedance logic lines such as TX1/TORCH/GPIO1, ENVM/TX2/GPIO2, HWEN, LEDI/NTC (NTC mode), SDA, and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.
5. Terminate the flash LED cathodes directly to the GND pin of the device. If possible, route the LED returns with a dedicated path to keep the high amplitude LED currents out the GND plane. For flash LEDs that are routed relatively far away from the device, a good approach is to sandwich the forward and return current paths over the top of each other on two layers. This helps reduce the inductance of the LED current paths.
6. The NTC thermistor is intended to have its return path connected to the LED cathode. This allows the thermistor resistive divider voltage (V_{NTC}) to trip the comparators threshold as V_{NTC} is falling. Additionally, the thermistor-to-LED cathode junction can have low thermal resistivity because both the LED and the thermistor are electrically connected at GND. The drawback is that the thermistor return detects the switching currents from the boost converter of the LM3554. Because of this, it is necessary to have a filter capacitor at the NTC pin which terminates close to the device GND and which can conduct the switched currents to GND.

10.2 Layout Example

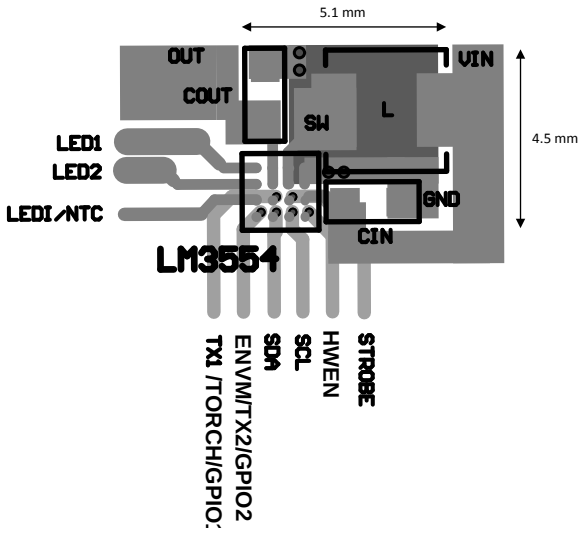

Figure 66. LM3554 Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

AN1112 DSBGA Wafer Level Chip Scale Package (SNVA009)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3554TME/NOPB	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SF
LM3554TME/NOPB.A	Active	Production	DSBGA (YFQ) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SF
LM3554TMX/NOPB	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SF
LM3554TMX/NOPB.A	Active	Production	DSBGA (YFQ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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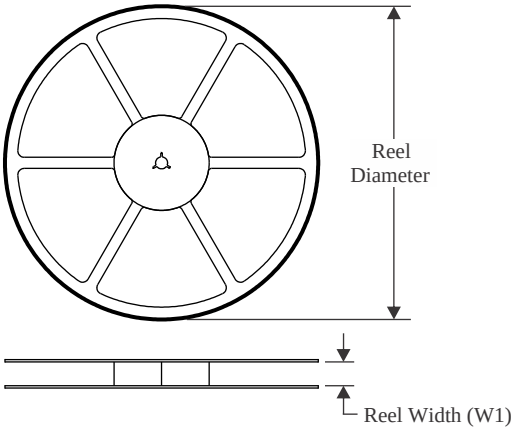
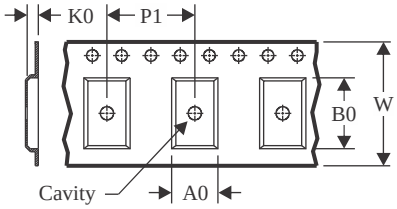
TAPE AND REEL INFORMATION

REEL DIMENSIONS

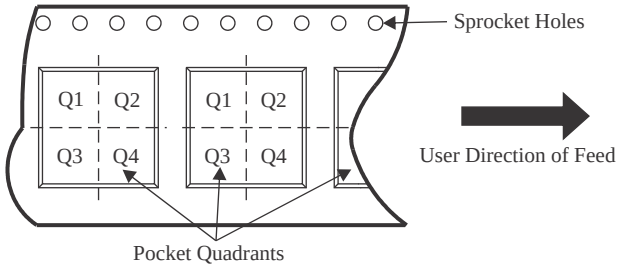


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

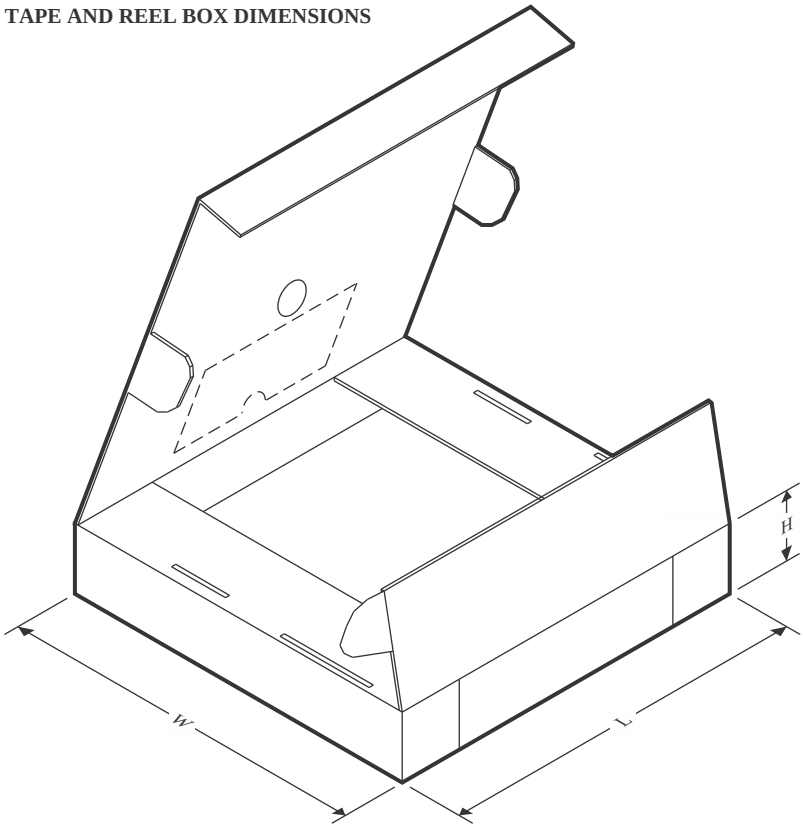
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3554TME/NOPB	DSBGA	YFQ	16	250	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LM3554TMX/NOPB	DSBGA	YFQ	16	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1

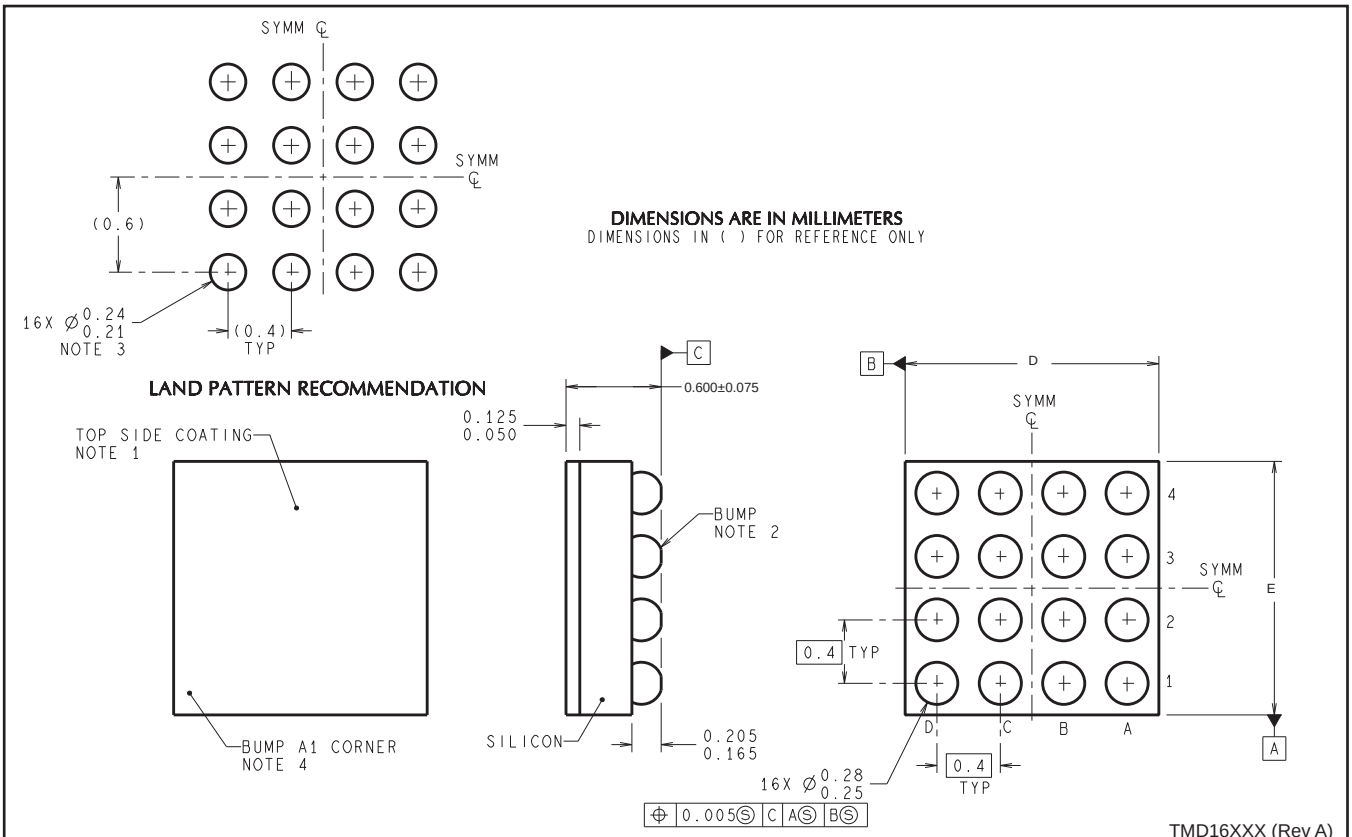
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3554TME/NOPB	DSBGA	YFQ	16	250	208.0	191.0	35.0
LM3554TMX/NOPB	DSBGA	YFQ	16	3000	208.0	191.0	35.0

YFQ0016



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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