

TSM6970D

20V Dual N-Channel MOSFET w/ESD Protected


Pin Definition:

- | | |
|-------------|-------------|
| 1. Drain 1 | 8. Drain 2 |
| 2. Source 1 | 7. Source 2 |
| 3. Source 1 | 6. Source 2 |
| 4. Gate 1 | 5. Gate 2 |

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
20	21 @ $V_{GS} = 4.5V$	8
	25 @ $V_{GS} = 2.5V$	7
	33 @ $V_{GS} = 1.8V$	6

Features

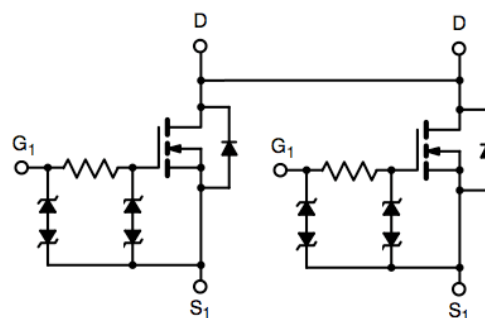
- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance
- ESD Protect 2KV

Application

- Load Switch
- PA Switch

Ordering Information

Part No.	Package	Packing
TSM6970DCA RV	TSSOP-8	3Kpcs / 13" Reel

Block Diagram


Dual N-Channel MOSFET

Absolute Maximum Rating ($T_a = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current, $V_{GS} @ 4.5V$	I_D	8	A
Pulsed Drain Current, $V_{GS} @ 4.5V$	I_{DM}	30	A
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	2.5	A
Maximum Power Dissipation	P_D	2	W
		1.28	
Operating Junction Temperature	T_J	+150	$^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R_{\theta JC}$	30	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta JA}$	62.5	$^\circ C/W$

Notes:

- a. Pulse width limited by the Maximum junction temperature
b. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Preliminary

TSM6970D

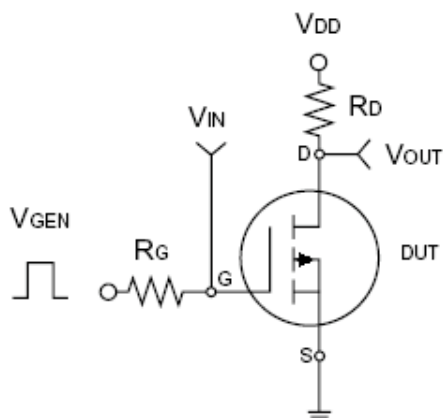
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Electrical Specifications

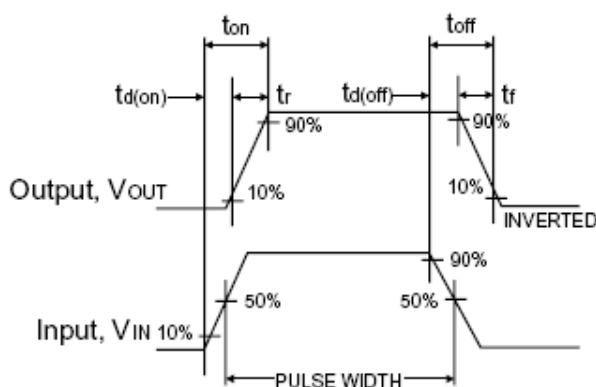
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	0.4	--	1	V
Gate Body Leakage	$V_{GS} = \pm 8V, V_{DS} = 0V$	I_{GSS}	--	--	± 10	μA
Zero Gate Voltage Drain Current	$V_{DS} = 16V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
On-State Drain Current	$V_{DS} = 5V, V_{GS} = 4.5V$	$I_{D(ON)}$	10	--	--	A
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 8A$	$R_{DS(ON)}$	--	18	21	m Ω
	$V_{GS} = 2.5V, I_D = 7A$		--	21	25	
	$V_{GS} = 1.8V, I_D = 6A$		--	26	33	
Forward Transconductance	$V_{DS} = 5V, I_D = 8A$	g_{fs}	--	13	--	S
Diode Forward Voltage	$I_S = 2.5A, V_{GS} = 0V$	V_{SD}	--	--	1.7	V
Dynamic ^b						
Total Gate Charge	$V_{DS} = 10V, I_D = 8A,$ $V_{GS} = 4.5V$	Q_g	--	13.8	--	nC
Gate-Source Charge		Q_{gs}	--	4.1	--	
Gate-Drain Charge		Q_{gd}	--	5.6	--	
Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	1160	--	pF
Output Capacitance		C_{oss}	--	104	--	
Reverse Transfer Capacitance		C_{rss}	--	29	--	
Switching ^c						
Turn-On Delay Time	$V_{DD} = 10V,$ $I_D = 1A, V_{GEN} = 4.5V,$ $R_G = 3\Omega$	$t_{d(on)}$	--	140	200	nS
Turn-On Rise Time		t_r	--	210	250	
Turn-Off Delay Time		$t_{d(off)}$	--	3700	4800	
Turn-Off Fall Time		t_f	--	2000	2600	

Notes:

- pulse test: $PW \leq 300\mu S$, duty cycle $\leq 2\%$
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

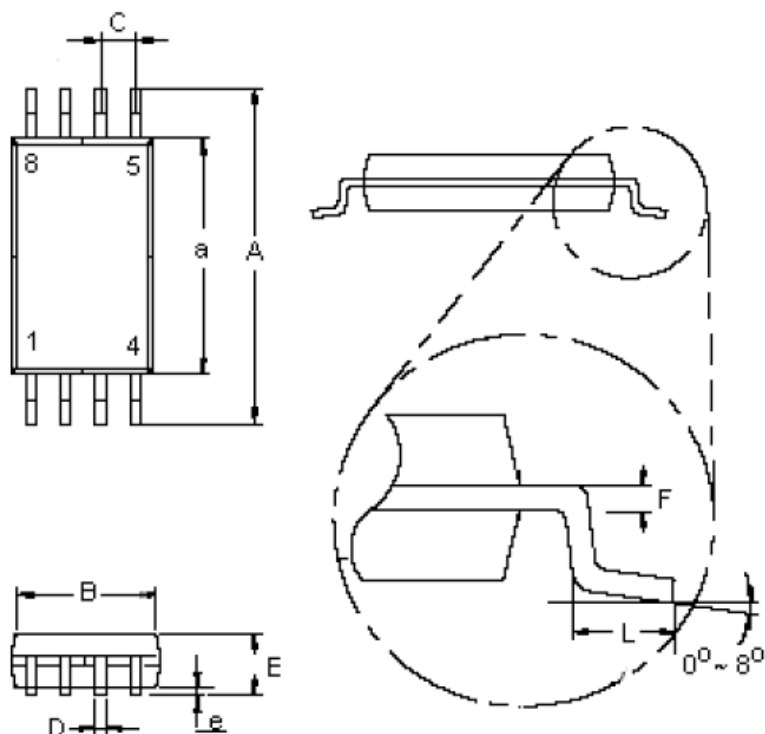


Switching Test Circuit



Switchin Waveforms

TSSOP-8 Mechanical Drawing



TSSOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.20	6.60	0.244	0.260
a	4.30	4.50	0.170	0.177
B	2.90	3.10	0.114	0.122
C	0.65 (typ)		0.025 (typ)	
D	0.25	0.30	0.010	0.019
E	1.05	1.20	0.041	0.049
e	0.05	0.15	0.002	0.009
F	0.127		0.005	
L	0.50	0.70	0.020	0.028

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