**MOTOROLA**

# MC33470

*Advance Information*

# Synchronous Rectification DC/DC Converter Programmable Integrated Controller

The MC33470 is a digitally programmable switching voltage regulator, specifically designed for Microprocessor supply, Voltage Regulator Module and general purpose applications, to provide a high power regulated output voltage using a minimum of external parts. A 5–bit digital–to–analog converter defines the dc output voltage.

This product has three additional features. The first is a pair of high speed comparators which monitor the output voltage and expedite the circuit response to load current changes. The second feature is a soft start circuit which establishes a controlled response when input power is applied and when recovering from external circuit fault conditions. The third feature is two output drivers which provide synchronous rectification for optimum efficiency.

This product is ideally suited for computer, consumer, and industrial equipment where accuracy, efficiency and optimum regulation performance is desirable.

**MC33470 Features:**

- 5–Bit Digital–to–Analog Converter Allows Digital Control of Output Voltage
- High Speed Response to Transient Load Conditions
- Output Enable Pin Provides On/Off Control
- Programmable Soft Start Control
- High Current Output Drives for Synchronous Rectification
- Internally Trimmed Reference with Low Temperature Coefficient
- Programmable Overcurrent Protection
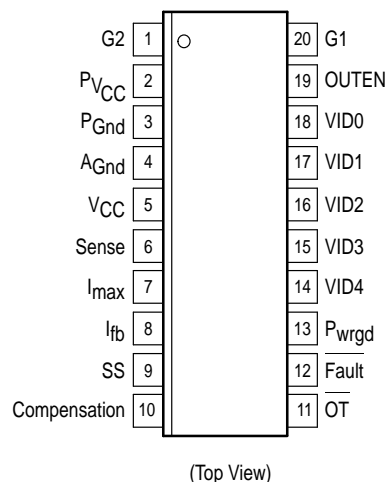- Overvoltage Fault Indication
- Functionally Similar to the LTC1553

## SYNCHRONOUS RECTIFICATION DC/DC CONVERTER PROGRAMMABLE INTEGRATED CONTROLLER

### SEMICONDUCTOR TECHNICAL DATA
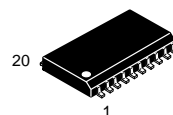


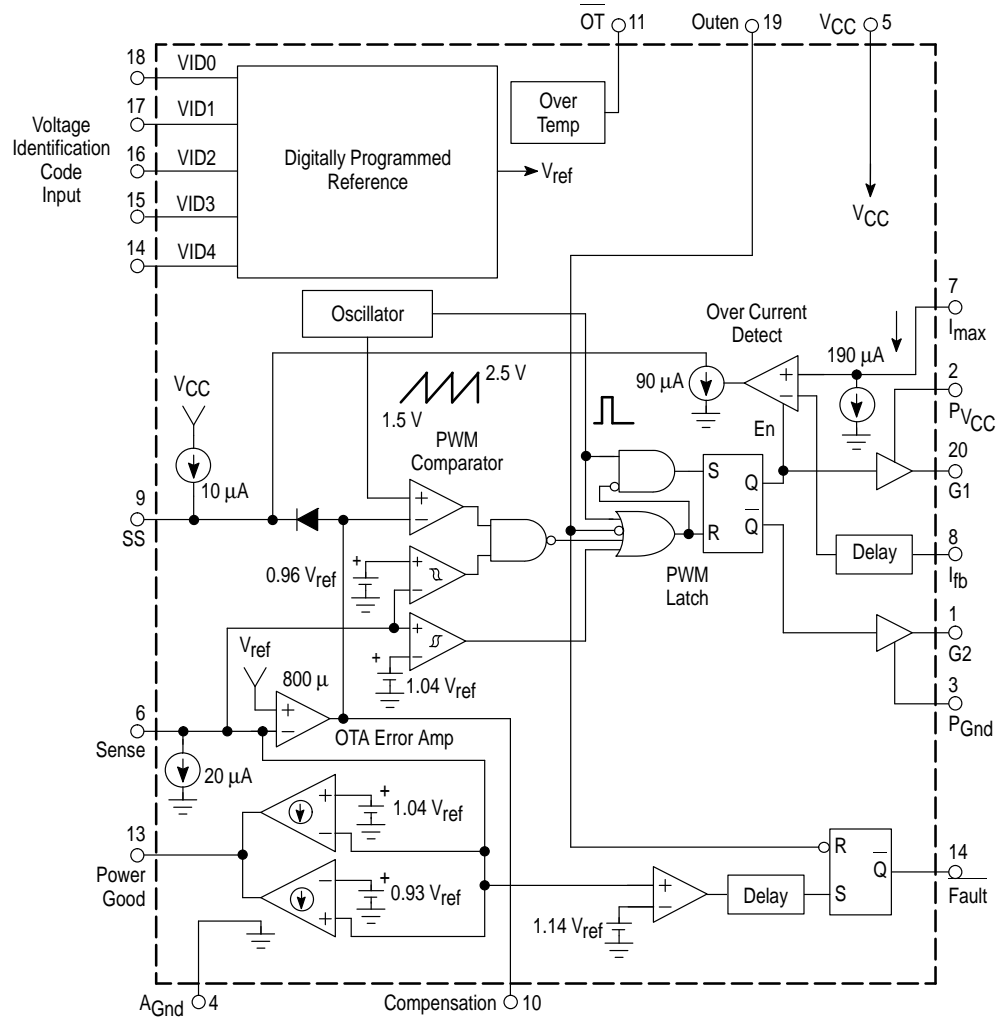**DW SUFFIX**
PLASTIC PACKAGE
CASE 751D
(SO–20L)

### PIN CONNECTIONS

| | | | | |
|---|---|---|---|---|
| G2 | 1 | ○ | 20 | G1 |
| $PV_{CC}$ | 2 | | 19 | OUTEN |
| $P_{Gnd}$ | 3 | | 18 | VID0 |
| $A_{Gnd}$ | 4 | | 17 | VID1 |
| $V_{CC}$ | 5 | | 16 | VID2 |
| Sense | 6 | | 15 | VID3 |
| $I_{max}$ | 7 | | 14 | VID4 |
| $I_{fb}$ | 8 | | 13 | $P_{wrgd}$ |
| SS | 9 | | 12 | $\overline{Fault}$ |
| Compensation | 10 | | 11 | $\overline{OT}$ |

(Top View)

### ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
|---|---|---|
| MC33470DW | $T_A$ = 0° to +75°C | SO–20L |

© Motorola, Inc. 1997

Rev 0

# MC33470

## Simplified Block Diagram

$\overline{OT}$ ○ 11  Outen ○ 19  $V_{CC}$ ○ 5

18 VID0
17 VID1
16 VID2
15 VID3
14 VID4

Voltage Identification Code Input

Digitally Programmed Reference → $V_{ref}$

Over Temp

$V_{CC}$

Oscillator

2.5 V / 1.5 V

PWM Comparator

$V_{CC}$

10 μA

9 SS

0.96 $V_{ref}$

1.04 $V_{ref}$

$V_{ref}$

800 μ

6 Sense

OTA Error Amp

20 μA

1.04 $V_{ref}$

13 Power Good

0.93 $V_{ref}$

Over Current Detect

90 μA    190 μA

En

7 $I_{max}$
2 $PV_{CC}$

S  Q
R  $\overline{Q}$

PWM Latch

Delay

20 G1
8 $I_{fb}$
1 G2
3 $P_{Gnd}$

Delay

1.14 $V_{ref}$

R  $\overline{Q}$
S

14 Fault

$A_{Gnd}$ ○ 4       Compensation ○ 10

## MAXIMUM RATINGS ($T_C = 25°C$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | V |
| Output Driver Supply Voltage (Operating) | $PV_{CC}$ | 18 | V |
| $I_{max}$, $I_{fb}$ Inputs | $V_{in}$ | −0.3 to 18 | V |
| All Other Inputs and Digital (OT, Fault, Power Good) Outputs | $V_{in}$ | −0.3 to $V_{CC}$ + 0.3 | V |
| Power Dissipation and Thermal Characteristics Maximum Power Dissipation Case 751D DW Suffix ($T_A = 70°C$) Thermal Resistance Junction–to–Ambient Thermal Resistance Junction–to–Case | $P_D$ $R_{\theta JA}$ $R_{\theta JC}$ | 0.60 91 60 | W °C/W °C/W |
| Operating Junction Temperature | $T_J$ | 125 | °C |
| Operating Ambient Temperature (Notes 1 and 2) | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +125 | °C |

**NOTE:** ESD data available upon request

# MC33470

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $P_{V_{CC}}$, = 12 V for typical values $T_A$ = Low to High [Notes 1, 2, 3], for min/max values $T_A$ is the operating ambient temperature range that applies, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Frequency ($V_{CC}$ = 4.5 to 5.5 V) | $f_{osc}$ | 210 | 300 | 390 | kHz |
| **FEEDBACK AMPLIFIER** | | | | | |
| Voltage Feedback Input Threshold (Note 4)<br>    VID0, VID1, VID2 and VID4 = "1" and VID3 = "0"<br>    VID4 = "1" and VID0, VID1, VID2 and VID3 = "0" | $V_{sense}$ | 1.764<br>2.744<br>3.43 | 1.8<br>2.8<br>3.5 | 1.836<br>2.856<br>3.57 | V<br>V<br>V |
| Input Bias Current ($V_{CM}$ = 2.8 V) | $I_{IB}$ | – | 20 | – | µA |
| Transconductance ($V_{CM}$ = 2.8 V, $V_{COMP}$ = 2.0 V) | $G_M$ | 400 | 800 | 1200 | µmho |
| Open Loop Voltage Gain ($V_{COMP}$ = 2.0 V) | $A_{VOL}$ | – | 67 | – | dB |
| Output Line Regulation ($V_{CC}$ = 4.5 to 5.5 V) | $Reg_{line}$ | – | 7.0 | – | mV |
| Output Load Regulation | $Reg_{load}$ | – | 5.0 | – | mV |
| Output Current<br>    Source<br>    Sink | <br>$I_{OH}$<br>$I_{OL}$ | <br>–<br>– | <br>120<br>120 | <br>–<br>– | µA |
| **PWM SECTION** | | | | | |
| Duty Cycle at G1 Output<br>    Maximum<br>    Minimum | <br>$DC_{max}$<br>$DC_{min}$ | <br>77<br>– | <br>88<br>– | <br>95<br>0 | % |
| Propagation Delay<br>    Comp Input to G1 Output, $T_J$ = 25°C<br>    Comp Input to G2 Output, $T_J$ = 25°C | <br>$t_{PLH1}$<br>$t_{PLH2}$ | <br>–<br>– | <br>0.1<br>0.1 | <br>–<br>– | µs |
| **SOFT–START SECTION** | | | | | |
| Charge Current ($V_{Soft-Start}$ = 0 V) | $I_{chg}$ | 7.0 | 10 | 13 | µA |
| Discharge Current under Current Limit (Note 5)<br>    ($V_{Soft-Start}$ = 2.0 V, $V_{sense}$ = $V_{out}$, $V_{imax}$ = $V_{CC}$, $V_{ifb}$ = 0 V) | $I_{SSIL}$ | 30 | 90 | 150 | µA |
| Discharge Current under Hard Current Limit<br>    ($V_{Soft-Start}$ = 2.0 V, $V_{sense}$ < $V_{out}$/2, $V_{imax}$ = $V_{CC}$, $V_{ifb}$ = 0 V) | $I_{SSHIL}$ | 40 | 64 | – | mA |
| Hard Current Limit Hold Time | $t_{SSHIL}$ | 100 | 200 | 300 | µs |
| **IMAX INPUT** | | | | | |
| Sink Current ($V_{in\ max}$ = $V_{CC}$, $V_{ifb}$ = $V_{CC}$) | $I_{OL}$ | 133 | 190 | 247 | µA |
| **POWER GOOD OUTPUT** | | | | | |
| Threshold For Logic "1" to "0" Transition<br>    Upper Threshold<br>    Lower Threshold | $V_{th}$ | <br>–<br>0.93 | <br>1.04<br>0.96 | <br>1.07<br>– | $V_{sense}$ |
| Response Time<br>    Logic "0" to "1" ($V_{sense}$ changes from 0 V to $V_O$)<br>    Logic "1" to "0" ($V_{sense}$ changes from $V_O$ to 0 V) | $t_{rPG}$ | <br>200<br>50 | <br>400<br>100 | <br>600<br>150 | µs |
| Sink Current ($V_{OL}$ = 0.5 V) | $I_{OLPG}$ | – | 10 | – | mA |
| Output Low Voltage ($I_{OL}$ = 100 µA) (Note 6) | $V_{OLPG}$ | – | 250 | 500 | mV |

**NOTES:** 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. VID1, VID3, VID4 = logic 0, and VID0, VID2 = logic 1.
4. $V_{sense}$ is provided from a low impedance voltage source or shorted to the output voltage.
5. Under a typical soft current limit, the net soft–start discharge current will be 90 µA ($I_{SSIL}$) – 10 µA ($I_{chg}$) = 80 µA. The softstart sink to source current ratio is designed to be 9:1.
6  Sense (Pin 6) = 5.0 V, Comp (Pin 10) open, VID4, VID2, VID1, VID0 = 1.0, VID3 = 0.
7. OUTEN is internally pulled low if VID0, 1, 2, 3, and 4 are floating.
8. Due to internal pull–up resistors, there will be an additional 0.5 mA per pin if any of the VID0, 1, 2, 3, or 4 pins are pulled low.

**ELECTRICAL CHARACTERISTICS (continued)** ($V_{CC}$ = 5.0 V, $P_{V_{CC}}$, = 12 V for typical values $T_A$ = Low to High [Notes 1, 2, 3], for min/max values $T_A$ is the operating ambient temperature range that applies, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **FAULT OUTPUT** | | | | | |
| Threshold For Logic "0" to "1" Transition | $V_{thF}$ | 1.12 | 1.14 | 1.2 | $V_{ref}$ |
| $V_{sense}$ Response Time Switches from 2.8 V to $V_{CC}$ | $t_{rF}$ | 50 | 100 | 150 | μs |
| Sink Current ($V_{OL}$ = 0.5 V) | $I_{OLF}$ | – | 10 | – | mA |
| **OVERTEMPERATURE OUTPUT** | | | | | |
| Threshold For Logic "1" to "0" Transition (OUTEN Voltage Decreasing) | $V_{thOUTEN}$ | 1.85 | 2.0 | 2.2 | V |
| Delay Time | $t_{DOT}$ | 25 | 50 | 100 | μs |
| Sink Current ($V_{OL}$ = 0.5 V) | $I_{OLF}$ | – | 10 | – | mA |
| **LOGIC INPUTS (VID0, VID1, VID2, VID3, VID4)** | | | | | |
| Input Low State | $V_{IL}$ | – | – | 0.8 | V |
| Input High State | $V_{IH}$ | 3.5 | – | – | V |
| Input Impedance | $R_{in}$ | – | 10 | – | kΩ |
| **OUTPUT ENABLE CONTROL (OUTEN)** | | | | | |
| Over–Temperature Driver Disable and Reset (OUTEN Voltage Decreasing) (Note 7) | $V_{OTDD}$ | 1.55 | 1.70 | 1.85 | V |
| **OUTPUT SECTIONS (G1, G2)** | | | | | |
| Source Resistance ($V_{sense}$ = 2.0 V, $V_G$ = $P_{V_{CC}}$ – 1.0 V) | $R_{OH}$ | – | 0.5 | – | Ω |
| Sink Resistance ($V_{sense}$ = 0 V, $V_G$ = 1.0 V) | $R_{OL}$ | – | 0.5 | – | |
| Output Voltage with OUTEN Reset ($I_{sink}$ = 1.0 mA) | $V_{OL}$ | – | 0.1 | 0.5 | V |
| Output Voltage Rise Time ($C_L$ = 10 nF, $T_J$ = 25°C) | $t_r$ | – | 70 | 140 | ns |
| Output Voltage Fall Time ($C_L$ = 10 nF, $T_J$ = 25°C) | $t_f$ | – | 70 | 140 | ns |
| G1, G2 Non–Overlap Time ($C_L$ = 10 nF, $T_J$ = 25°C) | $t_{NOL}$ | 30 | 150 | 210 | ns |
| **TOTAL DEVICE** | | | | | |
| Minimum Operating Voltage After Turn–On ($P_{V_{CC}}$ Decreasing) | $P_{V_{CC} min}$ | 10.8 | – | – | V |
| Minimum Operating Voltage After Turn–On ($V_{CC}$ Decreasing) | $V_{CC min}$ | 3.0 | – | 4.25 | V |
| $V_{CC}$ Current (Note 8) (OUTEN and $P_{V_{CC}}$ open, VID0, 1, 2, 3, 4 Floating) | $I_{CC}$ | – | 3.7 | 8.0 | mA |
| $P_{V_{CC}}$ Current (OUTEN = 5.0 V, VID0, 1, 2, 3, 4 Open, $P_{V_{CC}}$ = 12 V) | $P_{I_{CC}}$ | – | 15 | – | mA |

**NOTES:** 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. VID1, VID3, VID4 = logic 0, and VID0, VID2 = logic 1.
4. $V_{sense}$ is provided from a low impedance voltage source or shorted to the output voltage.
5. Under a typical soft current limit, the net soft–start discharge current will be 90 μA ($I_{SSIL}$) – 10 μA ($I_{chg}$) = 80 μA. The softstart sink to source current ratio is designed to be 9:1.
6 Sense (Pin 6) = 5.0 V, Comp (Pin 10) open, VID4, VID2, VID1, VID0 = 1.0, VID3 = 0.
7. OUTEN is internally pulled low if VID0, 1, 2, 3, and 4 are floating.
8. Due to internal pull–up resistors, there will be an additional 0.5 mA per pin if any of the VID0, 1, 2, 3, or 4 pins are pulled low.
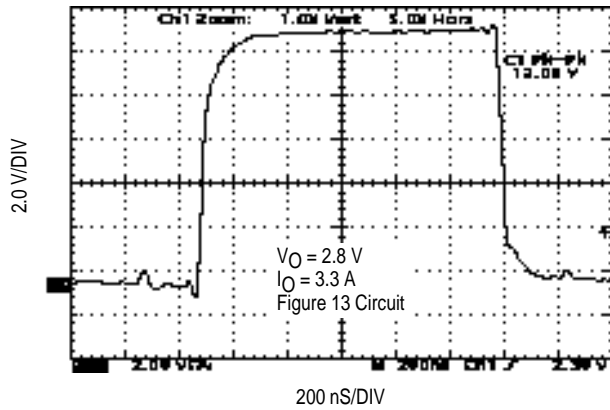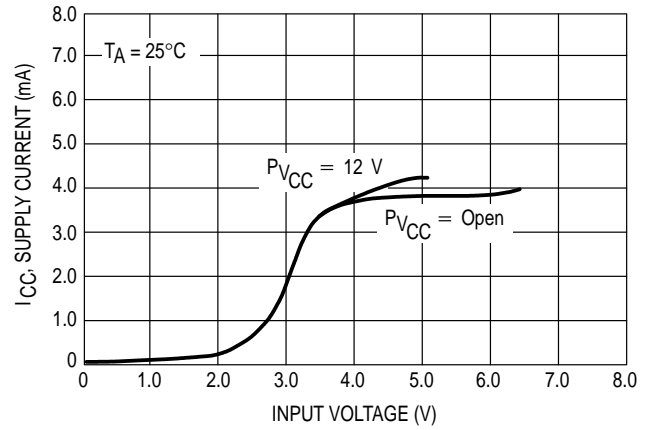
# MC33470

### Figure 1. Output Drive Waveform



2.0 V/DIV

$V_O$ = 2.8 V
$I_O$ = 3.3 A
Figure 13 Circuit

200 nS/DIV

### Figure 2. 5.0 V Supply Current



$I_{CC}$, SUPPLY CURRENT (mA)

$T_A$ = 25°C

$P_{V_{CC}}$ = 12 V

$P_{V_{CC}}$ = Open

INPUT VOLTAGE (V)

### Figure 3. Error Amplifier Transient Response



500 mV/DIV

$V_O$ = 2.8 V
$I_O$ transient = 0.3 to 16 A
Figure 13 Circuit

2.5 mS/DIV
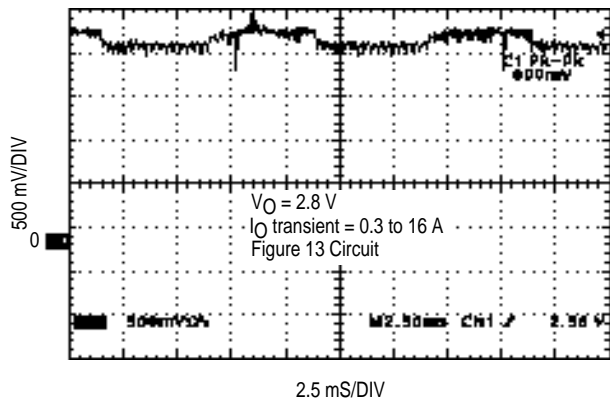
### Figure 4. Drive Output Source/Sink Saturation Voltage versus Load Current



$P_{V_{CC}}$

Source Saturation
(Load to Ground)

Sink Saturation
(Load to $P_{V_{CC}}$)

Ground
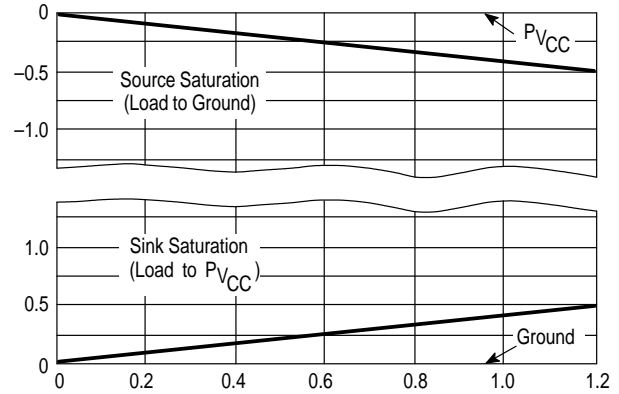
### Figure 5. Feedback Circuit Load Transient Response



50 mV/DIV

$V_O$ = 2.8 V
$I_O$ transient = 0.3 to 16 A
Figure 13 Circuit

2.5 mS/DIV
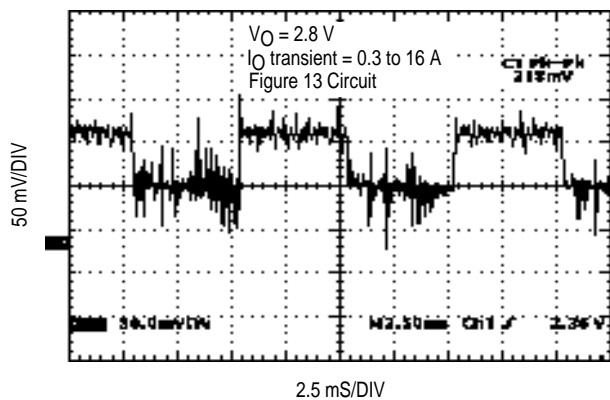
### Figure 6. Feedback Loop Gain and Phase versus Frequency



LOOP GAIN (dB)

$\varnothing$, EXCESS PHASE (DEGREES)

$V_{CCP}$ = 12 V
$V_{CC}$ = 5.0 V
$V_O$ = 2.8 V
$I_O$ = 3.3 A
$T_A$ = 25°C

Gain

Phase

f, FREQUENCY (Hz)
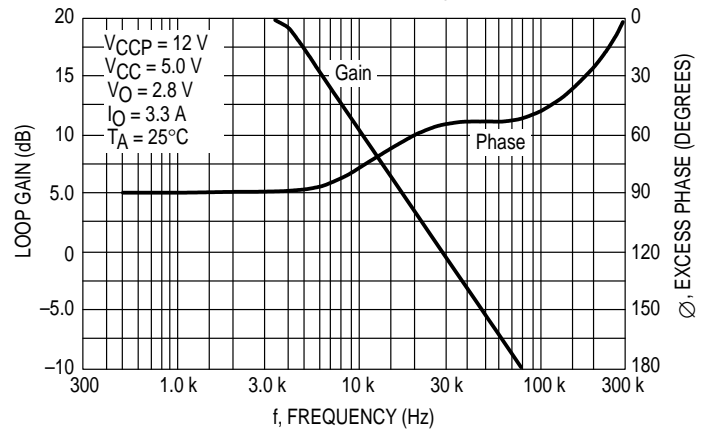
**Figure 7. Drive Output Source/Sink Saturation Voltage versus Load Current**

GAIN (μmho) / Ø, EXCESS PHASE (DEGREES)

V_CCP = 12 V
V_CC = 5.0 V
V_O = 2.8 V
R2 = 18.2 k
C16 = 0
T_A = 25°C
Figure 13

Gain

Phase

FREQUENCY (kHz)
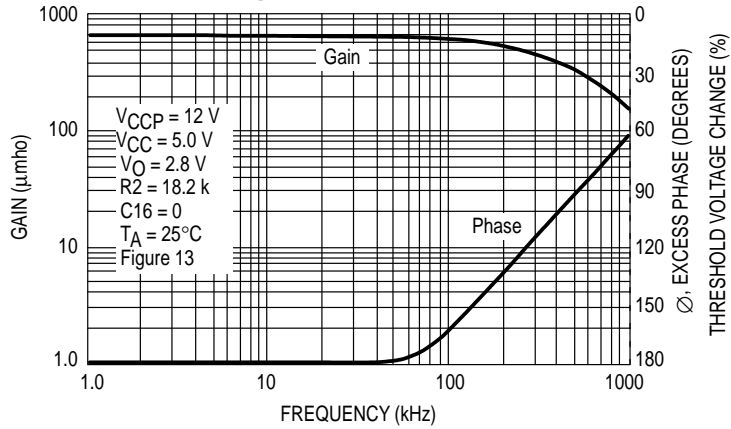
**Figure 8. Feedback Threshold Voltage versus Temperature**

THRESHOLD VOLTAGE CHANGE (%)

I_O = 3.3 A
V_O = 2.8 V

T_A, AMBIENT TEMPERATURE (°C)
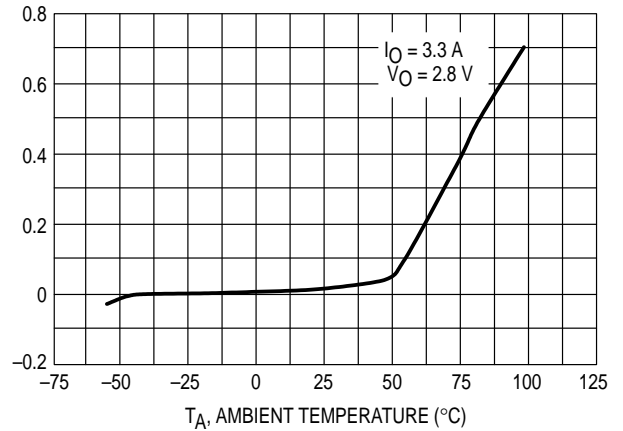
**Figure 9. I_max Current versus Temperature**

I_max, CURRENT CHANGE (%)

I_O = 3.3 A
V_O = 2.8 V

T_A, AMBIENT TEMPERATURE (°C)
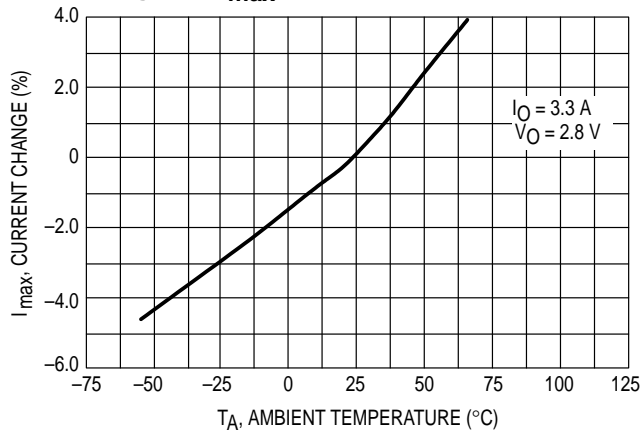
**Figure 10. V_sense Current Source versus Temperature**

I_sense, CURRENT CHANGE (%)

I_O = 3.3 A
V_O = 2.8 V

T_A, AMBIENT TEMPERATURE (°C)
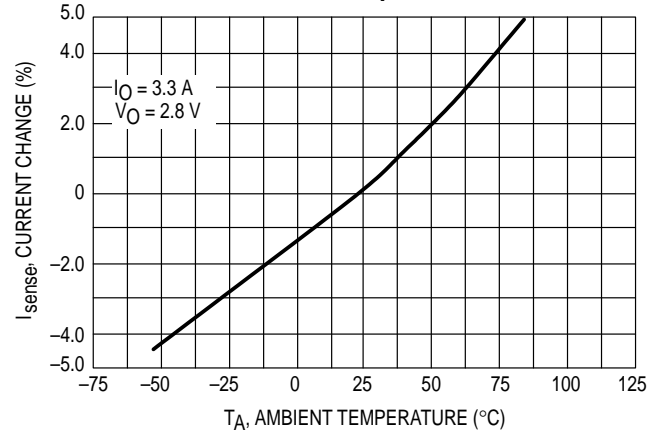
**Figure 11. V_CC Undervoltage Lockout Trip Point versus Temperature**

UVLO THRESHOLD CHANGE (%)

V_CC Increasing
I_O = 3.3 A
V_O = 2.8 V

T_A, AMBIENT TEMPERATURE (°C)
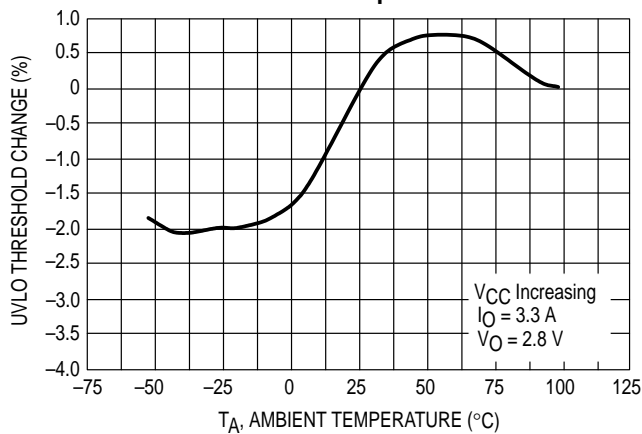
**Figure 12. Oscillator Frequency versus Temperature**

UVLO THRESHOLD CHANGE (%)

I_O = 3.3 A
V_O = 2.8 V

T_A, AMBIENT TEMPERATURE (°C)
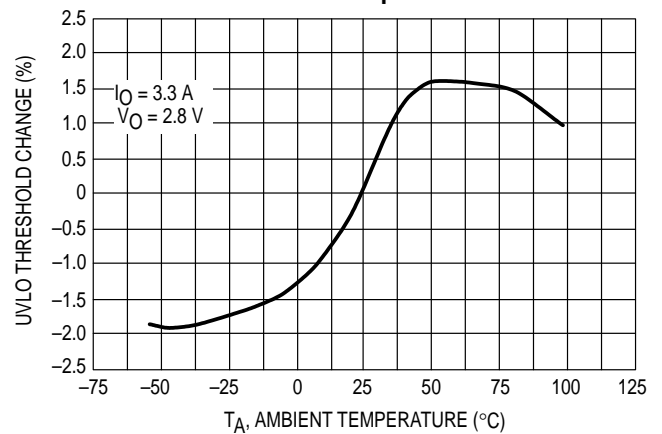
# MC33470

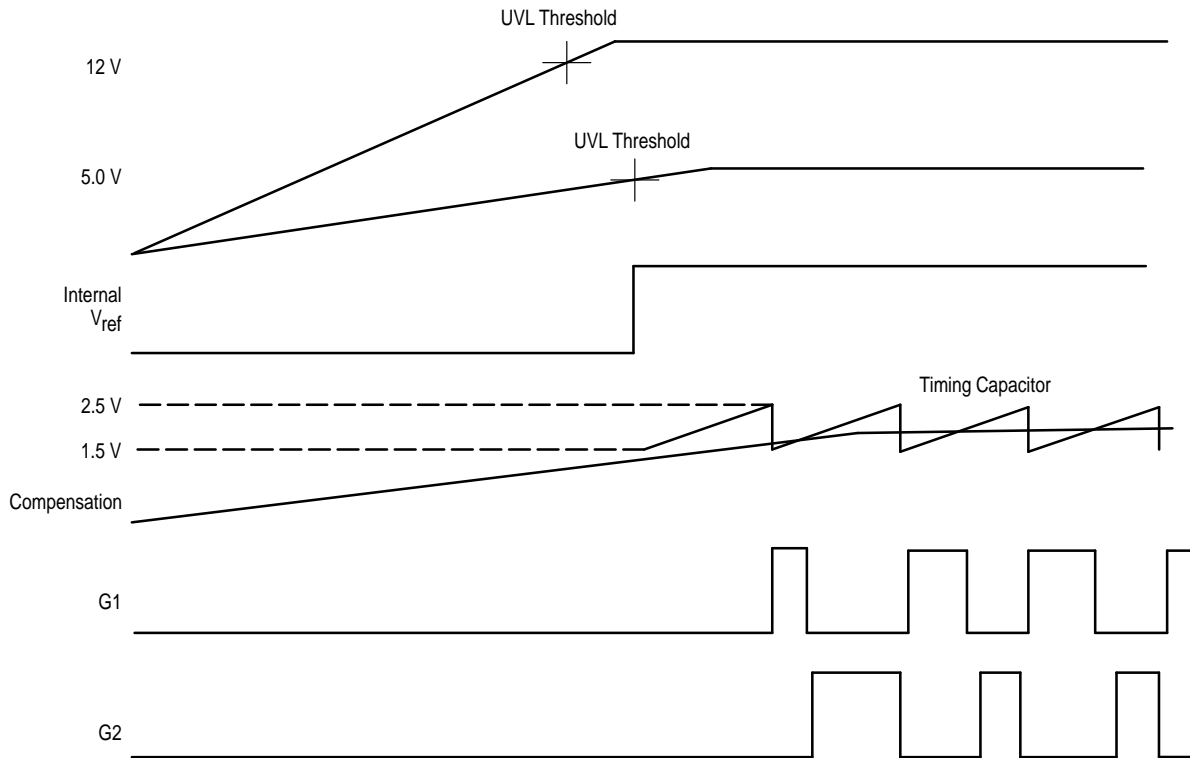**Figure 13. MC33470 Application Circuit**
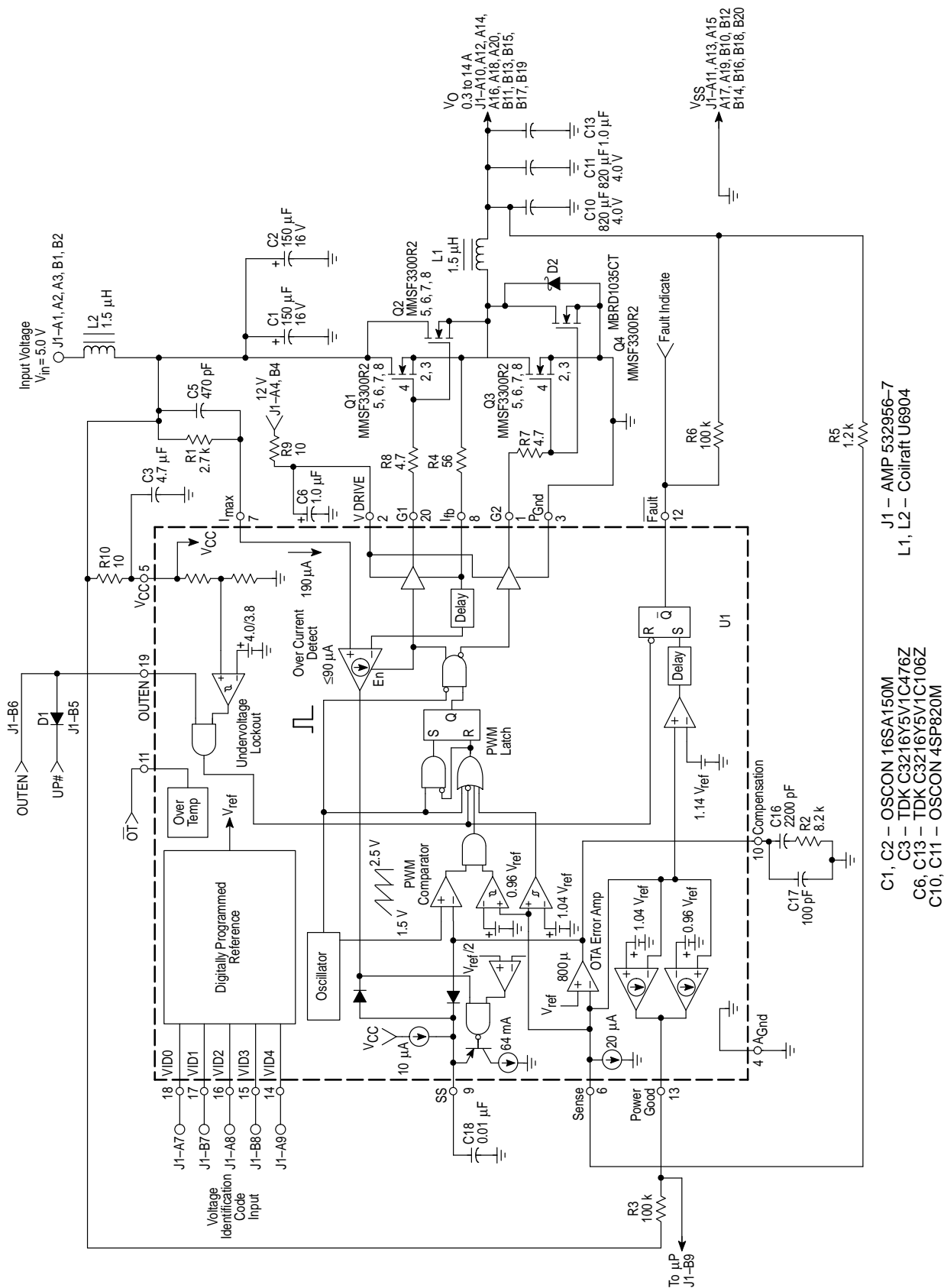
**Figure 14. Timing Diagram**



## OPERATING DESCRIPTION

The MC33470 is a monolithic, fixed frequency power switching regulator specifically designed for dc–to–dc converter applications which provide a precise supply voltage for state of the art processors. The MC33470 operates as fixed frequency, voltage mode regulator containing all the active functions required to directly implement digitally programmable step–down synchronous rectification with a minimum number of external components.

**Oscillator**

The oscillator frequency is internally programmed to 300 kHz. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the switch outputs. During the fall time of the internal sawtooth waveform, the oscillator generates an internal blanking pulse that disables the G1 output switching MOSFET. The internal sawtooth waveform has a nominal peak voltage of 2.5 V and a valley voltage of 1.5 V.

**Pulse Width Modulator**

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied to the inverting input. Output switch conduction is initiated when the ramp waveform is discharged to the valley voltage. As the ramp voltage increases to a voltage that exceeds the error amplifer output, the latch resets, terminating output G1 MOSFET conduction, and turning on output G2 MOSFET, for the duration of the oscillator ramp. This PWM/latch combination

prevents multiple output pulses during a given oscillator cycle.

The sense voltage input at Pin 6 is applied to the noninverting inputs of a pair of high speed comparators. The high speed comparators' inverting inputs are tied 0.96 x $V_{ref}$ and 1.04 x $V_{ref}$, respectively, to provide an optimum response to load changes. When load transients which cause the output voltage to fall outside a $\pm 4\%$ regulation window occur, the high speed comparators override the PWM comparator to force a zero or maximum duty cycle operating condition until the output voltage is once again within the linear window.

When voltages are initially provided to the supply pins, $V_{CC}$ and $P_{V_{CC}}$, undervoltage lockout circuits monitor each of the supply voltage levels. Both G1 and G2 output pins are held low until the $V_{CC}$ pin voltage exceeds 4.0 V and the $P_{V_{CC}}$ pin voltage exceeds 9.0 V.

**Error Amplifier and Voltage Reference**

The error amplifier is a transconductance type amplifier, having a nominal transconductance of 800 $\mu$mho. The transconductance has a negative temperature coefficient. Typical transconductance is 868 $\mu$mho at 0°C and 620 $\mu$mho at 125°C junction temperature. The amplifier has a cascode output stage which provides a typical 3.0 Mega–Ohms of impedance. The typical error amplifier dc voltage gain is 67 dB.

External loop compensation is required for converter stability. Compensation components may be connected from

the compensation pin to ground. The error amplifier input is tied to the sense pin which also has an internal 20 μA current source to ground. The current source is intended to provide a 24 mV offset when an external 1.2 k resistor is placed between the output voltage and the sense pin. The 24 mV offset voltage is intended to allow a greater dynamic load regulation range within a given specified tolerance for the output voltage. The offset may be increased by increasing the resistor value. The offset can be eliminated by connecting the sense pin directly to the regulated output voltage.

The voltage reference consists of an internal, low temperature coefficient, reference circuit with an added offset voltage. The offset voltage level is the output of the digital–to–analog converter. Control bits VID0 through VID4 control the amount of offset voltage which sets the value of the voltage reference, as shown in Table 1. The VID0–4 input bits each have internal 10 k pullup resistances. Therefore, the reference voltage, and the output voltage, may be programmed by connecting the VID pins to ground for logic "0" or by an open for a logic "1". Typically, a logic "1" will be recognized by a voltage > 0.67 x $V_{CC}$. A logic "0" is a voltage < $V_{CC}/3$.

### MOSFET Switch Outputs

The output MOSFETs are designed to switch a maximum of 18 V, with a peak drain current of 2.0 A. Both G1 and G2 output drives are designed to switch N–channel MOSFETs. Output drive controls to G1 and G2 are phased to prevent cross conduction of the internal IC output stages. Output dead time is typically 100 nanoseconds between G1 and G2 in order to minimize cross conduction of the external switching MOSFETs.

### Current Limit and Soft–Start Controls

The soft–start circuit is used both for initial power application and during current limit operation. A single external capacitor and an internal 10 μA current source control the rate of voltage increase at the error amplifier output, establishing the circuit turn on time. The G1 output will increase from zero duty cycle as the voltage across the soft–start capacitor increases beyond about 0.5 V. When the soft–start capacitor voltage has reached about 1.5 V, normal duty cycle operation of G1 will be allowed.

An overcurrent condition is detected by the current limit amplifier. The current limit amplifier is activated whenever the G1 output is high. The current limit amplifier compares the voltage drop across the external MOSFET driven by G1, as measured at the $I_{FB}$ pin, with the voltage at the $I_{max}$ pin. Because the $I_{max}$ pin draws 190 μA of input current, the overcurrent threshold is programmed by an external resistor.

Referring to Figure 13, the current limit resistor value can be determined from the following equation:

$$R1 = \frac{[(I_{L(max)})(R_{DS(on)})]}{(I_{max})}$$

where:

$$I_{L(max)} = \frac{I_O + I_{ripple}}{2}$$

$I_O$ = Maximum load current
$I_{ripple}$ = Inductor peak to peak ripple current

### OUTEN Input and OT Output Pins

On and off control of the MC33470 may be implemented with the OUTEN pin. A logic "1" applied the OUTEN pin, where a logic "1" is above 2.0 V, will allow normal operation of the MC33470. The OUTEN pin also has multiple thresholds to provide over temperature protection. An negative temperature coefficient thermistor can be connected to the OUTEN pin, as shown in Figure 15. Together with $R_S$, a voltage divider is formed. The divider voltage will decrease as the thermistor temperature increases. Therefore, the thermistor should be mounted to the hottest part on the circuit board. When the OUTEN voltage drops below 2.0 V typically, the MC33470 OT pin open collector output will switch from a logic "1" to a logic "0", providing a warning to the system. If the OUTEN voltage drops below 1.7 V, both G1 and G2 output driver pins are latched to a logic "0" state.

**Figure 15. OUTEN/OT Overtemperature Function**
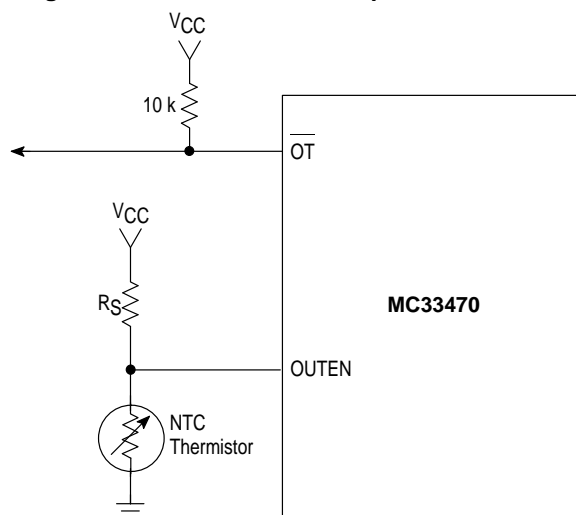


## APPLICATIONS INFORMATION

### Design Example

Given the following requirements, design a switching dc–to–dc converter:

$$V_{CC} = 5.0 \text{ V}$$
$$V_{CCP} = 12 \text{ V}$$
$$\text{VID4–0 bits} = 10111 - \text{Output Voltage} = 2.8 \text{ V}$$
$$\text{Output current} = 0.3 \text{ A to } 14 \text{ A}$$

Efficiency ≥ 80% at full load
Output ripple voltage ≈ 1% of output voltage

1. Choose power MOSFETs.

In order to meet the efficiency requirement, MOSFETs should be chosen which have a low value of $R_{DS(on)}$. However, the threshold voltage rating of the MOSFET must also be greater than 1.5 V, to prevent turn on of the synchronous rectifier MOSFETs due to dv/dt coupling through the Miller capacitance of the MOSFET drain–to–source junction. Figure 16 shows the gate voltage transient due to this effect.

In this design, choose two parallel MMSF3300 MOSFETs for both the main switch and the synchronous rectifier to maximize efficiency.

2. $D \approx V_O/V_{in} = 2.8/5.0 = 0.56$

3. Inductor selection

In order to maintain continuous mode operation at 10% of full load current, the minimum value of the inductor will be:

$L_{min} = (V_{in} - V_O)(DTs)/(2I_{O\ min})$
$= (5 - 2.8)(0.56 \times 3.3\ \mu s)/(2 \times 1.4\ A) = 1.45\ \mu H$

Coilcraft's U6904, or an equivalent, provides a surface mount 1.5 μH choke which is rated for for full load current.

4. Output capacitor selection

$V_{ripple} \approx \Delta I_L \times ESR$, where ESR is the equivalent series resistance of the output capacitance. Therefore:

$ESR_{max} = V_{ripple}/\Delta I_L = 0.01 \times 2.8\ V/1.4\ A = 0.02\ \Omega$ maximum

The AVX TPS series of tantalum chip capacitors may be chosen. Or OSCON capacitors may be used if leaded parts are acceptable. In this case, the output capacitance consists of two parallel 820 μF, 4.0 V capacitors. Each capacitor has a maximum specified ESR of 0.012 Ω.

5. Input Filter

As with all buck converters, input current is drawn in pulses. In this case, the current pulses may be 14 A peak. If a 1.5 μH choke is used, two parallel OSCON 150 μF, 16 V capacitors will provide a filter cutoff frequency of 7.5 kHz.

6. Feedback Loop Compensation

The corner frequency of the output filter with L = 1.5 μH and $C_O = 1640$ μF is 3.2 kHz. In addition, the ESR of each output capacitor creates a zero at:

$f_Z = 1/(2\pi\ C\ ESR) = 1/(2\pi \times 820\ \mu F \times 0.012) = 16.2\ kHz$

The dc gain of the PWM is: Gain = $V_{in}/V_{pp} = 5/1 = 5.0$. Where $V_{pp}$ is the peak–to–peak sawtooth voltage across the internal timing capacitor. In order to make the feedback loop as responsive as possible to load changes, choose the unity gain frequency to be 10% of the switching frequency, or 30 kHz. Plotting the PWM gain over frequency, at a frequency of 30 kHz the gain is about −16.5 dB = 0.15. Therefore, to have a 30 kHz unity gain loop, the error amplifier gain at 30 kHz should be 1/0.15 = 6.7. Choose a design phase margin for the loop of 60°. Also, choose the error amp type to be an integrator for best dc regulation performance. The phase boost needed by the error amplifier is then 60° for the desired phase margin. Then, the following calculations can be made:

k = tan [Boost/2 + 45°] = tan [60/2 + 45] = 3.73
Error Amp zero freq = $f_C$/K = 30 kHz/3.73 = 8.0 kHz
Error Amp pole freq = $K_{f_C}$ = 3.73 x 30 kHz = 112 kHz
R2 = Error Amp Gain/$G_m$ = 6.7/800 μ = 8.375 k – use an 8.2 k standard value
C16 = 1/(2π R2 $f_Z$) = 1/(2π x 8.2 k x 8.0 kHz) = 2426 pF – use 2200 pF
C17 = 1/(2π R2 $f_p$) = 1/(2π x 8.2 k x 112 kHz) = 173 pF – use 100 pF

The complete design is shown in Figure 13. The PC board top and bottom views are shown in Figures 17 and 18.

**Figure 16. Voltage Coupling Through Miller Capacitance**
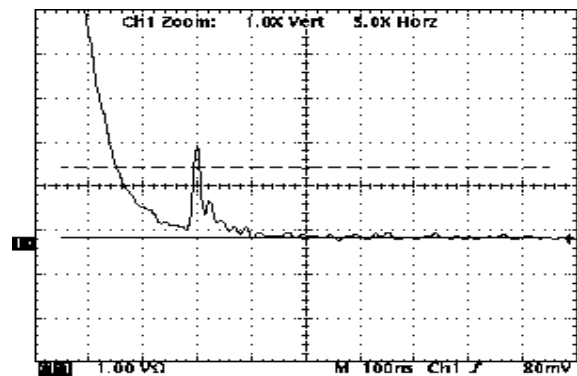
# MC33470

## PIN FUNCTION DESCRIPTION

| Pin | Name | Description |
|---|---|---|
| 1 | G2 | This is a high current dual totem pole output Gate Drive for the Lower, or rectifier, N–channel MOSFET. Its output swings from ground to $P_{V_{CC}}$. During initial power application, both G2 and G1 are held low until both $V_{CC}$ and $P_{V_{CC}}$ have reached proper levels. |
| 2 | $P_{V_{CC}}$ | This is a separate power source connection for driving N–channel MOSFETs from the G1 and G2 outputs. It may be connected to 12 V. |
| 3 | $P_{Gnd}$ | This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry. |
| 4 | $A_{Gnd}$ | This pin is the ground for the control circuitry. |
| 5 | $V_{CC}$ | This pin is the positive supply of the control IC. |
| 6 | Sense | This pin is used for feedback from the output of the power supply. It has a 20 µA current source to ground which can be used to provide offset in the converter output voltage. |
| 7 | $I_{max}$ | This pin sets the current limit threshold. 190 µA must be sourced into the pin. The external resistor is determined from the following equation: R = ([$R_{DS(on)}$] [$I_{LIM}$]/[190 µA]) |
| 8 | $I_{FB}$ | This pin has two functions. First, it provides cycle–by–cycle current limiting. Second, if the current is excessive, this pin will reinitiate a soft–start cycle. If the voltage at the $I_{FB}$ pin drops below the voltage at the $I_{max}$ pin when G1 is on, the controller will go into current limit. The current limit circuit can be disabled by floating the $I_{max}$ pin and shorting the $I_{FB}$ pin to $V_{CC}$. |
| 9 | SS | This is the soft–start pin. A capacitor at this pin, in conjunction with a 10 µA internal current source, sets the soft–start time. During moderate overload (current limit with $V_O$ > 50% of the set value), the soft–start capacitor will be discharged by an internal 90 µA current source in order to reduce the duty cycle of G1. During hard current limit (current limit with $V_O$ < 50% of set value), the soft–start capacitor will be discharged by a 64 mA current source. |
| 10 | Comp | This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter. |
| 11 | OT | This is the over temperature fault pin. OT is an open drain output that will be pulled low if the OUTEN pin is less than 2.0 V. |
| 12 | Fault | This pin indicates a fault condition. Fault is an open drain output that switches low if $V_O$ exceeds 115% of its set value. Once triggered, the controller will remain in this state until the power supply is recycled or the OUTEN pin is toggled. |
| 13 | $P_{wrgd}$ | This pin is an open drain output which indicates that $V_O$ is properly regulated. A high level on $P_{wrgd}$ indicates that $V_O$ is within ±4% of its set value for more than 400 µs. $P_{wrgd}$ will switch low if $V_O$ is outside ±4% for more than 100 µs. |
| 14 | VID4 | Voltage ID pin. This CMOS–compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull–up resistor to $V_{CC}$. |
| 15 | VID3 | Voltage ID pin. This CMOS–compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull–up resistor to $V_{CC}$. |
| 16 | VID2 | Voltage ID pin. This CMOS–compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull–up resistor to $V_{CC}$. |
| 17 | VID1 | Voltage ID pin. This CMOS–compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull–up resistor to $V_{CC}$. |
| 18 | VID0 | Voltage ID pin. This CMOS–compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull–up resistor to $V_{CC}$. |
| 19 | OUTEN | This is the on/off control pin. A CMOS–compatible logic "1" allows the controller to operate. This pin can also be used as a temperature sensor to trigger the OT pin (when OUTEN drops below 2.0 V OT pulls low). When OUTEN drops below 1.7 V for longer than 50 µs, the controller will shut down. |
| 20 | G1 | This is a high current dual totem pole output Gate Drive for the Upper, or switching, N–channel MOSFET. Its output swings from ground to $P_{V_{CC}}$. During initial power application, both G2 and G1 are held low until both $V_{CC}$ and $P_{V_{CC}}$ have reached proper levels. |

# MC33470

**Table 1. Voltage Identification Code**

| VID4 | VID3 | VID2 | VID1 | VID0 | V$_O$ |
|------|------|------|------|------|-------|
| 0 | 1 | 1 | 1 | 1 | – |
| 0 | 1 | 1 | 1 | 0 | – |
| 0 | 1 | 1 | 0 | 1 | – |
| 0 | 1 | 1 | 0 | 0 | – |
| 0 | 1 | 0 | 1 | 0 | – |
| 0 | 1 | 0 | 0 | 1 | – |
| 0 | 1 | 0 | 0 | 0 | – |
| 0 | 0 | 1 | 1 | 1 | – |
| 0 | 0 | 1 | 1 | 0 | – |
| 0 | 0 | 1 | 0 | 1 | 1.8 |
| 0 | 0 | 1 | 0 | 0 | 1.85 |
| 0 | 0 | 0 | 1 | 1 | 1.9 |
| 0 | 0 | 0 | 1 | 0 | 1.95 |
| 0 | 0 | 0 | 0 | 1 | 2.0 |
| 0 | 0 | 0 | 0 | 0 | 2.05 |
| 1 | 1 | 1 | 1 | 1 | No CPU |
| 1 | 1 | 1 | 1 | 0 | 2.1 |
| 1 | 1 | 1 | 0 | 1 | 2.2 |
| 1 | 1 | 1 | 0 | 0 | 2.3 |
| 1 | 1 | 0 | 1 | 1 | 2.4 |
| 1 | 1 | 0 | 1 | 0 | 2.5 |
| 1 | 1 | 0 | 0 | 1 | 2.6 |
| 1 | 1 | 0 | 0 | 0 | 2.7 |
| 1 | 0 | 1 | 1 | 1 | 2.8 |
| 1 | 0 | 1 | 1 | 0 | 2.9 |
| 1 | 0 | 1 | 0 | 1 | 3.0 |
| 1 | 0 | 1 | 0 | 0 | 3.1 |
| 1 | 0 | 0 | 1 | 1 | 3.2 |
| 1 | 0 | 0 | 1 | 0 | 3.3 |
| 1 | 0 | 0 | 0 | 1 | 3.4 |
| 1 | 0 | 0 | 0 | 0 | 3.5 |

# MC33470

**Table 2. Connector Pin Function**

| PIN | ROW A | ROW B |
|-----|-------|-------|
| 1 | 5.0 $V_{in}$ | 5.0 $V_{in}$ |
| 2 | 5.0 $V_{in}$ | 5.0 $V_{in}$ |
| 3 | 5.0 $V_{in}$ | Reserved |
| 4 | 12 $V_{in}$ | 12 $V_{in}$ |
| 5 | Reserved | UP# |
| 6 | $I_{share}$ | OUTEN |
| 7 | VID0 | VID1 |
| 8 | VID2 | VID3 |
| 9 | VID4 | $P_{wrgd}$ |
| 10 | $V_{CCP}$ | $V_{SS}$ |
| 11 | $V_{SS}$ | $V_{CCP}$ |
| 12 | $V_{CCP}$ | $V_{SS}$ |
| 13 | $V_{SS}$ | $V_{CCP}$ |
| 14 | $V_{CCP}$ | $V_{SS}$ |
| 15 | $V_{SS}$ | $V_{CCP}$ |
| 16 | $V_{CCP}$ | $V_{SS}$ |
| 17 | $V_{SS}$ | $V_{CCP}$ |
| 18 | $V_{CCP}$ | $V_{SS}$ |
| 19 | $V_{SS}$ | $V_{CCP}$ |
| 20 | $V_{CCP}$ | $V_{SS}$ |

# MC33470

**Figure 17. PC Board Top View**
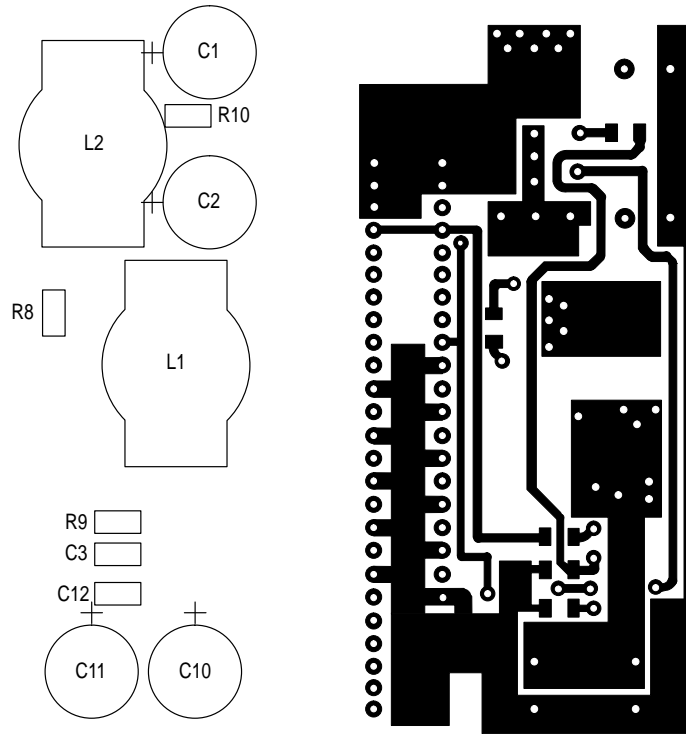


**Figure 18. PC Board Bottom View**
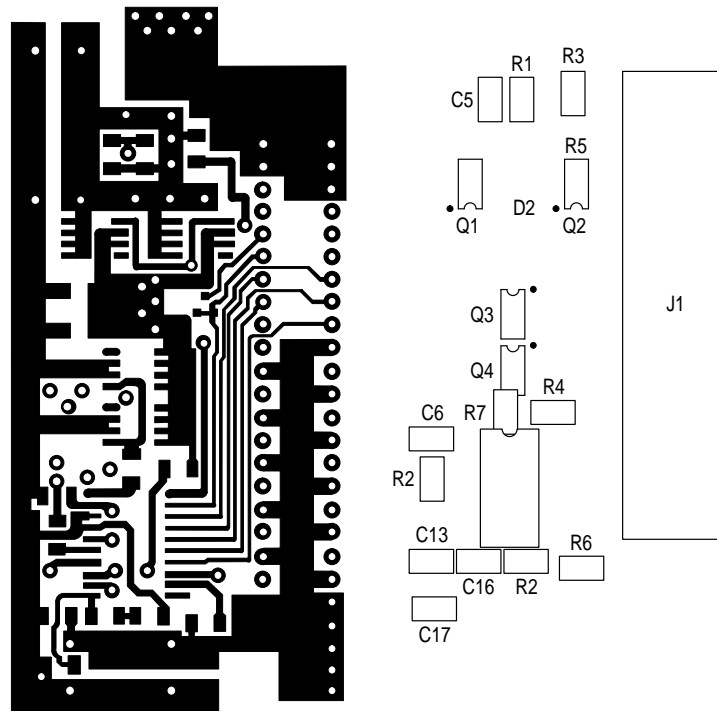
# MC33470
## OUTLINE DIMENSIONS

**DW SUFFIX**
PLASTIC PACKAGE
CASE 751D
(SO–20L)
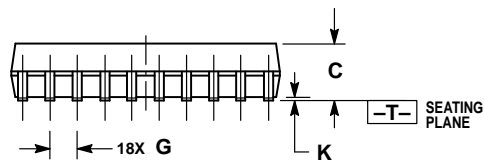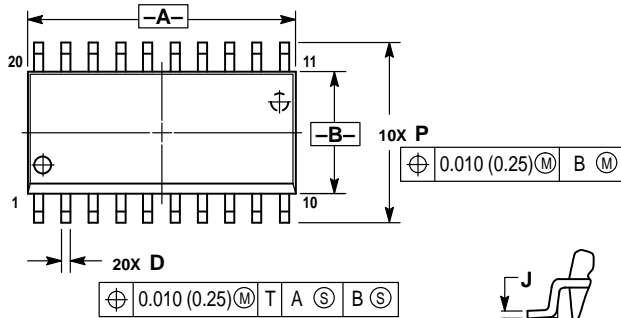
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|-------|-------|
|     | MIN  | MAX  | MIN   | MAX   |
| A   | 12.65 | 12.95 | 0.499 | 0.510 |
| B   | 7.40  | 7.60  | 0.292 | 0.299 |
| C   | 2.35  | 2.65  | 0.093 | 0.104 |
| D   | 0.35  | 0.49  | 0.014 | 0.019 |
| F   | 0.50  | 0.90  | 0.020 | 0.035 |
| G   | 1.27 BSC | | 0.050 BSC | |
| J   | 0.25  | 0.32  | 0.010 | 0.012 |
| K   | 0.10  | 0.25  | 0.004 | 0.009 |
| M   | 0 °   | 7 °   | 0 °   | 7 °   |
| P   | 10.05 | 10.55 | 0.395 | 0.415 |
| R   | 0.25  | 0.75  | 0.010 | 0.029 |

Mfax is a trademark of Motorola, Inc.

**How to reach us:**
**USA/EUROPE/Locations Not Listed**: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

**Customer Focus Center: 1–800–521–6274**

**Mfax**™: RMFAX0@email.sps.mot.com – TOUCHTONE 1–602–244–6609
Motorola Fax Back System      – US & Canada ONLY 1–800–774–1848
     – http://sps.motorola.com/mfax/
  **HOME PAGE**: http://motorola.com/sps/

**JAPAN**: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 141,
4–32–1 Nishi–Gotanda, Shagawa–ku, Tokyo, Japan. 03–5487–8488

**ASIA/PACIFIC**: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

Ⓜ **MOTOROLA**