

## Features

- Fast Read Access Time - 55 ns
- Low Power CMOS Operation
  - 100  $\mu$ A max. Standby
  - 25 mA max. Active at 5 MHz
- JEDEC Standard Packages
  - 32-Lead 600-mil PDIP
  - 32-Lead PLCC
  - 32-Lead TSOP
- 5V  $\pm$  10% Supply
- High-Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100  $\mu$ s/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

## Description

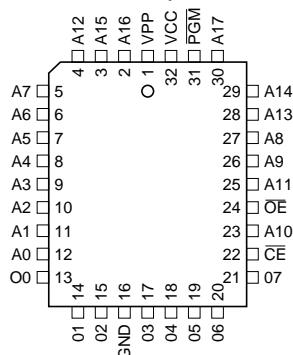
The AT27C020 is a low-power, high performance 2,097,152-bit one-time programmable read only memory (OTP EPROM) organized as 256K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 55 ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

In read mode, the AT27C020 typically consumes 8 mA. Standby mode supply current is typically less than 10  $\mu$ A.

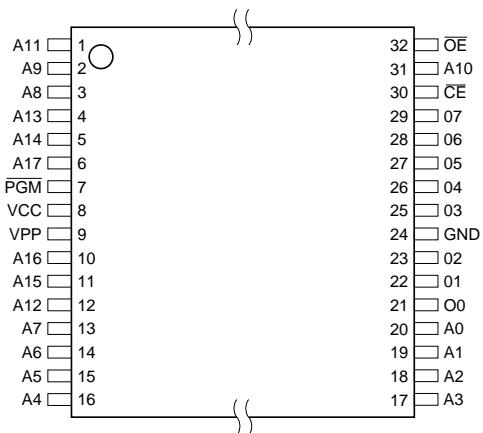
## Pin Configurations

Pin Name	Function
A0 - A17	Addresses
O0 - O7	Outputs
CE	Chip Enable
OE	Output Enable
PGM	Program Strobe

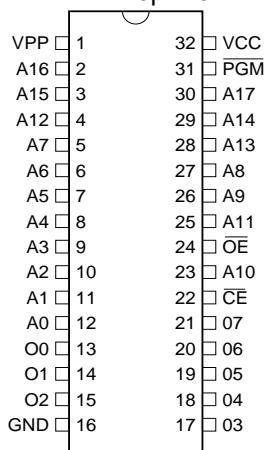
PLCC Top View



TSOP Top View  
Type 1



PDIP Top View



## 2-Megabit (256K x 8) OTP EPROM

## AT27C020

The AT27C020 is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, and TSOP packages. All devices feature two-line control ( $\overline{CE}$ ,  $\overline{OE}$ ) to give designers the flexibility to prevent bus contention.

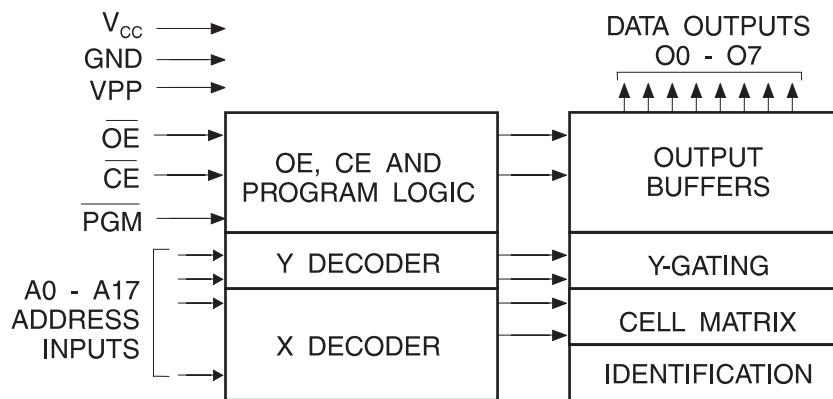
With 256K byte storage capability, the AT27C020 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C020 have additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100  $\mu$ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

## System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu$ F high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the  $V_{CC}$  and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu$ F bulk electrolytic capacitor should be utilized, again connected between the  $V_{CC}$  and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## Block Diagram



## Absolute Maximum Ratings\*

Temperature Under Bias.....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
$V_{PP}$ Supply Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC which may overshoot to +7.0V for pulses of less than 20 ns.

## Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	$A_i$	$V_{PP}$	Outputs
Read	$V_{IL}$	$V_{IL}$	X <sup>(1)</sup>	$A_i$	X	$D_{OUT}$
Output Disable	X	$V_{IH}$	X	X	X	High Z
Standby	$V_{IH}$	X	X	X	X	High Z
Rapid Program <sup>(2)</sup>	$V_{IL}$	$V_{IH}$	$V_{IL}$	$A_i$	$V_{PP}$	$D_{IN}$
PGM Verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	$A_i$	$V_{PP}$	$D_{OUT}$
PGM Inhibit	$V_{IH}$	X	X	X	$V_{PP}$	High Z
Product Identification <sup>(4)</sup>	$V_{IL}$	$V_{IL}$	X	$A9 = V_H^{(3)}$ $A0 = V_{IH}$ or $V_{IL}$ $A1 - A17 = V_{IL}$	X	Identification Code

Notes: 1. X can be  $V_{IL}$  or  $V_{IH}$ .

2. Refer to Programming Characteristics.

3.  $V_H = 12.0 \pm 0.5V$ .

4. Two identifier bytes may be selected. All  $A_i$  inputs are held low ( $V_{IL}$ ), except A9 which is set to  $V_H$  and A0 which is toggled low ( $V_{IL}$ ) to select the Manufacturer's Identification byte and high ( $V_{IH}$ ) to select the Device Code byte.

## DC and AC Operating Conditions for Read Operation

		AT27C020				
		-55	-70	-90	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C				
	Ind.	-40°C - 85C				
V <sub>CC</sub> Power Supply		5V ± 10%				

## DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> (Com., Ind.)		±1.0	µA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub> (Com., Ind.)		±5.0	µA
I <sub>PP</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	V <sub>PP</sub> = V <sub>CC</sub>		±10	µA
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	I <sub>SB1</sub> (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	µA
		I <sub>SB2</sub> (TTL), $\overline{CE} = 2.0$ to $V_{CC} + 0.5V$		1.0	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz, I <sub>OUT</sub> = 0 mA, $\overline{CE} = V_{IL}$		25	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 µA	2.4		V

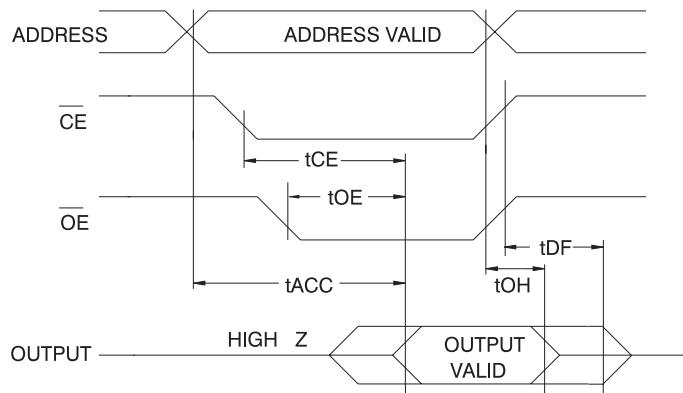
Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.  
 2. V<sub>PP</sub> may be connected directly to V<sub>CC</sub> except during programming. The supply current would then be the sum of I<sub>CC</sub> and I<sub>PP</sub>.

## AC Characteristics for Read Operation

Symbol	Parameter	Condition	AT27C020										Units	
			-55		-70		-90		-12		-15			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t <sub>ACC</sub> <sup>(3)</sup>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		55		70		90		120		150	ns	
t <sub>CE</sub> <sup>(2)</sup>	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		55		70		90		120		150	ns	
t <sub>OE</sub> <sup>(2)(3)</sup>	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		20		30		35		35		40	ns	
t <sub>DF</sub> <sup>(4)(5)</sup>	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			18		20		20		30		40	ns	
t <sub>OH</sub>	Output Hold from Address, $\overline{CE}$ or $OE$ , whichever occurred first		7		7		0		0		0		ns	

Note: 1. 2, 3, 4, 5. See AC Waveforms for Read Operation diagram.

## AC Waveforms for Read Operation<sup>(1)</sup>

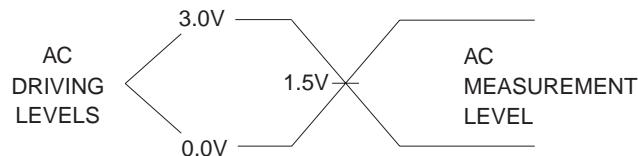


Notes:

1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2.  $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
3.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

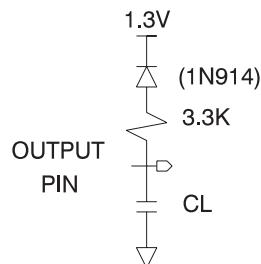
## Input Test Waveforms and Measurement Levels

For -55 devices only:

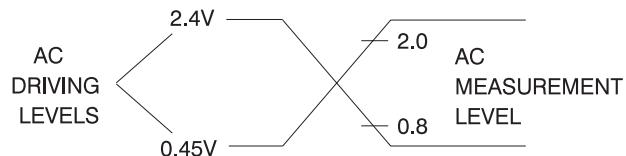


$t_R, t_F < 5$  ns (10% to 90%)

## Output Test Load<sup>(1)</sup>



For -70,-90,-12,-15 devices only:



$t_R, t_F < 20$  ns (10% to 90%)

Note:

1.  $CL = 100$  pF including jig capacitance except -55 devices where  $CL = 30$  pF.

## Pin Capacitance

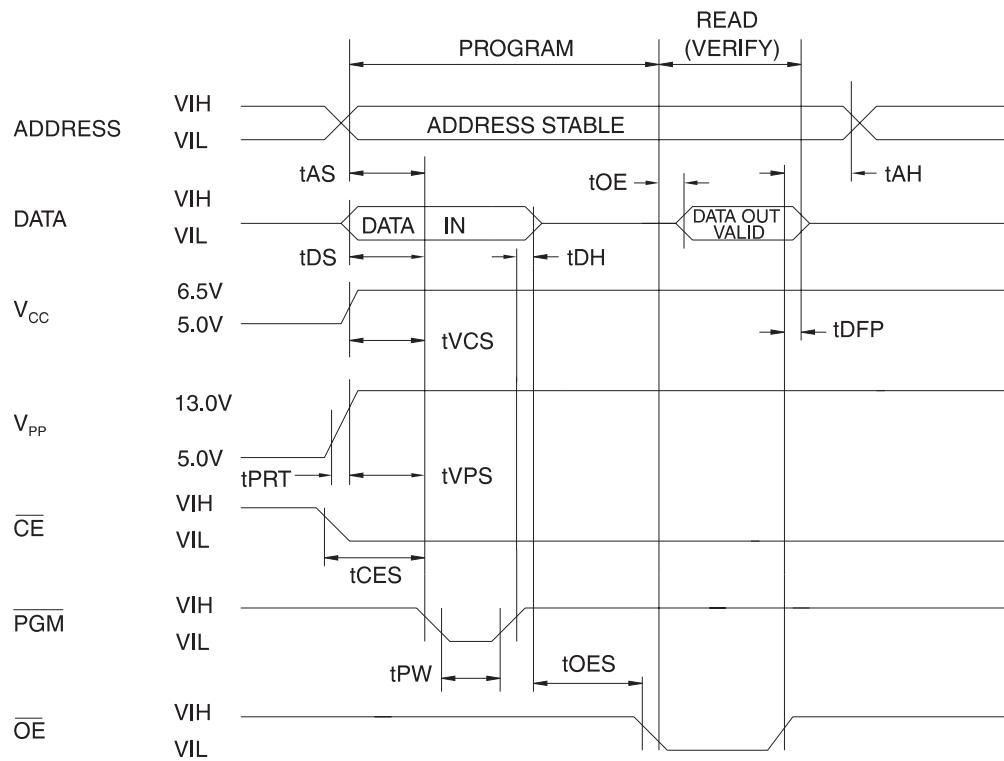
$f = 1$  MHz,  $T = 25^\circ\text{C}$ <sup>(1)</sup>

	Typ	Max	Units	Conditions
$C_{IN}$	4	8	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

Note:

1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## Programming Waveforms (1)



Notes:

1. The Input Timing reference is 0.8V for V<sub>IL</sub> and 2.0V for V<sub>IH</sub>.
2. t<sub>OE</sub> and t<sub>DFP</sub> are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C020, a 0.1  $\mu$ F capacitor is required across V<sub>PP</sub> and ground to suppress voltage transients.

## DC Programming Characteristics

T<sub>A</sub> = 25  $\pm$  5°C, V<sub>CC</sub> = 6.5  $\pm$  0.25V, V<sub>PP</sub> = 13.0  $\pm$  0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = V <sub>IL</sub> , V <sub>IH</sub>		$\pm 10$	$\mu$ A
V <sub>IL</sub>	Input Low Level		-0.6	0.8	V
V <sub>IH</sub>	Input High Level		2.0	V <sub>CC</sub> + 1.0	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 $\mu$ A	2.4		V
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Program and Verify)			40	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
V <sub>ID</sub>	A9 Product Identification Voltage		11.5	12.5	V

## AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Condition <sup>(1)</sup>	Limits		Units
			Min	Max	
$t_{AS}$	Address Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns. Input Pulse Levels: 0.45V to 2.4V Input Timing Reference Level: 0.8V to 2.0V Output Timing Reference Level: 0.8V to 2.0V	2		μs
$t_{CES}$	$\overline{CE}$ Setup Time		2		μs
$t_{OES}$	$\overline{OE}$ Setup Time		2		μs
$t_{DS}$	Data Setup Time		2		μs
$t_{AH}$	Address Hold Time		0		μs
$t_{DH}$	Data Hold Time		2		μs
$t_{DFP}$	$\overline{OE}$ High to Output Float Delay <sup>(2)</sup>		0	130	ns
$t_{VPS}$	$V_{PP}$ Setup Time		2		μs
$t_{VCS}$	$V_{CC}$ Set up Time		2		μs
$t_{PW}$	$\overline{PGM}$ Program Pulse Width <sup>(3)</sup>		95	105	μs
$t_{OE}$	Data Valid from $\overline{OE}$			150	ns
$t_{PRT}$	$V_{PP}$ Pulse Rise Time During Programming		50		ns

Notes:

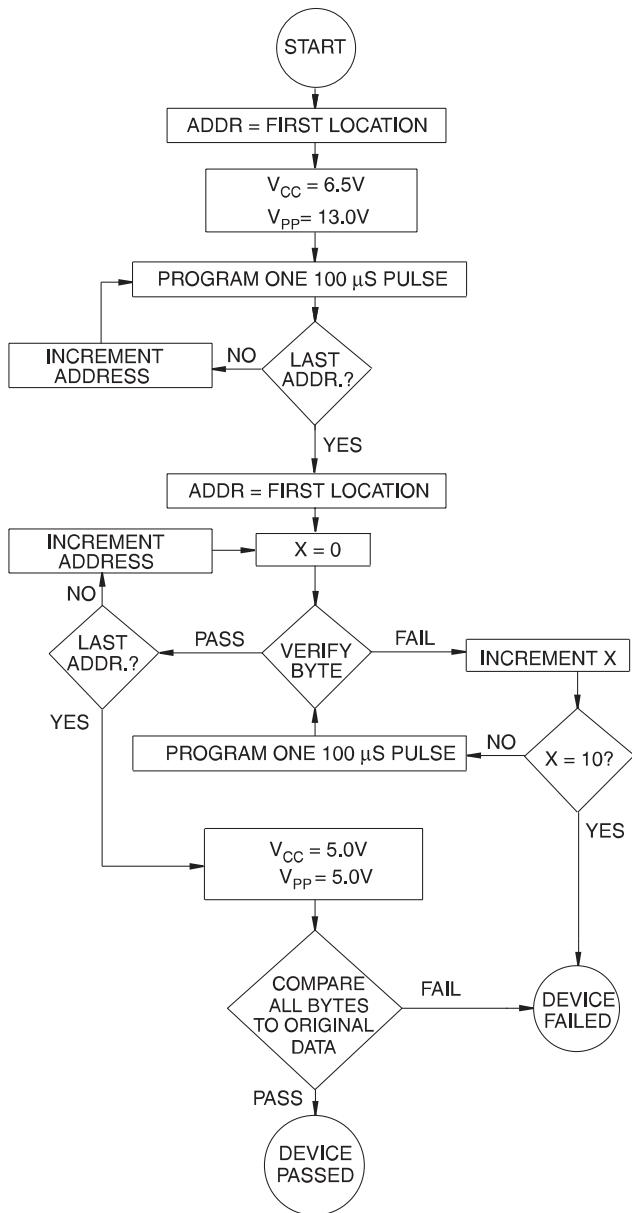
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 μs ± 5%.

## Atmel's 27C020 Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	0	1	1	0	86

## Rapid Programming Algorithm

A 100  $\mu$ s PGM pulse width is used to program. The address is set to the first location.  $V_{CC}$  is raised to 6.5V and  $V_{PP}$  is raised to 13.0V. Each address is first programmed with one 100  $\mu$ s PGM pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100  $\mu$ s pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $V_{PP}$  is then lowered to 5.0V and  $V_{CC}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



## Ordering Information

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	25	0.1	AT27C020-55JC AT27C020-55PC AT27C020-55TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-55JI AT27C020-55PI AT27C020-55TI	32J 32P6 32T	Industrial (-40°C to 85°C)
70	25	0.1	AT27C020-70JC AT27C020-70PC AT27C020-70TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-70JI AT27C020-70PI AT27C020-70TI	32J 32P6 32T	Industrial (-40°C to 85°C)
90	25	0.1	AT27C020-90JC AT27C020-90PC AT27C020-90TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-90JI AT27C020-90PI AT27C020-90TI	32J 32P6 32T	Industrial (-40°C to 85°C)
120	25	0.1	AT27C020-12JC AT27C020-12PC AT27C020-12TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-12JI AT27C020-12PI AT27C020-12TI	32J 32P6 32T	Industrial (-40°C to 85°C)
150	25	0.1	AT27C020-15JC AT27C020-15PC AT27C020-15TC	32J 32P6 32T	Commercial (0°C to 70°C)
	25	0.1	AT27C020-15JI AT27C020-15PI AT27C020-15TI	32J 32P6 32T	Industrial (-40°C to 85°C)

## Package Type

32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)