

AN5829S

Sound multiplex decoder IC for the U.S. televisions

Overview

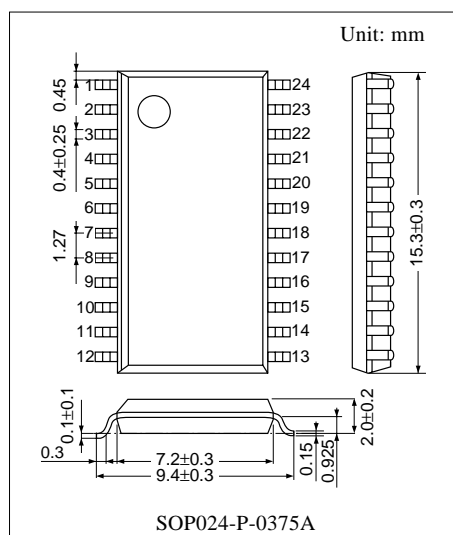
The AN5829S is a multiplex sound demodulation IC dedicated to the U.S. television and incorporates a bi-directional I²C interface (adjustment, mode SW), an AGC circuit and external stereo input switches (2 systems).

Features

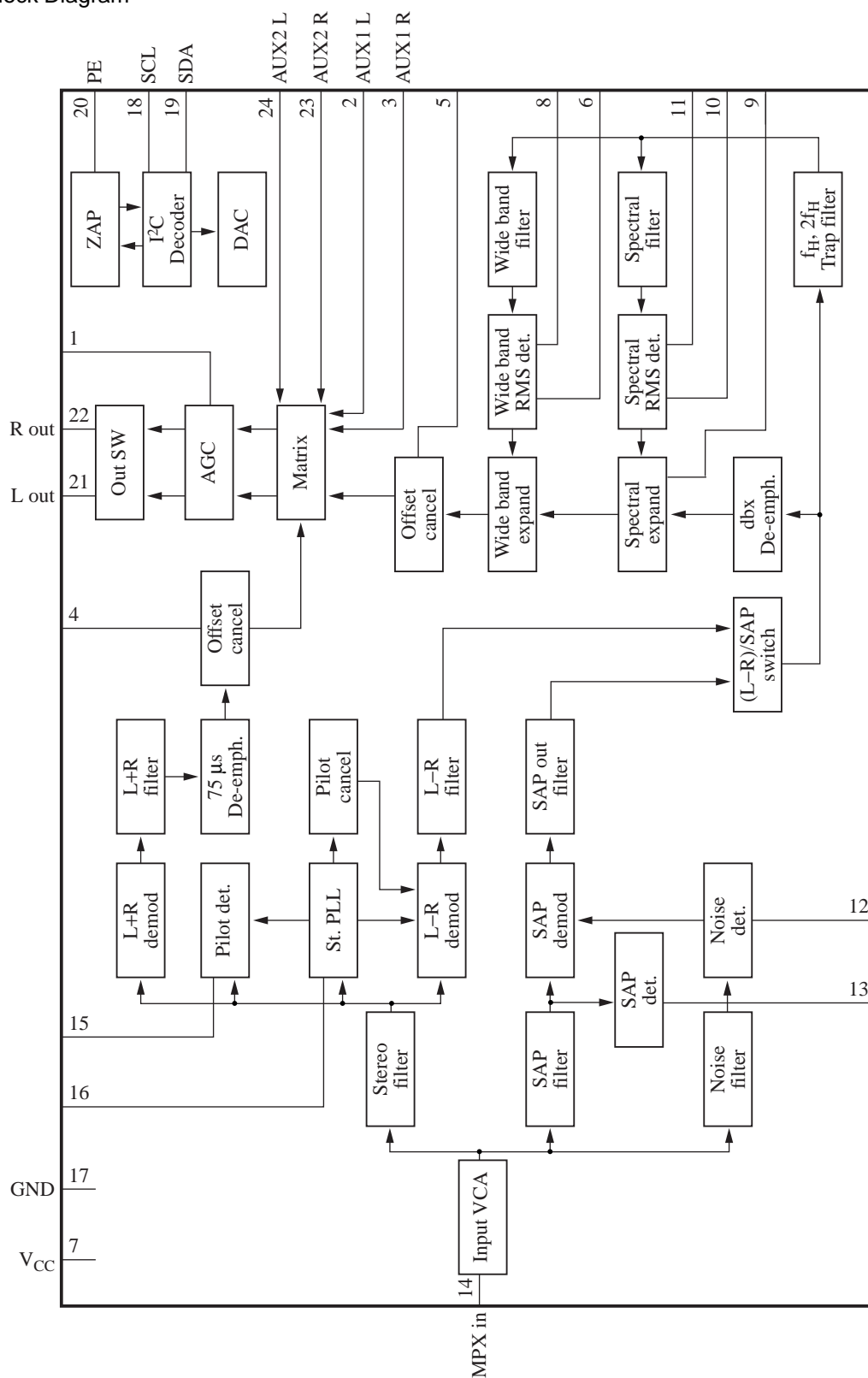
- Stereo demodulation, SAP demodulation, dbx noise reduction, AGC, external stereo input SW and I²C bus interface are integrated in a single chip
- Bi-directional I²C bus makes it possible to monitor MPX input level, separation adjustment (3 places), mode changeover and receiving status.
- Eliminated external parts (multi-sound block: 21 pieces → 14 pieces)
- Lower power dissipation ($V_{CC} = 5\text{ V}$, $I_{TOT} = 18\text{ mA}$)

Applications

- Televisions and VCRs for the North American market



■ Block Diagram



■ Pin Descriptions

| Pin No. | Description | Pin No. | Description |
|---------|---------------------------------|---------|------------------------|
| 1 | AGC timing | 13 | SAP carrier detection |
| 2 | External input 1 L-ch | 14 | Composite input |
| 3 | External input 1 R-ch | 15 | Pilot signal detection |
| 4 | 75 μ s filter offset cancel | 16 | Stereo PLL filter |
| 5 | dbx offset cancel | 17 | GND |
| 6 | Wideband timing | 18 | SCL |
| 7 | V _{CC} | 19 | SDA |
| 8 | Wideband level sensor input | 20 | PE for ZAP |
| 9 | Spectral filter | 21 | L-ch output |
| 10 | Spectral timing | 22 | R-ch output |
| 11 | Spectral level sensor input | 23 | External input 2 R-ch. |
| 12 | SAP noise level detection | 24 | External input 2 L-ch. |

■ Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|----------------------------------|------------------|-------------|------|
| Supply voltage | V _{CC} | 6.0 | V |
| Supply current | I _{CC} | 25 | mA |
| Power dissipation *2 | P _D | 150 | mW |
| Operating ambient temperature *1 | T _{opr} | −20 to +75 | °C |
| Storage temperature *1 | T _{stg} | −55 to +125 | °C |

Note) The use of this IC, which builds in dbx-TV noise reduction, requires a license agreement with THAT Corporation.

*1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

*2: T_a = 75°C

■ Recommended Operating Range

| Parameter | Symbol | Range | Unit |
|----------------|-----------------|------------|------|
| Supply voltage | V _{CC} | 4.5 to 5.5 | V |

■ Electrical Characteristics at $V_{CC} = 5\text{ V}$, NR: On, $T_a = 25^\circ\text{C}$

Input level (at 100% modulation) L+R: 75 mV[rms] (pre-emphasis off)

L-R: 150 mV[rms] (dbx noise reduction off)

Pilot: 15 mV[rms]

SAP: 45 mV[rms] (dbx noise reduction off)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|------------------------------------|---------------|--|------|------|-----|---------|
| Total circuit current | I_{CC} | No signal | 11 | 18 | 25 | mA |
| Mono output level | $V_{0(MON)}$ | $f = 1\text{ kHz}$, (mono) 100%mod | 430 | 480 | 530 | mV[rms] |
| Mono frequency characteristics-1 | $V_{1(MON)}$ | $f = 300\text{ Hz}$, (mono) 30%mod | -0.5 | 0 | 0.5 | dB |
| Mono frequency characteristics-2 | $V_{2(MON)}$ | $f = 8\text{ kHz}$, (mono) 30%mod | -1.2 | -0.1 | 0.7 | dB |
| Mono distortion ratio | $THD_{(MON)}$ | $f = 1\text{ kHz}$, (mono) 100%mod | — | — | 0.7 | % |
| Mono noise level | $V_{N(MON)}$ | Input short-circuit, BPF (A curve) | — | — | -60 | dBV |
| (L), (R) output voltage difference | $V_{LR(MON)}$ | $f = 1\text{ kHz}$, (mono) 100%mod | -0.5 | 0 | 0.5 | dB |
| Stereo output level | $V_{0(ST)}$ | $f = 1\text{ kHz}$, (L(R)-only) 100%mod | 380 | 480 | 580 | mV[rms] |
| Stereo frequency characteristics-1 | $V_{1(ST)}$ | $f = 300\text{ Hz}$, (L(R)-only) 30%mod | -0.7 | 0 | 0.7 | dB |
| Stereo frequency characteristics-2 | $V_{2(ST)}$ | $f = 3\text{ kHz}$, (L(R)-only) 30%mod | -1 | 0 | 1 | dB |
| Stereo frequency characteristics-3 | $V_{3(ST)}$ | $f = 8\text{ kHz}$, (L(R)-only) 30%mod | -2.5 | -0.5 | 1.5 | dB |
| Stereo distortion ratio | $THD_{(ST)}$ | $f = 1\text{ kHz}$, (L(R)-only) 100%mod | — | — | 1 | % |
| Stereo noise level | $V_{N(ST)}$ | $f = 15.73\text{ kHz}$, (f_H), 15 mV[rms] f_H , 2 f_H Trap+BPF | — | — | -60 | dBV |
| Stereo discrimination level | $V_{TH(ST)}$ | $f = 15.73\text{ kHz}$ (f_H) | 4 | 8 | 13 | mV[rms] |
| Stereo discrimination hysteresis | $V_{HY(ST)}$ | $f = 15.73\text{ kHz}$ (f_H) | 0.5 | — | 5 | dB |
| SAP output level | $V_{0(SAP)}$ | $f = 1\text{ kHz}$, (SAP) 100%mod | 370 | 500 | 680 | mV[rms] |
| SAP frequency characteristics-1 | $V_{1(SAP)}$ | $f = 300\text{ Hz}$, (SAP) 30%mod | -1 | 0 | 1 | dB |
| SAP frequency characteristics-2 | $V_{2(SAP)}$ | $f = 3\text{ kHz}$, (SAP) 30%mod | -2.5 | -0.5 | 1 | dB |
| SAP distortion ratio | $THD_{(SAP)}$ | $f = 1\text{ kHz}$, (SAP) 100% | — | — | 1.5 | % |
| SAP noise level | $V_{N(SAP)}$ | $f = 78.7\text{ kHz}$, ($5f_H$), $V = 45\text{ mV[rms]}$, BPF | — | — | -70 | dBV |
| SAP discrimination level | $V_{TH(SAP)}$ | $f = 78.7\text{ kHz}$, ($5f_H$) | 11 | — | 26 | mV[rms] |
| SAP discrimination hysteresis | $V_{HY(SAP)}$ | $f = 78.7\text{ kHz}$, ($5f_H$) | 0.5 | — | 5 | dB |
| SAP → Stereo crosstalk | C_{T1} | (SAP) 1 kHz, 100%mod (Stereo) pilot-signal | — | — | -50 | dB |
| Stereo → SAP crosstalk | C_{T2} | (Stereo) 1 kHz, 100%mod (SAP) carrier-signal | — | — | -50 | dB |
| SAP → Mono crosstalk | C_{T3} | (SAP) 1 kHz, 100%mod | — | — | -50 | dB |
| Mono → SAP crosstalk | C_{T4} | (Mono) 1 kHz, 100%mod (SAP) carrier-signal | — | — | -56 | dB |
| AUX 1, AUX 2 to INT crosstalk | C_{T5} | $f = 1\text{ kHz}$, $V_{IN} = 500\text{ mV[rms]}$ | — | — | 50 | dB |
| INT, AUX 2 to AUX 1 crosstalk | C_{T6} | INT: (mono) 1 kHz, 100%mod EXT: $f = 1\text{ kHz}$, 500 mV[rms] | — | — | 50 | dB |
| INT, AUX 1 to AUX 2 crosstalk | C_{T7} | INT: (mono) 1 kHz, 100%mod EXT: $f = 1\text{ kHz}$, 500 mV[rms] | — | — | 50 | dB |

■ Electrical Characteristics at $V_{CC} = 5\text{ V}$, NR: On, $T_a = 25^\circ\text{C}$ (continued)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|------------|---|-----|-----|-----|---------|
| AGC gain 1*1 | V_{AGC1} | $f = 1\text{ kHz}$, $V_{IN(EXT)} = 50\text{ mV[rms]}$ | 67 | 100 | 140 | mV[rms] |
| AGC gain 2*1 | V_{AGC2} | $f = 1\text{ kHz}$, $V_{IN(EXT)} = 500\text{ mV[rms]}$ | 180 | 270 | 390 | mV[rms] |
| I²C interface | | | | | | |
| Sink current at ACK | I_{ACK} | Maximum pin 2 sink current at ACK | 1 | 2 | 20 | mA |
| SCL, SDA signal input high level | V_{IHI} | — | 3.5 | — | 5.0 | V |
| SCL, SDA signal input low level | V_{ILO} | — | 0 | — | 0.9 | V |
| Input available maximum frequency | f_{Imax} | — | — | — | 100 | kbit/s |

Note) *1: 00H register: D7 = 0, D6 = 1

• Design reference data

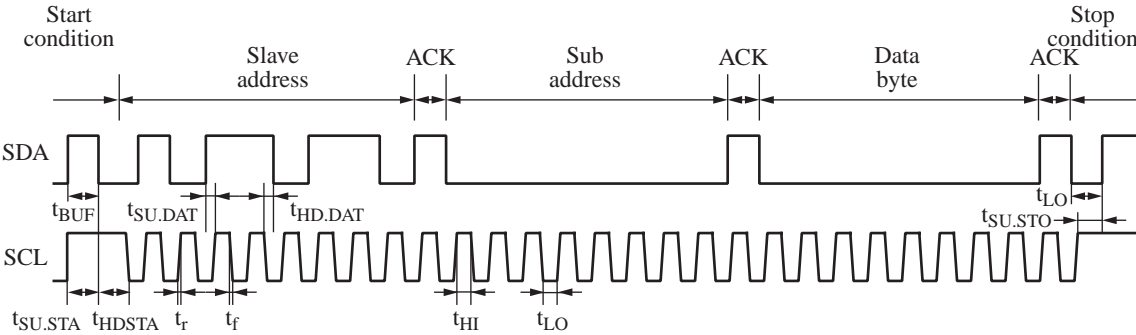
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------|---------------|---|-----|-----|-----|------|
| Stereo separation (100%)-1 | Sep_{100-1} | $f = 300\text{ Hz}$, (L(R)-only) 100%mod | 20 | 35 | — | dB |
| Stereo separation (100%)-2 | Sep_{100-2} | $f = 1\text{ kHz}$, (L(R)-only) 100 %mod | 17 | 28 | — | dB |
| Stereo separation (100%)-3 | Sep_{100-3} | $f = 3\text{ kHz}$, (L(R)-only) 100%mod | 20 | 35 | — | dB |
| Stereo separation (100%)-4 | Sep_{100-4} | $f = 8\text{ kHz}$, (L(R)-only) 100%mod | 10 | 18 | — | dB |
| Stereo separation (30%)-1 | Sep_{30-1} | $f = 300\text{ Hz}$, (L(R)-only) 30%mod | 22 | 35 | — | dB |
| Stereo separation (30%)-2 | Sep_{30-2} | $f = 1\text{ kHz}$, (L(R)-only) 30%mod | 20 | 35 | — | dB |
| Stereo separation (30%)-3 | Sep_{30-3} | $f = 3\text{ kHz}$, (L(R)-only) 30%mod | 22 | 35 | — | dB |
| Stereo separation (30%)-4 | Sep_{30-4} | $f = 8\text{ kHz}$, (L(R)-only) 30%mod | 14 | 22 | — | dB |
| Stereo separation (10%)-1 | Sep_{10-1} | $f = 300\text{ Hz}$, (L(R)-only) 10%mod | 20 | 35 | — | dB |
| Stereo separation (10%)-2 | Sep_{10-2} | $f = 1\text{ kHz}$, (L(R)-only) 10%mod | 20 | 35 | — | dB |
| Stereo separation (10%)-3 | Sep_{10-3} | $f = 3\text{ kHz}$, (L(R)-only) 10%mod | 20 | 30 | — | dB |
| Stereo separation (10%)-4 | Sep_{10-4} | $f = 8\text{ kHz}$, (L(R)-only) 10%mod | 14 | 22 | — | dB |

I²C interface

| | | | | | | |
|-----------------------------|--------------|---|------|---|------|----|
| Bus free before start | t_{BUF} | — | 4.0 | — | — | μs |
| Start condition set-up time | $t_{SU,STA}$ | — | 4.0 | — | — | μs |
| Start condition hold time | $t_{HD,STA}$ | — | 4.0 | — | — | μs |
| Low period SCL, SDA | t_{LO} | — | 4.0 | — | — | μs |
| High period SCL | t_{HI} | — | 4.0 | — | — | μs |
| Rise time SCL, SDA | t_r | — | — | — | 1.0 | μs |
| Fall time SCL, SDA | t_f | — | — | — | 0.35 | μs |
| Data set-up time (write) | $t_{SU,DAT}$ | — | 0.25 | — | — | μs |
| Data hold time (write) | $t_{HD,DAT}$ | — | 0.3 | — | — | μs |
| Acknowledge set-up time | $t_{SU,ACK}$ | — | — | — | 3.5 | μs |
| Acknowledge hold time | $t_{HD,ACK}$ | — | 0 | — | — | μs |
| Stop condition set-up time | $t_{SU,STO}$ | — | 4.0 | — | — | μs |

■ Electrical Characteristics at $V_{CC} = 5\text{ V}$, NR: On, $T_a = 25^\circ\text{C}$ (continued)



■ Terminal Equivalent Circuits

| Pin No. | Equivalent circuit | Description | DC voltage (V) |
|---------|--------------------|--|----------------|
| 1 | | AGC: AGC level sensor pin | 0.5 to 2.0 |
| 2 | | AUXIL: External input1 L-ch input pin | 2.2 |
| 3 | | AUXIR: External input 1 R-ch input pin | 2.2 |

■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | DC voltage (V) |
|---------|--------------------|--|----------------|
| 4 | | OFCAN1: 75 μ s filter output Offset cancel pin | 2.2 |
| 5 | | OFCAN2: dbx output Offset cancel pin | 2.2 |
| 6 | | WBTIME: Wide expander effective value detection recovery time set-up pin | 2.2 |
| 7 | — | V_{CC} : V_{CC} pin | V_{CC} |
| 8 | | WBDET: RMS detection circuit input pin of wide band expander | 2.2 |

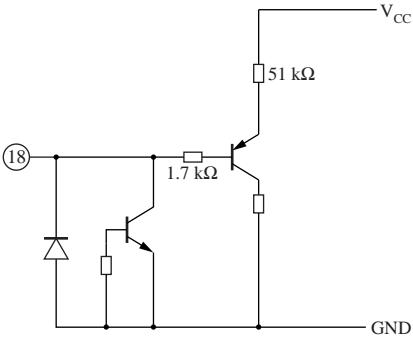
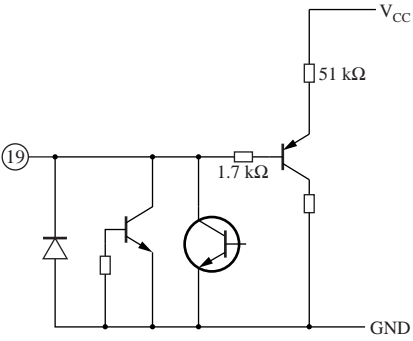
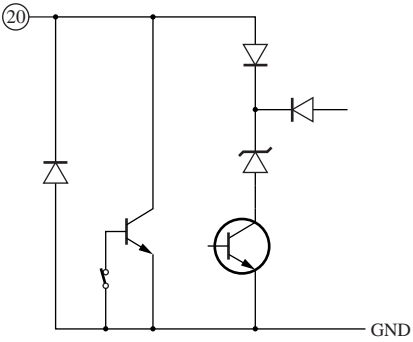
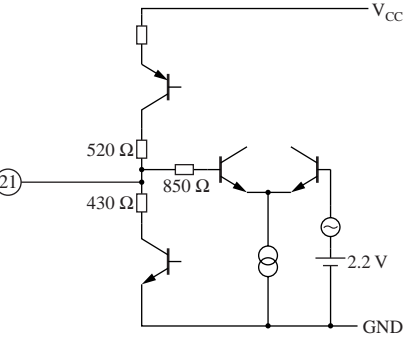
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | DC voltage (V) |
|---------|--------------------|--|---------------------|
| 9 | | SPEFIL: Variable de-emphasis level adjusting pin | 2.2 |
| 10 | | SPETIME: RMS detection recovery time pin of variable de-emphasis | 0.2 |
| 11 | | SPEDET: RMS detection circuit input pin of variable de-emphasis | 2.2 |
| 12 | | NOISEDET: Noise detecting pin of SAP malfunction-prevention-circuit(Mute SAP de-modulation at detecting noise.) | $V_{CC} - 2 V_{BE}$ |

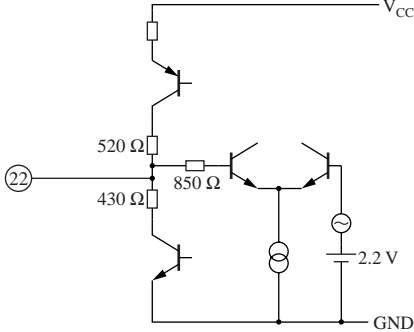
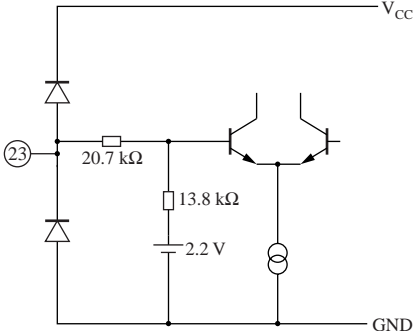
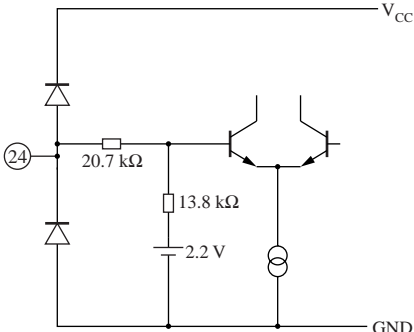
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | DC voltage (V) |
|---------|--------------------|---|------------------------|
| 13 | | SAPDET: SAP signal carrier level detection pin | $V_{CC} - 2 V_{BE}$ |
| 14 | | MPXIN: Composite signal input pin | 2.2 |
| 15 | | PILOTDET: Stereo pilot signal detection pin | $2.2V_{CC} - 2 V_{BE}$ |
| 16 | | PLL: Stereo PLL low pass filter connection pin | $V_{CC} - 2 V_{BE}$ |
| 17 | — | GND: GND pin | 0 |

■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | DC voltage (V) |
|---------|---|---|----------------|
| 18 |  | SCL: I ² C bus clock input pin | — |
| 19 |  | SDA: I ² C bus data input pin | 2.2 |
| 20 |  | PE: Current application input pin for ZAP at final test | — |
| 21 |  | L-OUT: L-ch. line out output pin | 2.2 |

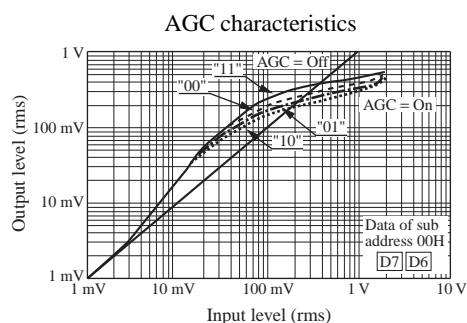
■ Terminal Equivalent Circuits (continued)

| Pin No. | Equivalent circuit | Description | DC voltage (V) |
|---------|---|---|----------------|
| 22 |  | R OUT: R-ch. line out output pin | 2.2 |
| 23 |  | AUX2R: External input 2 L-ch. input pin | 2.2 |
| 24 |  | AUX2L: External input 2 R-ch. input pin | 2.2 |

■ Usage Notes

1. AGC set-up method

By turning on AGC, the AGC performs 0 dB at a small signal input, Boost at a medium signal and gain reduction at a big signal. It can also control the I/O characteristics of AGC by I²C as shown below:



2. Guarantee of I²C operating temperature

I²C bus control operation at an operating ambient temperature is theoretically guaranteed based on IC design by means of the inspection using about 50% faster clock speed at the normal temperature ($T_a = 25^\circ\text{C}$).

Namely it is a theoretical value based on IC design, therefore it is not guaranteed at the shipping inspection because the inspection under a high and low temperature is not conducted.

3. Electrostatic breakdown

Pay attention to the following levels:

Pin 6: 200 pF, 130 V

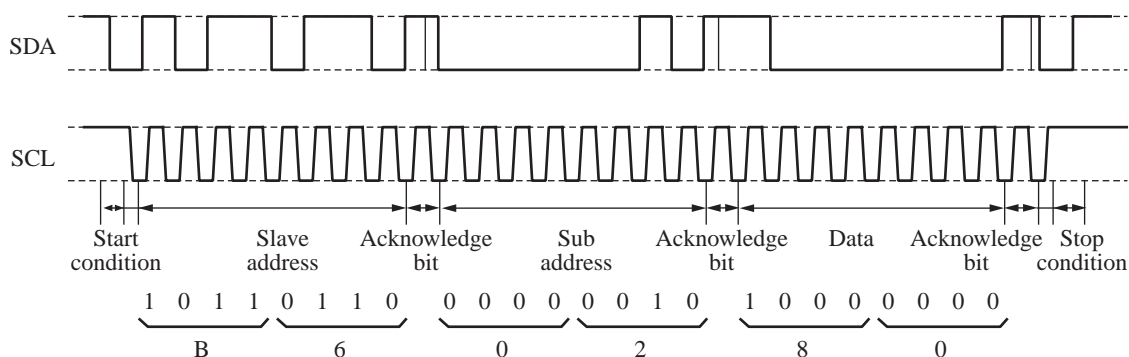
Pin 10: 200 pF, 150 V

Pin 22: 200 pF, 190 V

■ Technical Information

[1] I²C bus

1. Receiving mode



Transmission message

As transfer messages, SCL and SDA are transferred synchronously and serially. SCL is a constant clock frequency and SDA is address data for controlling a receiving side and is sent in parallel by synchronizing with SCL. Data are in principle sent by 8-bit 3-octet (byte) and there exists an acknowledge bit per octet. The frame structure is mentioned below:

1) Start condition

When SDA becomes from high to low at SCL = high, the receiver gets ready to receive.

2) Stop condition

When SDA becomes from low to high at SCL = high, the receiver stops receiving.

3) Slave address

Specified for each device. If any addresses of other devices are sent, receiving will be stopped.

4) Sub-address

Specified for each function.

5) Data

Data for controlling

6) Acknowledge bit

This is the bit that informs the master of data reception every octet. The master sends the high signal and the receiver sends back the low signal as shown with the dotted line in the above figure, thus the master acknowledges reception on the receiver side. If the low signal is not sent back, the reception will be stopped.

Except for the start and stop conditions, SDA does not change at SCL = high.

■ Technical Information

[1] I²C bus (continued)

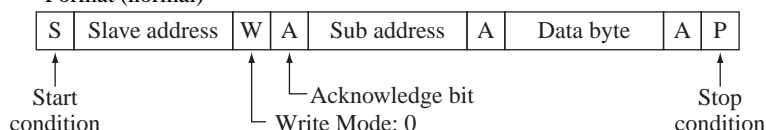
1. Receiving mode (continued)

<I²C of this IC>

- 1) Enhances adjustment-free mechanism of the TV set thanks to DAC control 3 and 9 switches
- 2) Auto-increment function
 - Sub address 0 *: Auto-increment mode
(Data sequential transfer leads to the sequential change of sub address, so that the data is inputted.)
 - Sub address 8 *: Data renewal mode
(With sequential data transfer, data are inputted in the same sub address.)

3) I²C bus protocol

- Slave address
- Format (normal)



- Auto-increment mode/data renewal mode



- 4) As the initial state of DAC is not guaranteed, never fail to input the following data in a power on mode.

"06" register: "04"

"00" register: adjustment data

"01" register: adjustment data

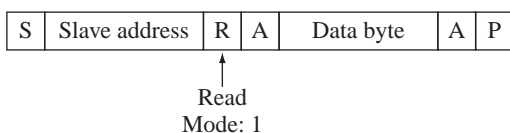
"02" register: "00"

"05" register: adjustment data

2. Transmission mode (read mode)

I²C bus protocol

- Slave address: 10110111 (B7H)
- Format



■ Technical Information (continued)

[1] I²C bus (continued)

- Sub address byte and data byte format

Write mode (slave add.: 10110110)

| Sub address | Upper MSB | | Data byte | | | | | Lower LSB | |
|-------------|---|------------------------------------|--|----|---|----|-------------------|----------------------|--|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| "00" | ← AGC adj. → | | ← Input level adjustment → | | | | | | |
| "01" | AUXselect 0: AUX1 1: AUX2 | AUX SW 0: Off 1: On | ← High frequency separation adjustment → | | | | | | |
| "02" | Adj.: 1 → On L: VGA out R: VCO f _H | Mute: 1 → On L: Mute R: Mute | AGC 1 → On | 0 | FMONO: 1 → On L: L+R R: L+R | 0 | St/SAP 0 → SAP | (L+R)/SAP 0 → SAP | |
| "05" | * | * | * | * | ← Low frequency separation adjustment → | | | | |
| "06" | * | * | * | * | * | * | 0 | 0 | |

* = Don't care

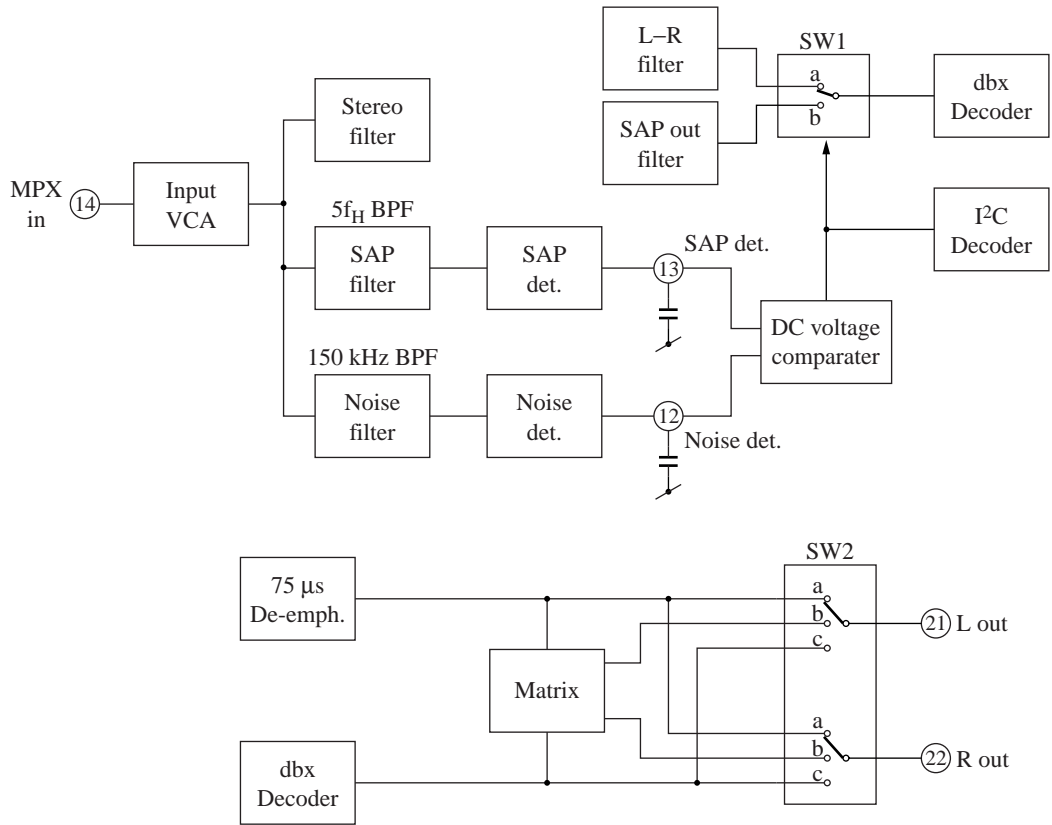
Read mode (slave add.: 10110111)

| Upper MSB | | | Data byte | | | | Lower LSB | |
|-----------------------|---------------------|----|-----------|----|----|----|-----------|--|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Pilot det. 1 → DET | SAP det. 1 → DET | * | * | * | * | * | * | |

* = Don't care

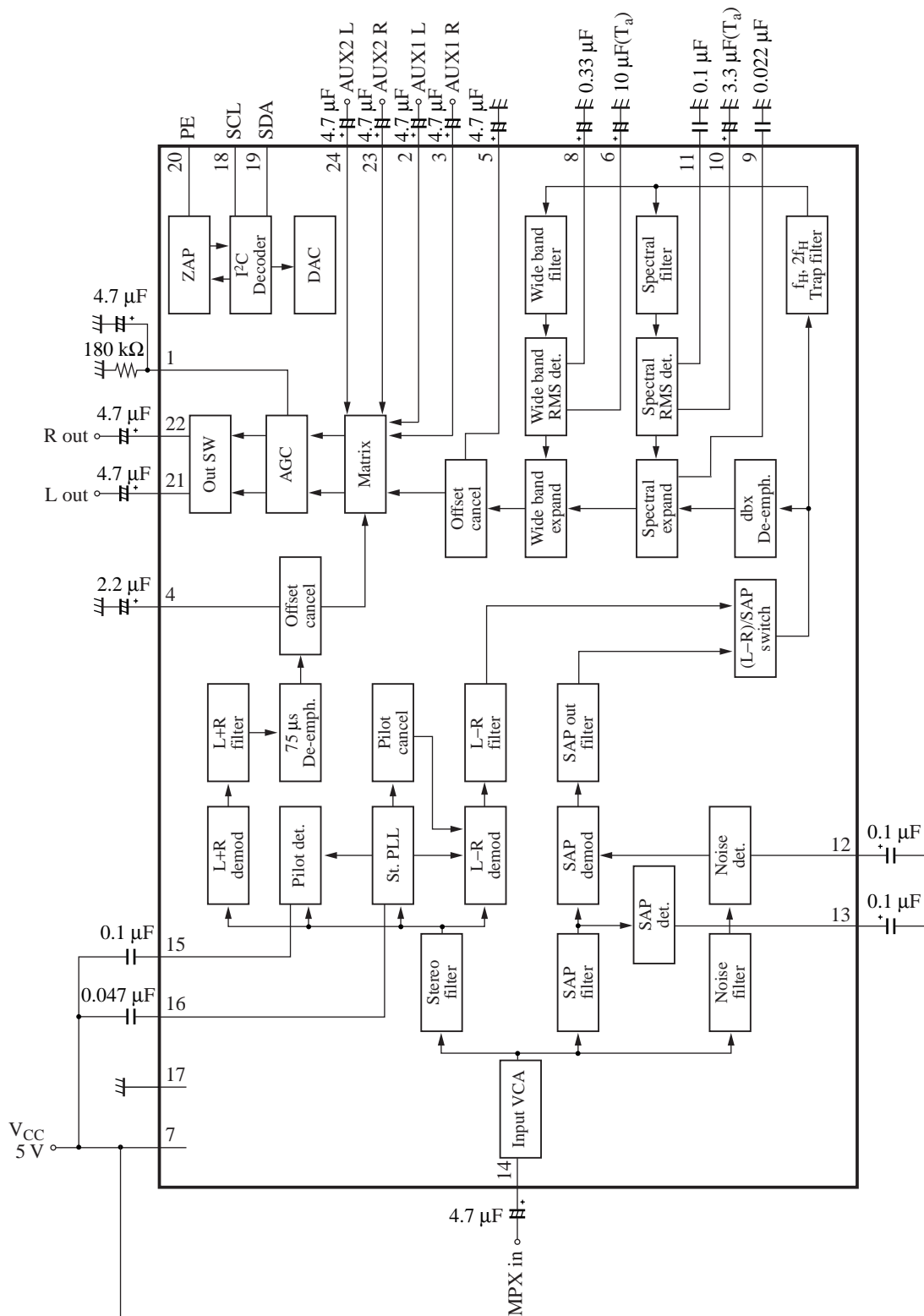
■ Technical Information (continued)

[2] Noise detecting operation in SAP receiving mode



| Pin 14 input | "02" register | Pin 12, pin 13 DC voltage | SW1 | SW2 | I²C SAP det. | Pin 21, pin 22 |
|--------------|---------------|------------------------------|-----|-----|--------------|----------------|
| Noise: Small | "00" | $V_{12} > V_{13}$ | b | c | 3.5 V to 5 V | SAP |
| Noise: Large | "00" | $V_{12} < V_{13}$ | a | a | 0 V to 0.9 V | L+R |

■ Application Circuit Example



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