



## 2.5Gbps PCI Express Passive Switches

### General Description

The MAX4888/MAX4889 high-speed passive switches route PCI Express® (PCIe) data between two possible destinations. The MAX4888 is a quad single-pole/double-throw (4 x SPDT) switch ideally suited for switching two half lanes of PCIe data between two destinations. The MAX4889 is an octal single-pole/double-throw (8 x SPDT) switch ideal for switching four half lanes of PCIe data between four destinations. The MAX4888/MAX4889 feature a single digital control input (SEL) to switch signal paths.

The MAX4888/MAX4889 are fully specified to operate from a single 3.0V to 3.6V power supply and also operate down to +1.65V. The MAX4888 is available in a 3.5mm x 5.5mm, 28-pin TQFN package. The MAX4889 is available in a 3.5mm x 9.0mm, 42-pin TQFN package. Both devices operate over the -40°C to +85°C temperature range.

### Applications

Desktop Computers  
Servers/Storage Area Networks  
Laptops

PCI Express is a registered trademark of PCI-Sig Corp.

### Features

- ◆ Single 1.65V to 3.6V Power-Supply Voltage
- ◆ Low Same-Pair Skew of 7ps
- ◆ Low 120μA (Max) Quiescent Current
- ◆ Supports PCIe Gen I Data Rates
- ◆ Flow-Through Pin Configuration for Ease of Layout
- ◆ Industry-Compatible Pinout
- ◆ Lead-Free Packaging

### Ordering Information/ Selector Guide

PART	PIN-PACKAGE	CONFIGURATION	PKG CODE
MAX4888ETI+	28 TQFN-EP*	Two Half Lanes	T283555-1
MAX4889ETO+	42 TQFN-EP*	Four Half Lanes	T423590M-1

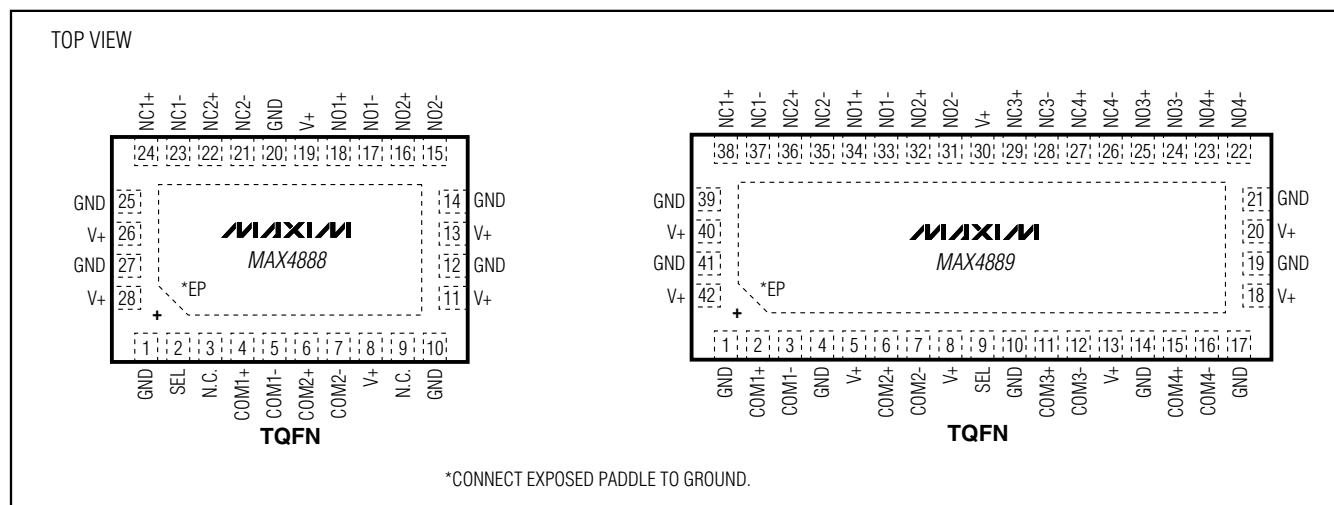
**Note:** All devices are specified over the -40°C to +85°C operating temperature range.

+ Denotes lead-free package.

\*EP = Exposed paddle.

Typical Application Circuit appears at end of data sheet.

### Pin Configurations



## 2.5Gbps PCI Express Passive Switches

### ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

V+	.....-0.3V to +4V
SEL, COM__, NO__, NC__ (Note 1)	.....-0.3V to (V+ + 0.3V)
I COM__ - NO__ I, I COM__ - NC__ I (Note 1)	.....0 to 2V
Continuous Current (COM__ to NO__/NC__)	.....±70mA
Peak Current (COM__ to NO__/NC__)	
(pulsed at 1ms, 10% duty cycle)	.....±70mA
Continuous Current (SEL)	.....±30mA
Peak Current (SEL)	
(pulsed at 1ms, 10% duty cycle)	.....±150mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

28-Pin TQFN (derate 20.8mW/°C above +70°C)	....1666.7mW
42-Pin TQFN (derate 35.7mW/°C above +70°C)	....2857.1mW
Operating Temperature Range	.....-40°C to +85°C
Storage Temperature Range	.....-65°C to +150°C
Lead Temperature (soldering, 10s)	.....+300°C
Junction Temperature	.....+150°C

**Note 1:** Signals on SEL, NO\_\_, NC\_\_ or COM\_\_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(V+ = 3.0V to 3.6V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3.3V, T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>						
Analog-Signal Range	V <sub>COM_</sub> , V <sub>NO_</sub> , V <sub>NC_</sub>		-0.1	(V+ - 1.2)		V
Voltage Between COM and NO/NC	I V <sub>COM_</sub> - V <sub>NO_</sub> I, I V <sub>COM_</sub> - V <sub>NC_</sub> I		0		1.8	V
On-Resistance	R <sub>ON</sub>	V+ = 3.0V, I <sub>COM_</sub> = 15mA, V <sub>NO_</sub> or V <sub>NC_</sub> = 0V, 1.8V		7		Ω
On-Resistance Match Between Pairs of Same Channel	ΔR <sub>ON</sub>	V+ = 3.0V, I <sub>COM_</sub> = 15mA, V <sub>NO_</sub> or V <sub>NC_</sub> = 0V (Notes 3, 4)		0.1	1	Ω
On-Resistance Match Between Channels	ΔR <sub>ON</sub>	V+ = 3.0V, I <sub>COM_</sub> = 15mA, V <sub>NO_</sub> or V <sub>NC_</sub> = 0V (Notes 3, 4)		0.6	2	Ω
On-Resistance Flatness	R <sub>FLAT(ON)</sub>	V+ = 3.0V, I <sub>COM_</sub> = 15mA V <sub>NO_</sub> or V <sub>NC_</sub> = 0V, 1.8V (Notes 4, 5)		0.06	2	Ω
NO_ or NC_ Off-Leakage Current	I <sub>NO_(OFF)</sub> I <sub>NC_(OFF)</sub>	V+ = 3.6V; V <sub>COM_</sub> = 0V, 1.8V; V <sub>NO_</sub> or V <sub>NC_</sub> = 1.8V, 0V	-1		+1	μA
COM_ On-Leakage Current	I <sub>COM_(ON)</sub>	V+ = 3.6V; V <sub>COM_</sub> = 0V, 1.8V; V <sub>NO_</sub> or V <sub>NC_</sub> = V <sub>COM_</sub> or unconnected	-1		+1	μA

# 2.5Gbps PCI Express Passive Switches

MAX4888/MAX4889

## ELECTRICAL CHARACTERISTICS (continued)

(V+ = 3.0V to 3.6V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3.3V, T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC							
Turn-On Time	tON	VNO_ or VNC_ = 1.0V, RL = 50Ω, Figure 1		90	250		ns
Turn-Off Time	tOFF	VNO_ or VNC_ = 1.0V, RL = 50Ω, Figure 1		10	50		ns
Propagation Delay	tPD	RS = RL = 50Ω, unbalanced, Figure 2		50			ps
Output Skew Between Pairs	tSK1	RS = RL = 50Ω, unbalanced; skew between any two pairs, Figure 2		50			ps
Output Skew Between Same Pair	tSK2	RS = RL = 50Ω, unbalanced; skew between two lines on same pair, Figure 2		10			ps
On-Loss	GLOS	RS = RL = 50Ω, unbalanced, Figure 3	1MHz < f < 100MHz	-0.5			dB
			500MHz < f < 1.25GHz	-1.4			
Crosstalk	VCT1	Crosstalk between any two pairs, RS = RL = 50Ω, unbalanced, Figure 3	f = 50MHz	-53			dB
			f = 1.25GHz	-32			
Signaling Data Rate	BR	RS = RL = 50Ω		3.0			Gbps
Off-Isolation	VISO	Signal = 0dBm, RS = RL = 50Ω, Figure 3	f = 10MHz	-56			dB
			f = 1.25GHz	-26			
NO_/NC_ Off-Capacitance	CNO_/NC_(OFF)	Figure 4		1			pF
COM_ On-Capacitance	CCOM_(ON)	Figure 4		2			pF
LOGIC INPUT							
Input-Logic Low	VIL				0.5		V
Input-Logic High	VIH			1.4			V
Input-Logic Hysteresis	VHYST				100		mV
Input Leakage Current	IIN	VSEL = 0V or V+		-1		+1	μA
POWER SUPPLY							
Power-Supply Range	V+			1.65		3.60	V
V+ Supply Current	I+	VSEL = 0V or V+	MAX4888		60		μA
			MAX4889		120		

**Note 2:** All units are 100% production tested at T<sub>A</sub> = +85°C. Limits over the operating temperature range are guaranteed by design and characterization and are not production tested.

**Note 3:** ΔR<sub>ON</sub> = R<sub>ON</sub> (MAX) - R<sub>ON</sub> (MIN).

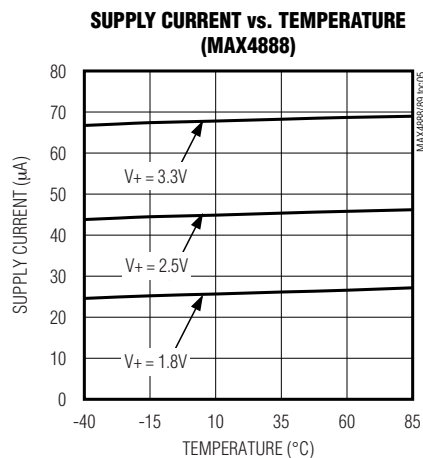
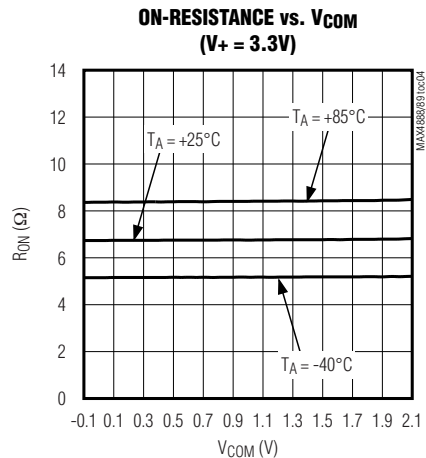
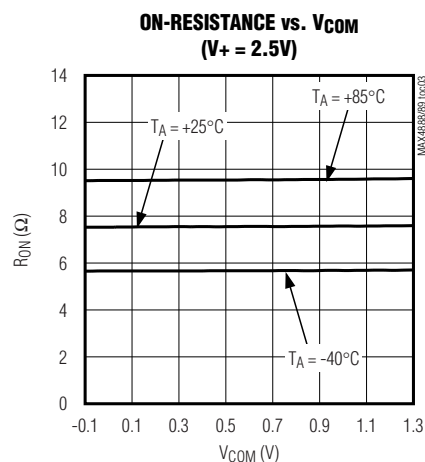
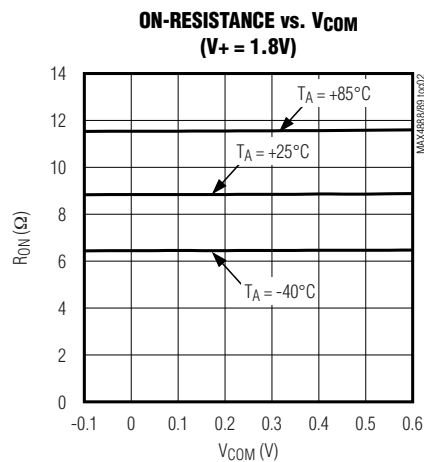
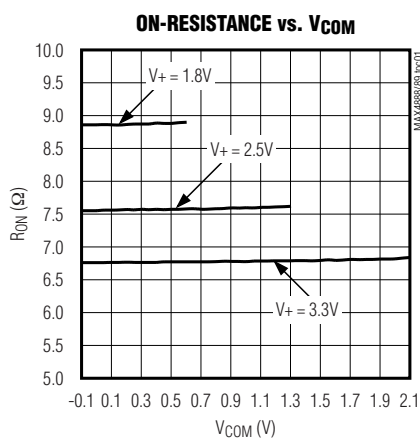
**Note 4:** Guaranteed by design. Not production tested.

**Note 5:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

# 2.5Gbps PCI Express Passive Switches

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

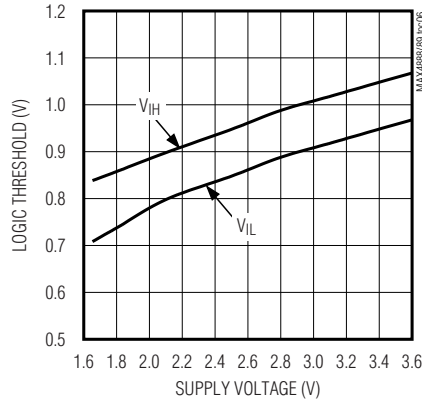


# 2.5Gbps PCI Express Passive Switches

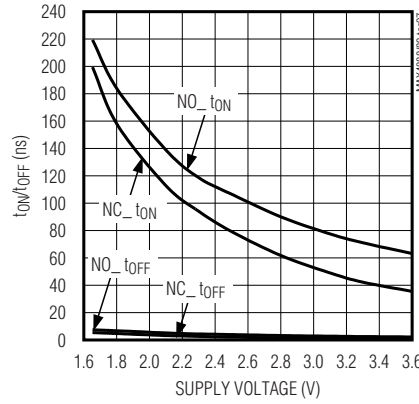
## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

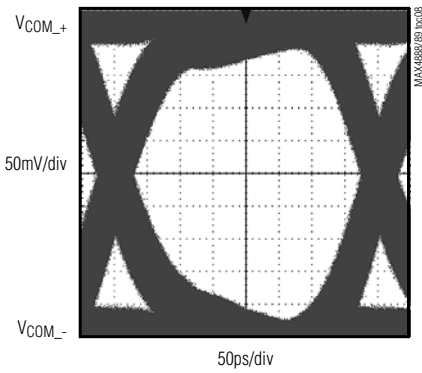
**LOGIC THRESHOLD vs. SUPPLY VOLTAGE**



**TURN-ON/-OFF TIME vs. SUPPLY VOLTAGE**

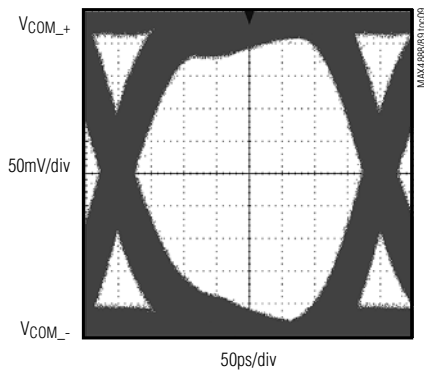


**EYE DIAGRAM**  
( $V_+ = 1.8\text{V}$ ,  $f = 1.25\text{GHz}$ ,  
600mVp-p PRBS SIGNAL,  $R_S = R_L = 50\Omega$ )<sup>†</sup>



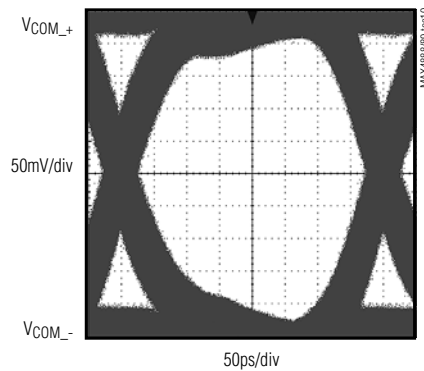
\*PRBS = PSEUDORANDOM BIT SEQUENCE  
<sup>†</sup>GEN I; 2.5Gps; UI = 400ps

**EYE DIAGRAM**  
( $V_+ = 2.5\text{V}$ ,  $f = 1.25\text{GHz}$ ,  
600mVp-p PRBS SIGNAL,  $R_S = R_L = 50\Omega$ )<sup>†</sup>



\*PRBS = PSEUDORANDOM BIT SEQUENCE  
<sup>†</sup>GEN I; 2.5Gps; UI = 400ps

**EYE DIAGRAM**  
( $V_+ = 3.3\text{V}$ ,  $f = 1.25\text{GHz}$ ,  
600mVp-p PRBS SIGNAL,  $R_S = R_L = 50\Omega$ )<sup>†</sup>



\*PRBS = PSEUDORANDOM BIT SEQUENCE  
<sup>†</sup>GEN I; 2.5Gps; UI = 400ps

MAX4888/MAX4889

## 2.5Gbps PCI Express Passive Switches

### Pin Description

PIN		NAME	FUNCTION
MAX4888	MAX4889		
1, 10, 12, 14, 20, 25, 27	1, 4, 10, 14, 17, 19, 21, 39, 41	GND	Ground
2	9	SEL	Digital Control Input
3, 9	—	N.C.	No Connection. Not internally connected.
4	2	COM1+	Analog Switch 1. Common Positive Terminal.
5	3	COM1-	Analog Switch 1. Common Negative Terminal.
6	6	COM2+	Analog Switch 2. Common Positive Terminal.
7	7	COM2-	Analog Switch 2. Common Negative Terminal.
8, 11, 13, 19, 26, 28	5, 8, 13, 18, 20, 30, 40, 42	V+	Positive-Supply Voltage Input. Connect V+ to a 1.65V to 3.6V supply voltage. Bypass V+ to GND with a 0.1µF capacitor placed as close to the device as possible. (See the <i>Board Layout</i> section).
15	31	NO2-	Analog Switch 2. Normally Open Negative Terminal.
16	32	NO2+	Analog Switch 2. Normally Open Positive Terminal.
17	33	NO1-	Analog Switch 1. Normally Open Negative Terminal.
18	34	NO1+	Analog Switch 1. Normally Open Positive Terminal.
21	35	NC2-	Analog Switch 2. Normally Closed Negative Terminal.
22	36	NC2+	Analog Switch 2. Normally Closed Positive Terminal.
23	37	NC1-	Analog Switch 1. Normally Closed Negative Terminal.
24	38	NC1+	Analog Switch 1. Normally Closed Positive Terminal.
—	11	COM3+	Analog Switch 3. Common Positive Terminal.
—	12	COM3-	Analog Switch 3. Common Negative Terminal.
—	15	COM4+	Analog Switch 4. Common Positive Terminal.
—	16	COM4-	Analog Switch 4. Common Negative Terminal.
—	22	NO4-	Analog Switch 4. Normally Open Negative Terminal.
—	23	NO4+	Analog Switch 4. Normally Open Positive Terminal.
—	24	NO3-	Analog Switch 3. Normally Open Negative Terminal.
—	25	NO3+	Analog Switch 3. Normally Open Positive Terminal.
—	26	NC4-	Analog Switch 4. Normally Closed Negative Terminal.
—	27	NC4+	Analog Switch 4. Normally Closed Positive Terminal.
—	28	NC3-	Analog Switch 3. Normally Closed Negative Terminal.
—	29	NC3+	Analog Switch 3. Normally Closed Positive Terminal.
EP	EP	EP	Exposed Paddle. Connect EP to GND.

# 2.5Gbps PCI Express Passive Switches

## Test Circuits/Timing Diagrams

MAX4888/MAX4889

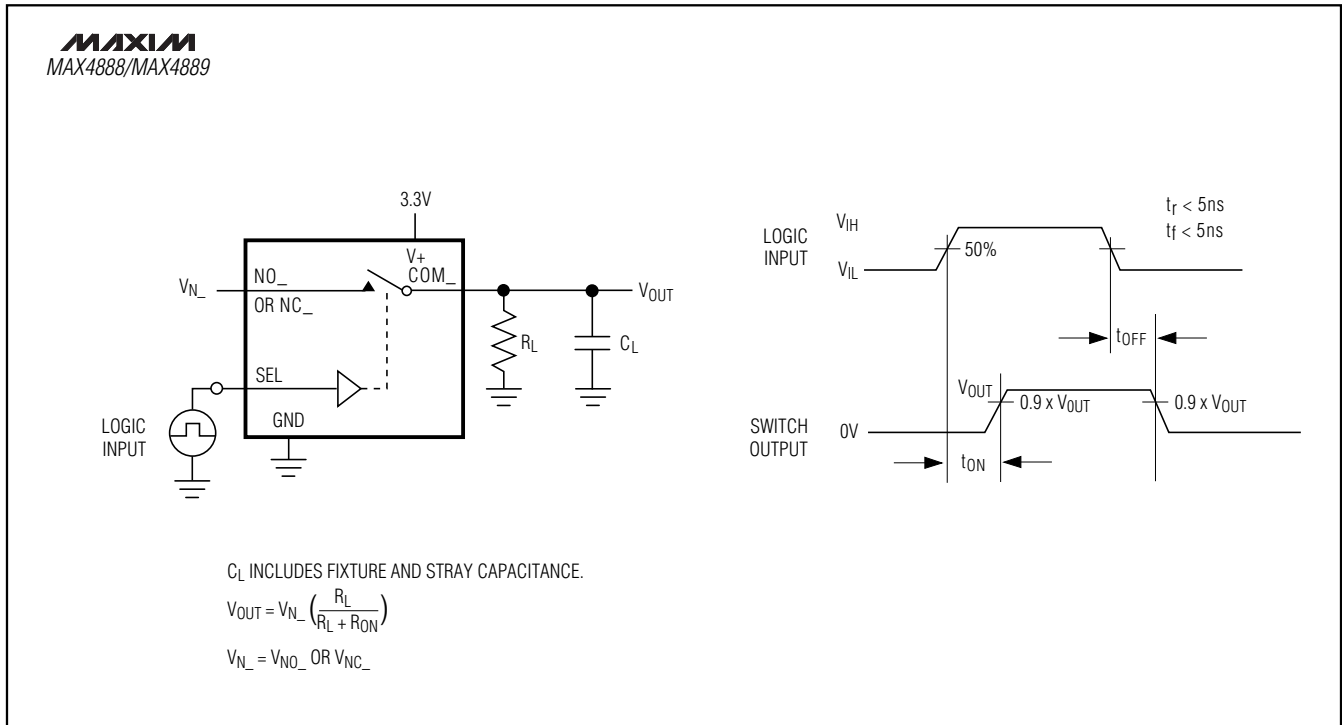


Figure 1. Switching Time

# 2.5Gbps PCI Express Passive Switches

## Test Circuits/Timing Diagrams (continued)

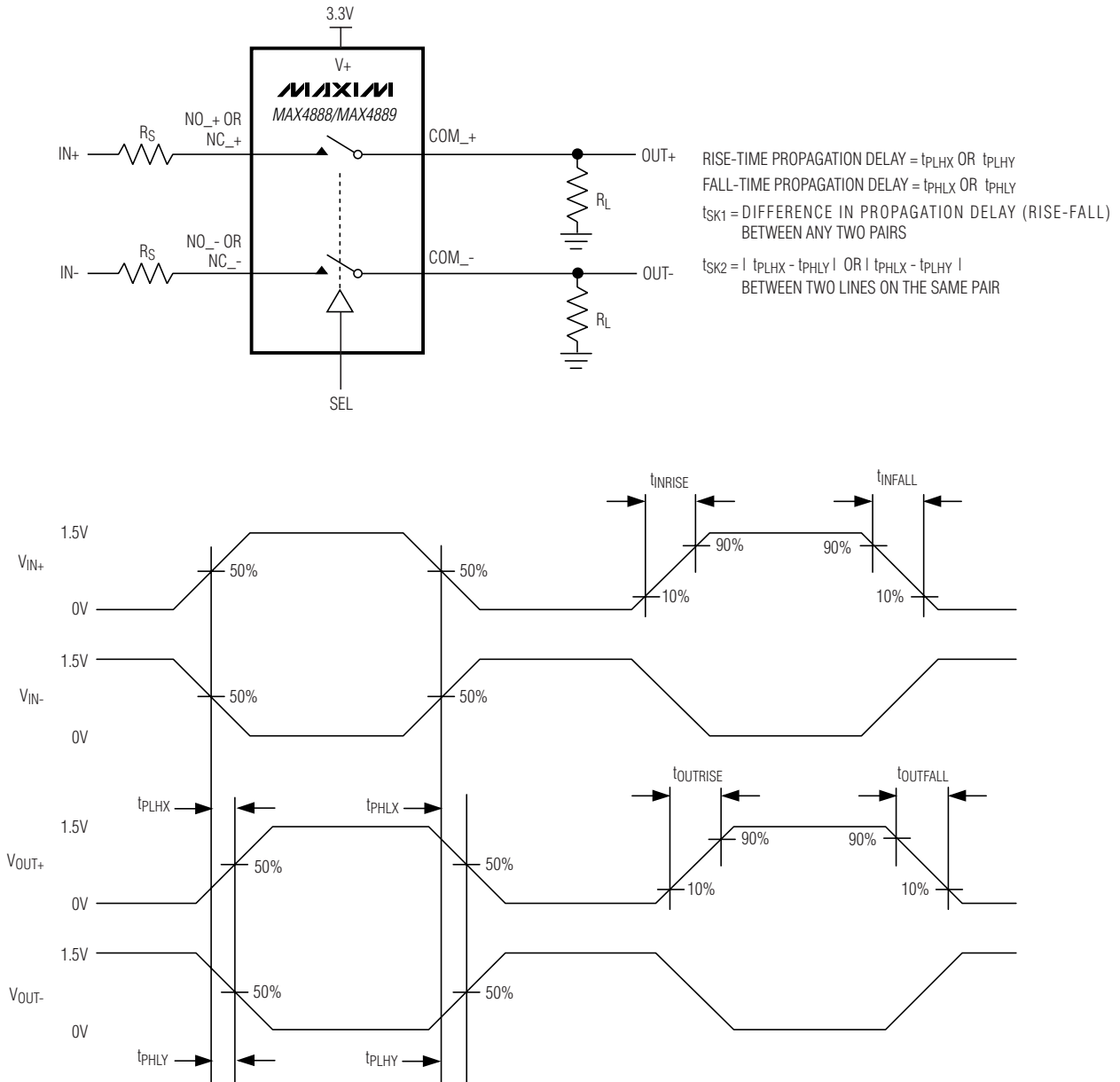


Figure 2. Propagation Delay and Output Skew



# 2.5Gbps PCI Express Passive Switches

## Test Circuits/Timing Diagrams (continued)

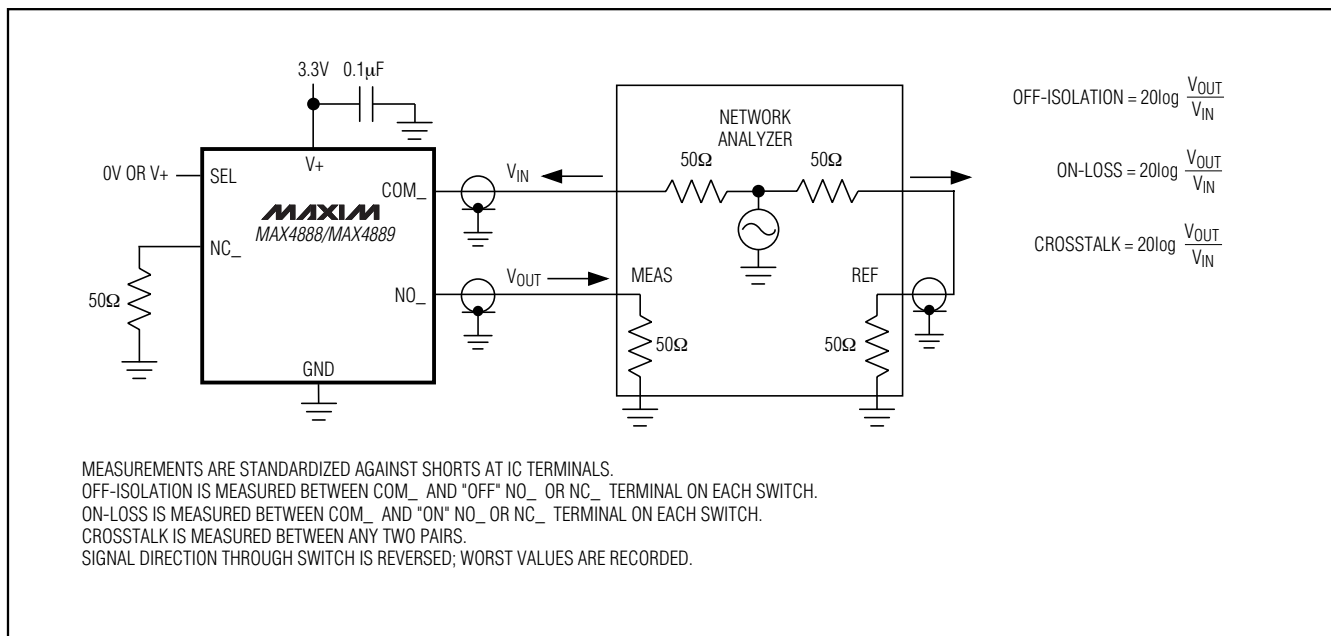


Figure 3. On-Loss, Off-Isolation, and Crosstalk

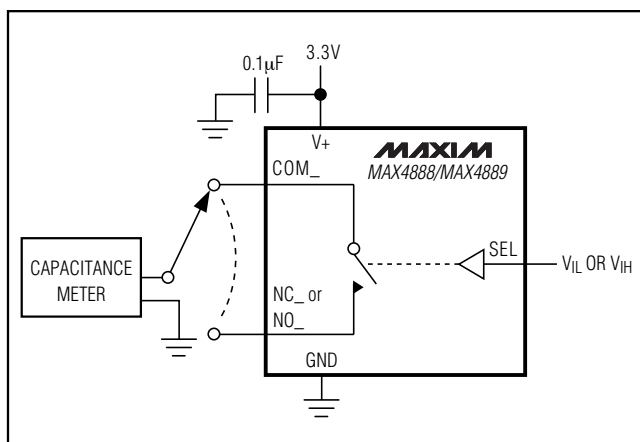


Figure 4. Channel Off-/On-Capacitance

## Detailed Description

The MAX4888/MAX4889 high-speed passive switches route PCIe data between two possible destinations. The MAX4888/MAX4889 are ideal for routing PCIe signals to change the system configuration. For example, in a graphics application, the MAX4888/MAX4889 create two

sets of eight lanes from a single 16-lane bus. The MAX4888/MAX4889 feature a single digital control input (SEL) to switch signal paths.

The MAX4888/MAX4889 are fully specified to operate from a single 3.0V to 3.6V power supply and also operate down to 1.65V.

### Digital Control Input (SEL)

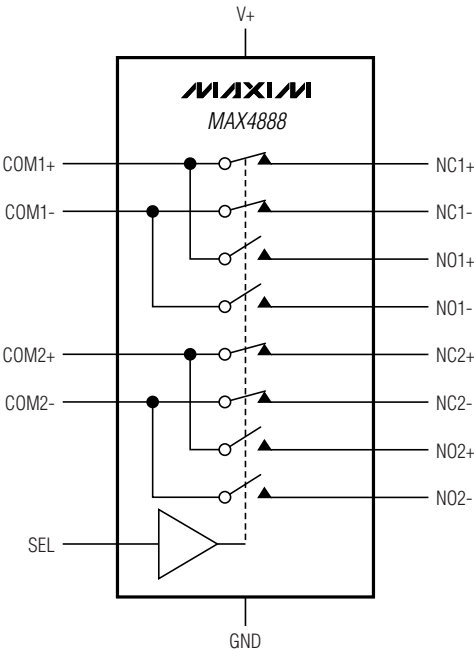
The MAX4888/MAX4889 provide a single digital control input (SEL) to select the signal path between the COM\_ and NO\_/NC\_ channels. The truth tables for the MAX4888/MAX4889 are depicted in the *Functional Diagrams/Truth Table* section. Drive SEL rail-to-rail to minimize power consumption.

### Analog Signal Levels

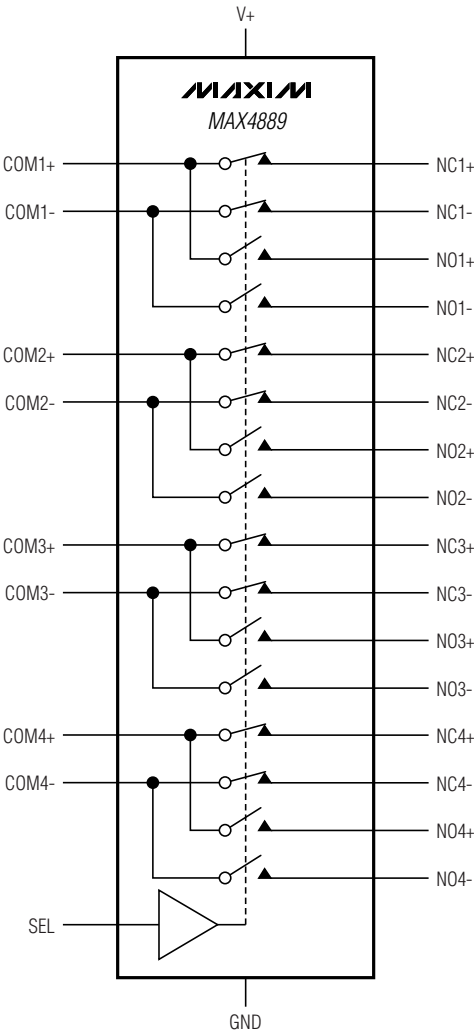
The MAX4888/MAX4889 accept standard PCIe signals to a maximum of  $V+ - 1.2V$ . Signals on the COM\_ channels are routed to either the NO\_+ or NC\_+ channels, and signals on the COM\_- channels are routed to either the NO\_- or NC\_- channels. The MAX4888/MAX4889 are bidirectional switches, allowing COM\_, NO\_, and NC\_ to be used as either inputs or outputs.

# 2.5Gbps PCI Express Passive Switches

Functional Diagrams/Truth Table



SEL	COM_ TO NC_	COM_ TO NO_
0	ON	OFF
1	OFF	ON



# 2.5Gbps PCI Express Passive Switches

## Applications Information

### PCIe Switching

The MAX4888/MAX4889 primary applications are aimed at reallocating PCIe lanes (see Figure 5). For example, in graphics applications, several manufacturers have found that it is possible to improve performance by a factor of nearly two by splitting a single 16-lane PCIe bus into two 8-lane buses. Two of the more prominent examples are SLI™ (Scaled Link Interface) and CrossFire™. The MAX4889 permits a computer motherboard to operate properly with a single 16-lane graphics card, and can later be updated to dual cards. The same motherboard can be used with dual cards where the user sets a jumper or a bit through software to switch between single- or dual-card operation.

### Board Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled impedance PCB traces as short as possible or follow impedance layouts per the PCIe specification. Ensure that power-supply bypass capacitors are placed as close to the device as possible. Multiple bypass capacitors are recommended. Connect all grounds and the exposed pad to large ground planes.

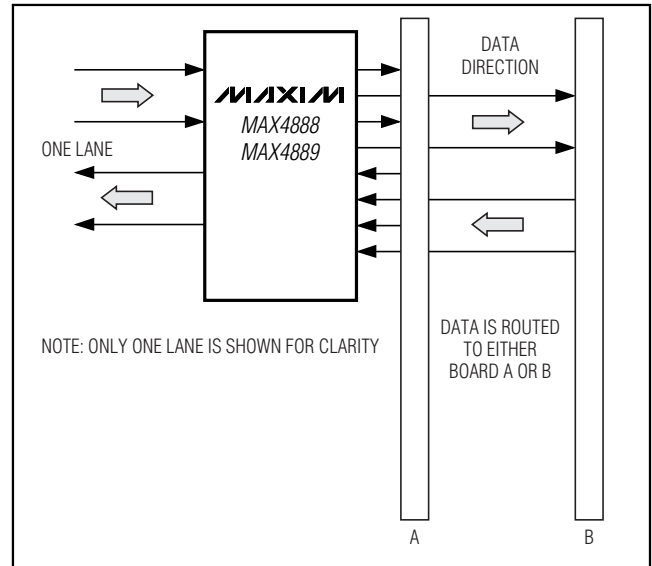


Figure 5. The MAX4888/MAX4889 Used as a Single-Lane Switch

## Chip Information

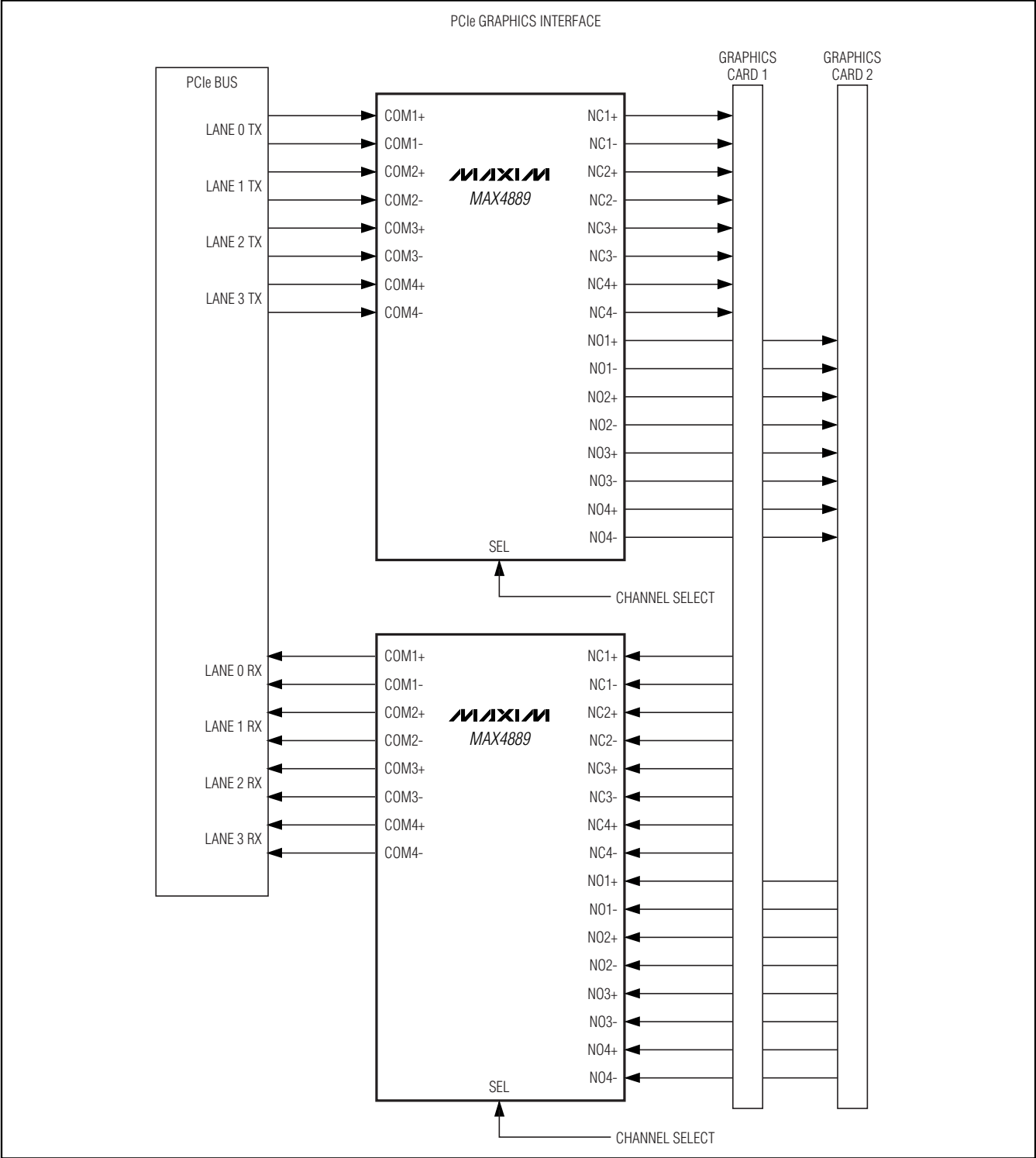
PROCESS: CMOS

CrossFire™ is a trademark of ATI Technologies, Inc.

SLI™ is a trademark of NVIDIA Corporation.

# 2.5Gbps PCI Express Passive Switches

## Typical Application Circuit

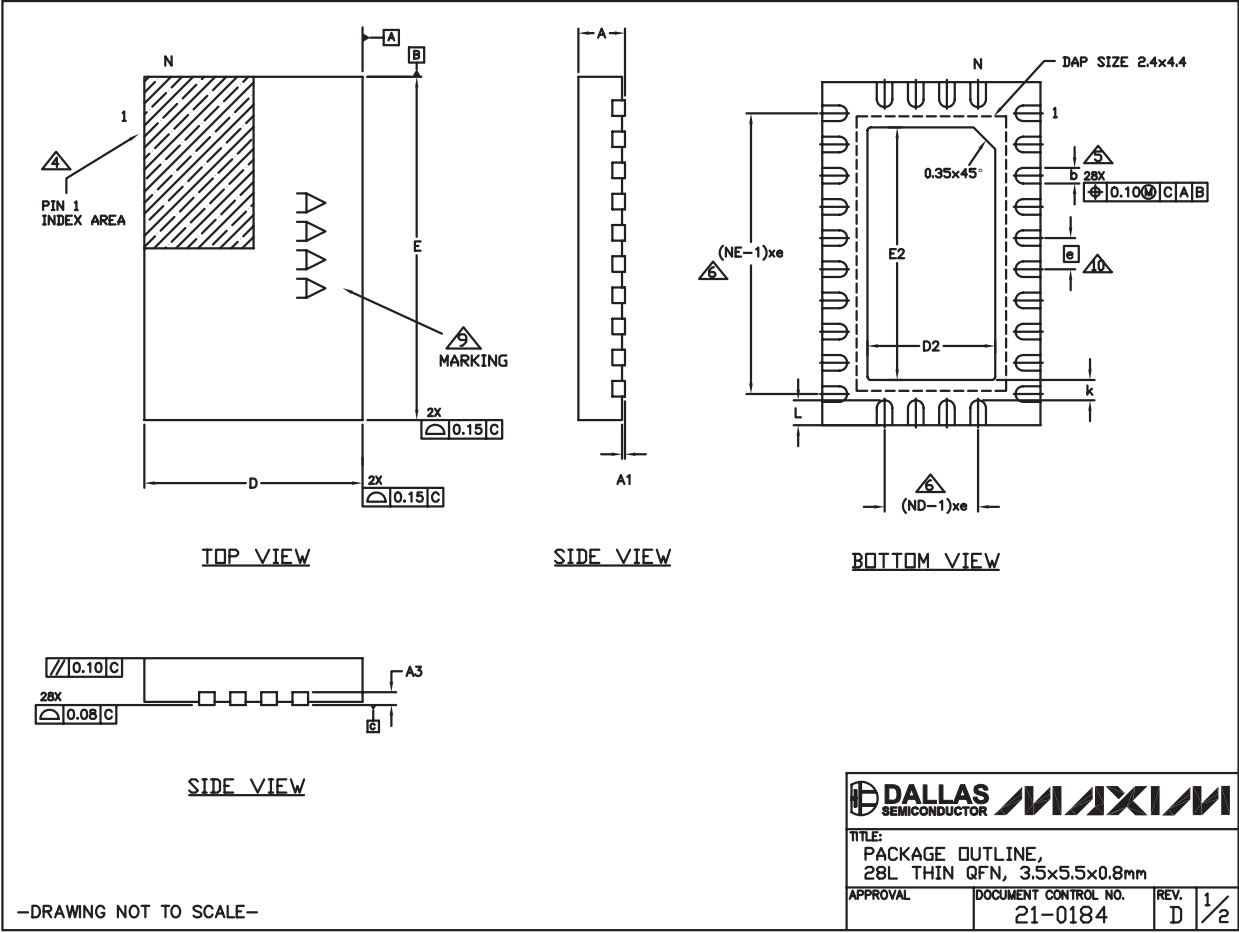


# 2.5Gbps PCI Express Passive Switches

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX4888/MAX4889



## 2.5Gbps PCI Express Passive Switches

### Package Information (continued)

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COMMON DIMENSIONS				
REF.	MIN.	NOM.	MAX.	NOTE
A	0.70	0.75	0.80	
A1	0	—	0.05	
A3	0.20 REF.			
b	0.20	0.25	0.30	
D	3.40	3.50	3.60	
E	5.40	5.50	5.60	
e	0.50 BSC.			
k	0.25	—	—	
L	0.30	0.40	0.50	ALL PINS
N	28			
ND	4			
NE	10			

PKG. CODE	EXPOSED PAD VARIATIONS					
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T283555-1	1.95	2.05	2.15	3.95	4.05	4.15

#### NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
10. LEAD CENTERLINES DEFINED BY DIMENSION e±0.05.

—DRAWING NOT TO SCALE—

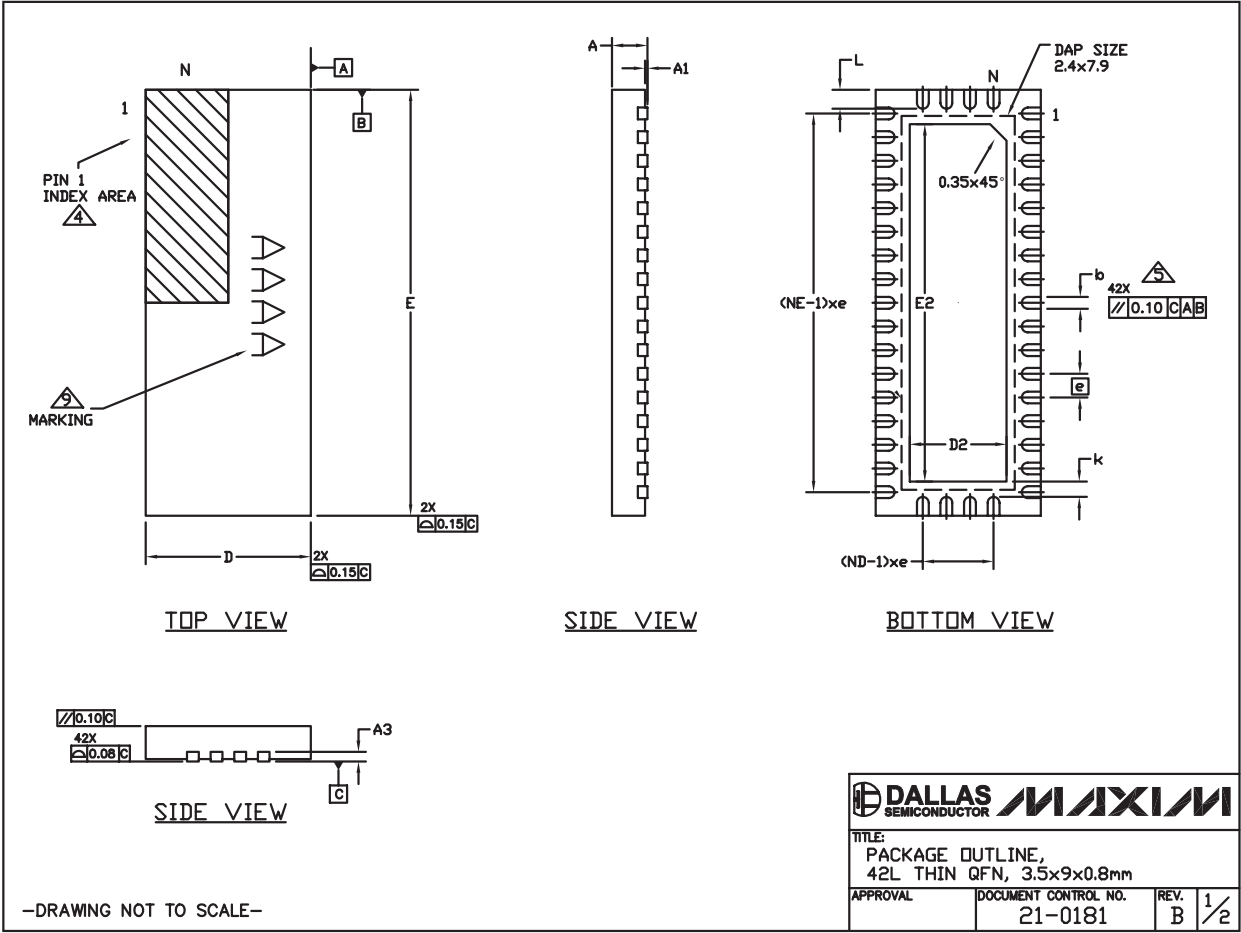
	
<b>TITLE:</b> PACKAGE OUTLINE, 28L THIN QFN, 3.5x5.5x0.8mm	
<b>APPROVAL</b>	<b>DOCUMENT CONTROL NO.</b> 21-0184
<b>REV.</b> D	<b>2/2</b>

# 2.5Gbps PCI Express Passive Switches

## Package Information (continued)

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MAX4888/MAX4889



## 2.5Gbps PCI Express Passive Switches

### Package Information (continued)

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COMMON DIMENSIONS				
REF.	MIN.	NOM.	MAX.	NOTE
A	0.70	0.75	0.80	
A1	0	—	0.05	
A3	0.20 REF.			
b	0.20	0.25	0.30	
D	3.40	3.50	3.60	
E	8.90	9.00	9.10	
e	0.50 BSC.			
k	0.25	—	—	
L	0.35	0.40	0.45	ALL PINS
N	42			
ND	4			
NE	17			

PKG. CODE	EXPOSED PAD VARIATIONS					
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T423590-1	1.95	2.05	2.15	7.45	7.55	7.65
T423590M-1	1.95	2.05	2.15	7.45	7.55	7.65

#### NOTES:

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- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
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- WARPAGE SHALL NOT EXCEED 0.10mm.
- MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
- LEAD CENTERLINES TO BE AT DEFINED BY DIMENSION e  $\pm 0.05$ .

—DRAWING NOT TO SCALE—

			
<b>TITLE:</b> PACKAGE OUTLINE, 42L THIN QFN, 3.5x9x0.8mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
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