64M-bit (×8 /×16) MirrorFlash™ Memory MBM29LP640UHM / MBM29LP640ULM

This is a MirrorFlash™ memory with a page mode which operates with a single 3V power supply. By adopting a new multi-bit technology, MirrorFlash™ architecture, it achieves a high-speed access performance with an initial access time of 90ns and page access time of 25ns.

Product Description

A 64M-bit MirrorFlash memory has been developed using MirrorFlash architecture for application in mobile phones, communication devices, set-top boxes and car navigation.

Dramatic improvements of the speed and density of mobile phones, the speed of laser printers, the map-searching ability in car navigation system, and the range of communication functions and applications in digital TVs and other set-top boxes have necessitated increases in the speed, functionality, and density of associated devices.

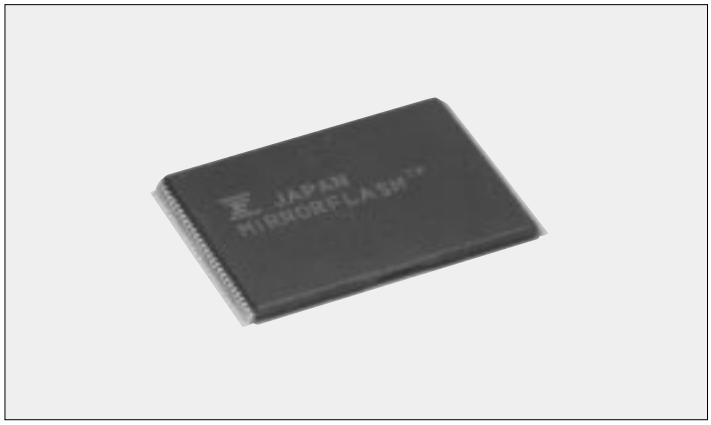
This product addresses the market demand for increased density and miniaturization by utilizing MirrorFlash architecture. The MirrorFlash architecture is a new multi-bit technology achieving 2-bit/cell structure, and allows larger density for existing devices compared to the conventional floating gate (FG) technology. FUJITSU has developed a 64M-bit product as the first of many products using this architecture. In addition, this MirrorFlash memory has been developed with a focus on fast access speed, resulting in the fastest-ever read-out speeds of 90ns for initial access and 25ns for page mode access. The programming performance is also largely improved through implementing of write-buffer programming that allows simultaneous writing of 32 bytes or 16 words. Other functions include a Hi-ROM function that prevents large-scale illegal copying of devices, write hardware protection for the boot block sector storing system programs and an acceleration function that enables high-speed programming at system.

Product Features

MirrorFlash Architecture

The cell structure for the MirrorFlash architecture is shown in **Fig. 1**. Unlike the conventional floating gate technology, this architecture features a nitride film inserted between the

Photo 1 External View



control gate and oxide film. The nitride film acts as an insulation membrane and is injected with electrons to maintain its electrical charge. Two electron spots (on the right and left sides) can be made in 1 cell, and a 2-bit/cell can be achieved by localizing the electrons at each.

High-speed Read Operation

Fig. 2 shows the page mode read timing. The page mode reads out an optional page (8 bytes or 4 words) by first selecting a high-order address (A21 to A2). Then, by selecting a low-order address (A1 to A-1 or A1 to A0), the data in the page can be read out at a high speed in units of bytes or words. There are products available with access times of 90ns and 110ns for this product type, and in-page access for each initial time 90ns / 110ns is 25ns / 30ns, respectively.

Write-Buffer Programming

Fig. 3 shows the conceptual diagram of the write-buffer programming. Conventionally, programming data was programmed in units of bytes or words. However, the write-buffer programming writes into the flash memory after loading 32 bytes or 16 words of data into the write buffer.

Single 3V Power Supply Operation

Reading/writing/erasing data is possible with only a single 3V power supply. Since the system does not require a 12V power supply, it can be configured without a voltage conversion element or other additional parts.

Compatibility with Conventional Products

Writing/erasing is possible using the same basic command sequence as for the single 3V power supply flash memory, which has already been commercialized.

Figure 1 Cell Structure of MirrorFlash Architecture and Stored Data

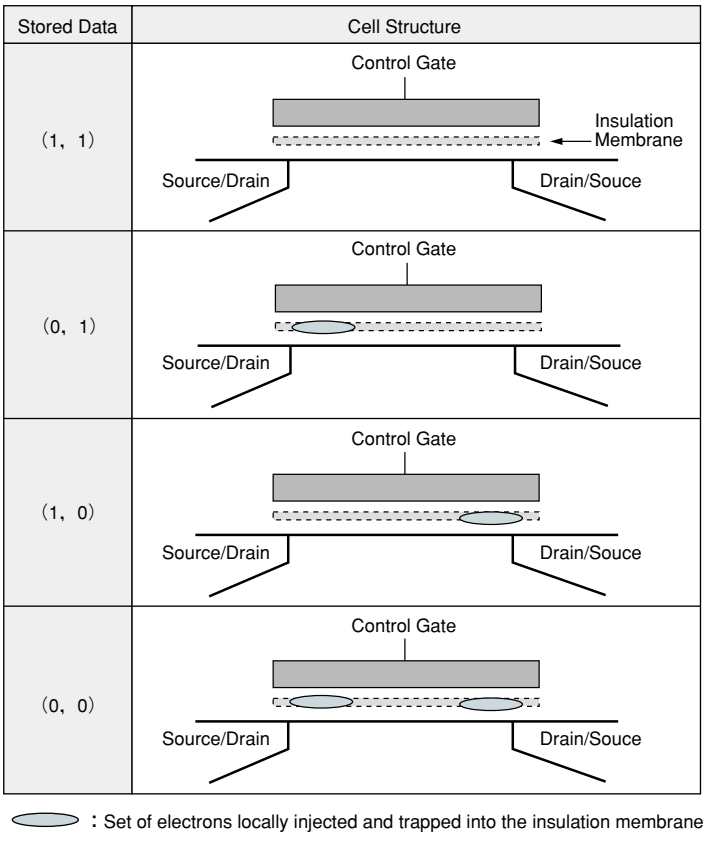


Figure 2 Page Mode Read-out Timing (during word mode)

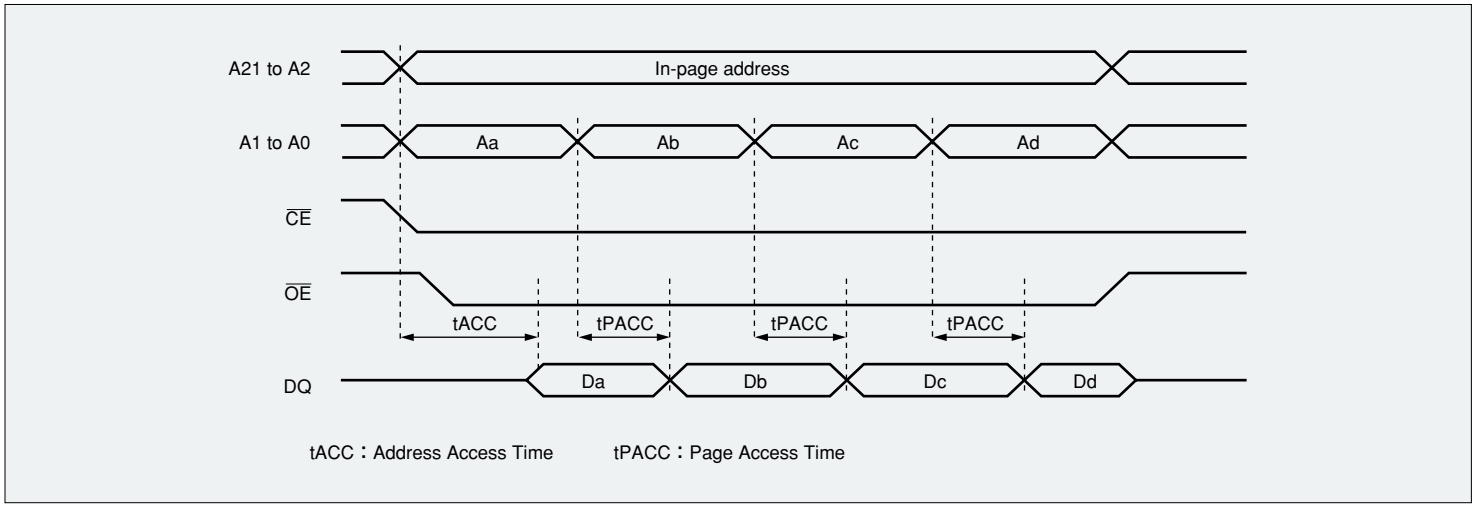


Figure 3 Conceptual Diagram of Write-Buffer Programming

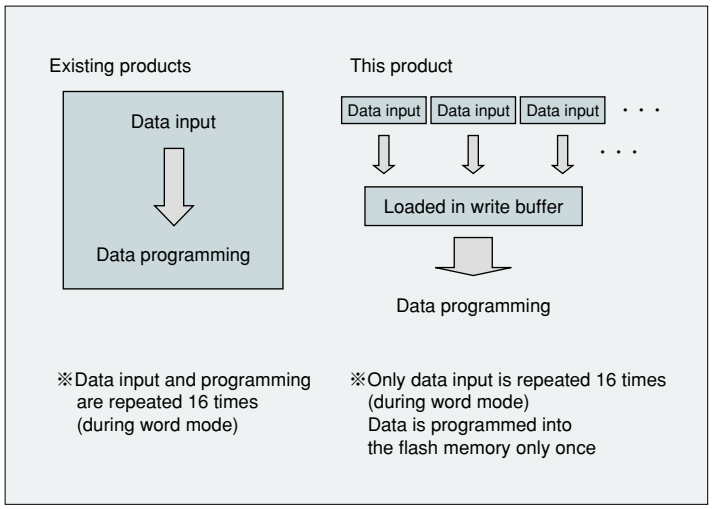
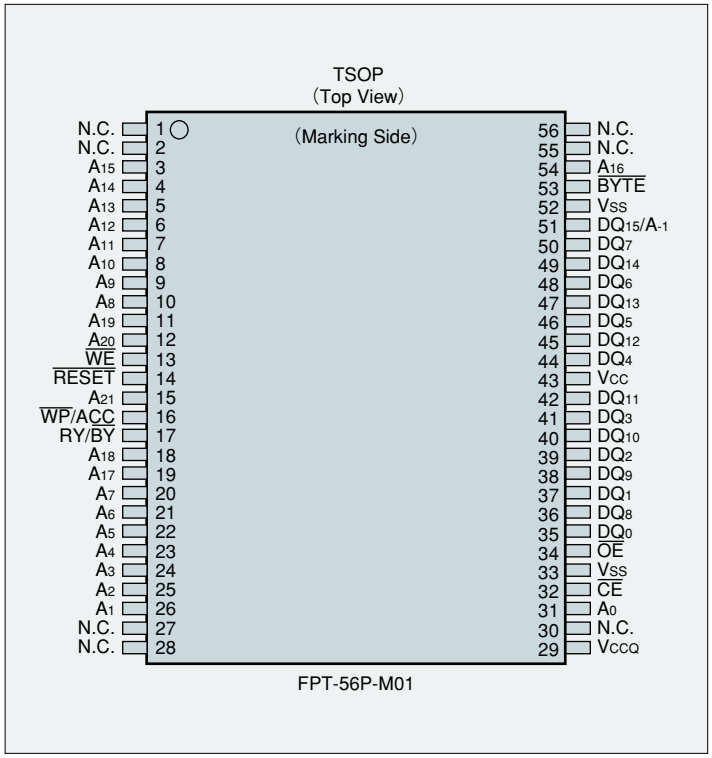


Figure 4 Pin Assignments



×8-bit or ×16-bit Configuration

When the BYTE pin is set to "H," the device operates in word mode, and data is read/written with DQ15 to DQ0. When the BYTE pin is set to "L," the device operates in byte mode. In this case, DQ15/A-1 is the lowest address bit, and the data is read/written with DQ7 to DQ0, while DQ14 to DQ8 are ignored.

Fig. 4 shows the pin assignments.

Hi-ROM Function

In addition to the normal memory region, a special 128 words region is offered as an area where data can be programmed only once. Programming special data (for example, unique ID number) provides a highly advanced security function by the combination with an application.

Write-Protection Function

A simpler write-protection function is realized through hardware method. This function protects the sector at highest or lowest order by setting the WP pin at "L", whether or not normal sector protection is performed.

Acceleration Function

This function is effective when a large amount of flash memory is programmed for incorporation at the time of system shipment. A high voltage (VACC) applied to the ACC pin activates the acceleration mode, enabling programming at higher-than-usual speed. This function is expected to reduce the programming time to 60% of that in conventional products.

Table 1 shows the product configuration.

Advantages and Effectiveness

The use of a memory structure one class higher can be realized using the existing technologies. For example, using a combination of various memories within a 9×12×1.4mm (max.) MCP (Multi Chip Package), numerous memory-device solutions can be realized for applications with limited mounting space, such as mobile phones. Although the maximum density for a single flash memory unit mountable on a 9×12×1.4mm MCP was 64M-bit with conventional technologies, MirrorFlash enables mounting of 128M-bit flash memory, greatly increasing the number of selections offered.

Applications

Sample applications for a 64M-bit MirrorFlash memory with the above characteristics include the following.

- Systems requiring high performance, large density, and small-size flash memory
- Systems performing XIP between the RAM and processor after the program is copied to RAM from the flash memory

at start-up
- Systems realizing code storage memory and data storage memory on the same flash

Future Development

This article has introduced FUJITSU's new product, MBM29LP640UHM / MBM29LP640ULM, as a solution for increased density, speed, and miniaturization of mobile phones, laser printers, set-top boxes, and car navigation devices. FUJITSU will continue to replenish the MirrorFlash family with a large variety of new products achieving multi-functionality, high functionality and increased density to meet customer needs. ★

NOTES

* MirrorFlash is a trademark of FUJITSU LIMITED.

Table 1 Product Line Up

Part Number			MBM29LP640UHM		MBM29LP640ULM	
Speed Version			90	11	90	11
Access Time		Initial	90	110	90	110
		Page	25	30	25	30
Power Supply Voltage			3.0V to 3.6V	2.7V to 3.6V	3.0V to 3.6V	2.7V to 3.6V
Power Consumption (Max.)	Read	Word	180mW		180mW	
	Erasing/Programming in progress		216mW		216mW	
	CMOS Standby		18 μW		18 μW	
Erase Time (Typical)			0.4 s /sector		0.4 s /sector	
Programming Time (Typical)*		16 Word	374 μs		374 μs	
Hardware rotection by $\overline{WP}$ Pin			Uppermost sector (SA127)		Lowermost sector (SA0)	
Package			TSOP-56		TSOP-56	

* During write-buffer operating : effective writing time is 23.5μs /word (Typical)