# 5810-F

## BiMOS II 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

### UCN5810AF



| | | | |
|---|---|---|---|
| OUT$_8$ | 1 | 18 | OUT$_9$ |
| OUT$_7$ | 2 | 17 | OUT$_{10}$ |
| OUT$_6$ | 3 | 16 | SERIAL DATA OUT |
| CLOCK | 4 CLK | 15 V$_{BB}$ | LOAD SUPPLY |
| GROUND | 5 | 14 | SERIAL DATA IN |
| LOGIC SUPPLY | 6 V$_{DD}$ | 13 BLNK | BLANKING |
| STROBE | 7 ST | 12 | OUT$_1$ |
| OUT$_5$ | 8 | 11 | OUT$_2$ |
| OUT$_4$ | 9 | 10 | OUT$_3$ |

LATCHES / REGISTER / REGISTER / LATCHES
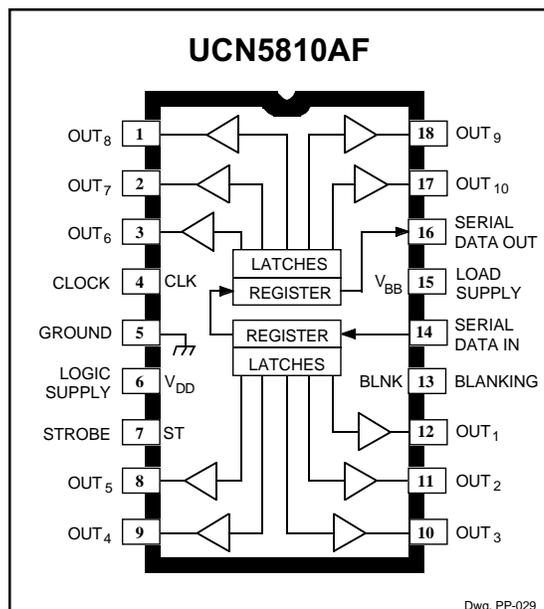
Dwg. PP-029

### ABSOLUTE MAXIMUM RATINGS
#### at T$_A$ = 25°C

Logic Supply Voltage, V$_{DD}$ ..................... **15 V**
Driver Supply Voltage, V$_{BB}$ .................... **60 V**
Continuous Output Current Range,
   I$_{OUT}$ ........................... **-40 mA to +15 mA**
Input Voltage Range,
   V$_{IN}$ ........................ **-0.3 V to V$_{DD}$ + 0.3 V**
Package Power Dissipation, P$_D$
   (UCN5810AF) ........................... **2.08 W***
   (UCN5810EPF) ........................ **1.60 W***
   (UCN5810LWF) ...................... **1.33 W***
Operating Temperature Range,
   T$_A$ ................................ **-20°C to +85°C**
Storage Temperature Range,
   T$_S$ .............................. **-55°C to +150°C**

*Derate linearly to 0 W at +150°C.

*Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.*

Note that the UCN5810AF (dual in-line package) and UCN5810LWF (small-outline IC package) are electrically identical and share a common terminal number assignment.

The UCN5810AF, UCN5810EPF, and UCN5810LWF combine a 10-bit CMOS shift register and accompanying data latches, control circuitry, bipolar sourcing outputs with DMOS active pull-downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The UCN5810AF/EPF/LWF feature reduced supply requirements (active DMOS pull-downs) and lower saturation voltages when compared with the original UCN5810A.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V supply, they will operate to at least 3.3 MHz. At 12 V, higher speeds are possible. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCN5811A (12 bits), UCN5812AF/EPF (20 bits), and UCN5818AF/EPF (32 bits).

The UCN5810AF/EPF/LWF output source drivers are NPN Darlingtons capable of sourcing up to 40 mA. The DMOS active pull-downs are capable of sinking up to 15 mA. For inter-digit blanking, all of the output drivers can be disabled and the DMOS sink drivers turned on by the BLANKING input high.

The UCN5810AF is furnished in an 18-pin dual in-line plastic package. The UCN5810EPF is furnished in a 20-lead plastic chip carrier. The UCN5810LWF is furnished in a wide-body, small-outline plastic package (SOIC) with gull-wing leads. Copper lead frames, reduced supply current requirements, and lower output saturation voltages allow all devices to source 25 mA from all outputs continuously, over the entire operating temperature range. All devices are also available for operation between -40°C and +85°C. To order, change the prefix from 'UCN' to 'UCQ'.
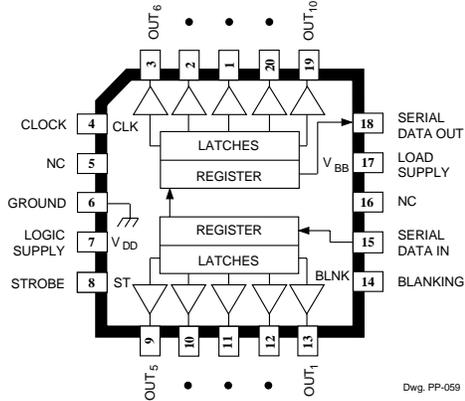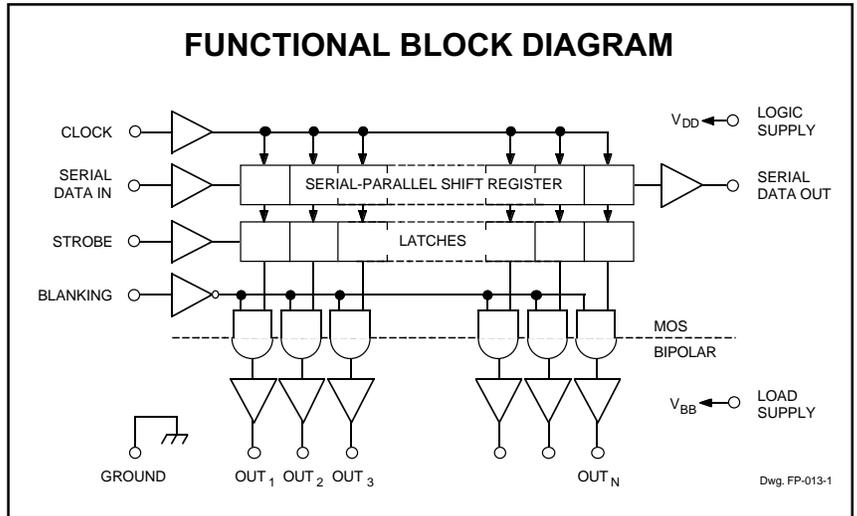
### FEATURES

- High-Speed Source Drivers
- 60 V Minimum Output Breakdown
- Improved Replacements for TL4810B
- Low Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- To 3.3 MHz Data Input Rate
- Active DMOS Pull-Downs

Always order by complete part number, e.g., **UCN5810AF** .

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# 5810-F
## *10-BIT SERIAL-INPUT,*
## *LATCHED SOURCE DRIVERS*
## *WITH ACTIVE-DMOS PULL-DOWNS*

### UCN5810EPF



Dwg. PP-059

### UCN5810LWF



Dwg. PP-029-1

## FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-013-1
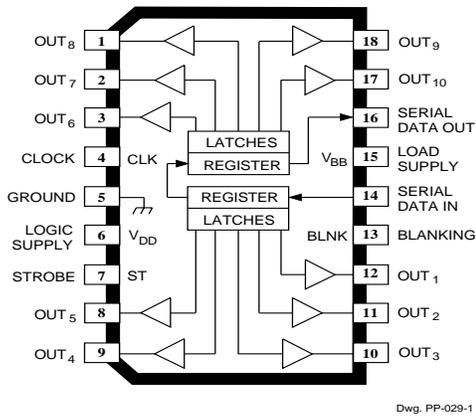
## TYPICAL INPUT CIRCUIT



Dwg. EP-010-4A
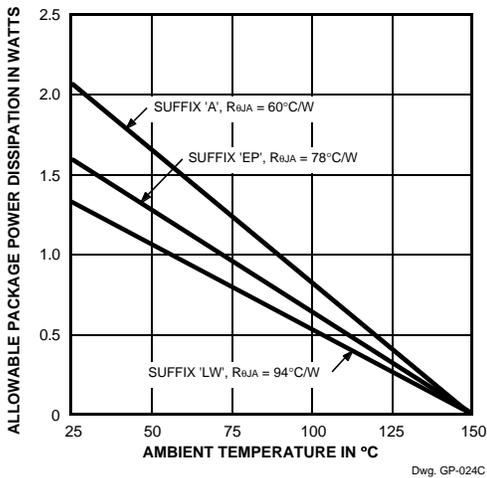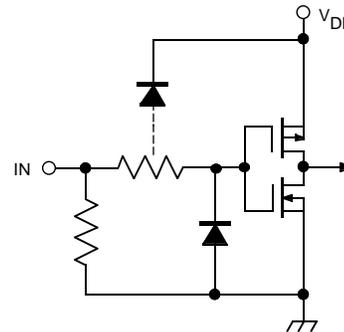
## TYPICAL OUTPUT DRIVER
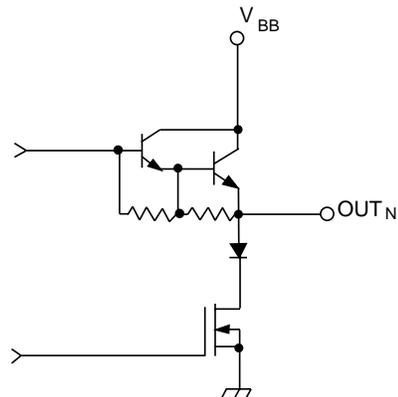


Dwg. No. A-14,219



SUFFIX 'A', $R_{\theta JA} = 60°C/W$

SUFFIX 'EP', $R_{\theta JA} = 78°C/W$

SUFFIX 'LW', $R_{\theta JA} = 94°C/W$

Dwg. GP-024C

## ELECTRICAL CHARACTERISTICS at $T_A$ = +25°C, $V_{BB}$ = 60 V unless otherwise noted.

| Characteristic | Symbol | Test Conditions | Limits @ $V_{DD}$ = 5 V | | | Limits @ $V_{DD}$ = 12 V | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Output Leakage Current | $I_{CEX}$ | $V_{OUT}$ = 0 V, $T_A$ = +70°C | — | -5.0 | -15 | — | -5.0 | -15 | μA |
| Output Voltage | $V_{OUT(1)}$ | $I_{OUT}$ = -25 mA | 58 | 58.5 | — | 58 | 58.5 | — | V |
| | $V_{OUT(0)}$ | $I_{OUT}$ = 1 mA | — | 1.0 | 1.5 | — | — | — | V |
| | | $I_{OUT}$ = 2 mA | — | — | — | — | 1.0 | 1.5 | V |
| Output Pull-Down Current | $I_{OUT(0)}$ | $V_{OUT}$ = 5 V to $V_{BB}$ | 2.0 | 3.5 | — | — | — | — | mA |
| | | $V_{OUT}$ = 20 V to $V_{BB}$ | — | — | — | 8.0 | 13 | — | mA |
| Input Voltage | $V_{IN(1)}$ | | 3.5 | — | 5.3 | 10.5 | — | 12.3 | V |
| | $V_{IN(0)}$ | | -0.3 | — | +0.8 | -0.3 | — | +0.8 | V |
| Input Current | $I_{IN(1)}$ | $V_{IN}$ = $V_{DD}$ | — | — | 100 | — | — | 240 | μA |
| | $I_{IN(0)}$ | $V_{IN}$ = 0.8 V | — | -0.05 | -0.5 | — | -0.1 | -1.0 | μA |
| Serial Data Output Voltage | $V_{OUT(1)}$ | $I_{OUT}$ = -200 μA | 4.5 | 4.7 | — | 11.7 | 11.8 | — | V |
| | $V_{OUT(0)}$ | $I_{OUT}$ = 200 μA | — | 200 | 250 | — | 100 | 200 | mV |
| Maximum Clock Frequency | $f_{clk}$ | | 3.3* | — | — | — | — | — | MHz |
| Supply Current | $I_{DD(1)}$ | All Outputs High | — | 100 | 300 | — | 200 | 500 | μA |
| | $I_{DD(0)}$ | All Outputs Low | — | 100 | 300 | — | 200 | 500 | μA |
| | $I_{BB(1)}$ | Outputs High, No Load | — | 0.7 | 2.0 | — | 0.7 | 2.0 | mA |
| | $I_{BB(0)}$ | Outputs Low | — | 10 | 100 | — | 10 | 100 | μA |
| Blanking to Output Delay | $t_{PHL}$ | $C_L$ = 30 pF, 50% to 50% | — | 2000 | — | — | 1000 | — | ns |
| | $t_{PLH}$ | $C_L$ = 30 pF, 50% to 50% | — | 1000 | — | — | 850 | — | ns |
| Output Fall Time | $t_f$ | $C_L$ = 30 pF, 90% to 10% | — | 1450 | — | — | 650 | — | ns |
| Output Rise Time | $t_r$ | $C_L$ = 30 pF, 10% to 90% | — | 650 | — | — | 700 | — | ns |

Negative current is defined as coming out of (sourcing) the specified device pin.

* Operation at a clock frequency greater than the specified minimum value is possible but not warranteed.

# 5810-F
## 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS
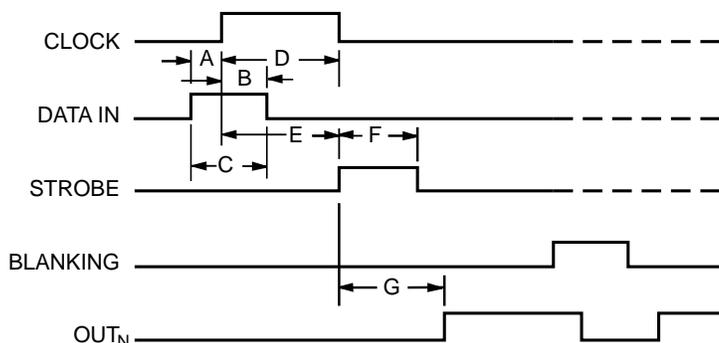


Dwg. No. A-12,649A

### TIMING REQUIREMENTS
($T_A$ = +25°C, $V_{DD}$ = 5 V, Logic Levels are $V_{DD}$ and Ground)

**A.** Minimum Data Active Time Before Clock Pulse
   (Data Set-Up Time) ........................................................... **75 ns**

**B.** Minimum Data Active Time After Clock Pulse
   (Data Hold Time) ............................................................... **75 ns**

**C.** Minimum Data Pulse Width ................................................ **150 ns**

**D.** Minimum Clock Pulse Width ............................................... **150 ns**

**E.** Minimum Time Between Clock Activation and Strobe ........................ **300 ns**

**F.** Minimum Strobe Pulse Width ............................................. **100 ns**

**G.** Typical Time Between Strobe Activation and
   Output Transistion .......................................................... **500 ns**

Timing is representative of a 3.3 MHz clock. Higher speeds may be attainable with increased supply voltage; operation at high temperatures will reduce the specified maximum clock frequency.

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

## TRUTH TABLE

| Serial Data Input | Clock Input | Shift Register Contents $I_1$ | $I_2$ | $I_3$ | ... | $I_{N-1}$ | $I_N$ | Serial Data Output | Strobe Input | Latch Contents $I_1$ | $I_2$ | $I_3$ | ... | $I_{N-1}$ | $I_N$ | Blanking | Output Contents $I_1$ | $I_2$ | $I_3$ | ... | $I_{N-1}$ | $I_N$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | ⌐ | H | $R_1$ | $R_2$ | ... | $R_{N-2}$ | $R_{N-1}$ | $R_{N-1}$ | | | | | | | | | | | | | | |
| L | ⌐ | L | $R_1$ | $R_2$ | ... | $R_{N-2}$ | $R_{N-1}$ | $R_{N-1}$ | | | | | | | | | | | | | | |
| X | ⌐ | $R_1$ | $R_2$ | $R_3$ | ... | $R_{N-1}$ | $R_N$ | $R_N$ | | | | | | | | | | | | | | |
| | | X | X | X | ... | X | X | X | L | $R_1$ | $R_2$ | $R_3$ | ... | $R_{N-1}$ | $R_N$ | | | | | | | |
| | | $P_1$ | $P_2$ | $P_3$ | ... | $P_{N-1}$ | $P_N$ | $P_N$ | H | $P_1$ | $P_2$ | $P_3$ | ... | $P_{N-1}$ | $P_N$ | L | $P_1$ | $P_2$ | $P_3$ | ... | $P_{N-1}$ | $P_N$ |
| | | | | | | | | | | X | X | X | ... | X | X | H | L | L | L | ... | L | L |

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State
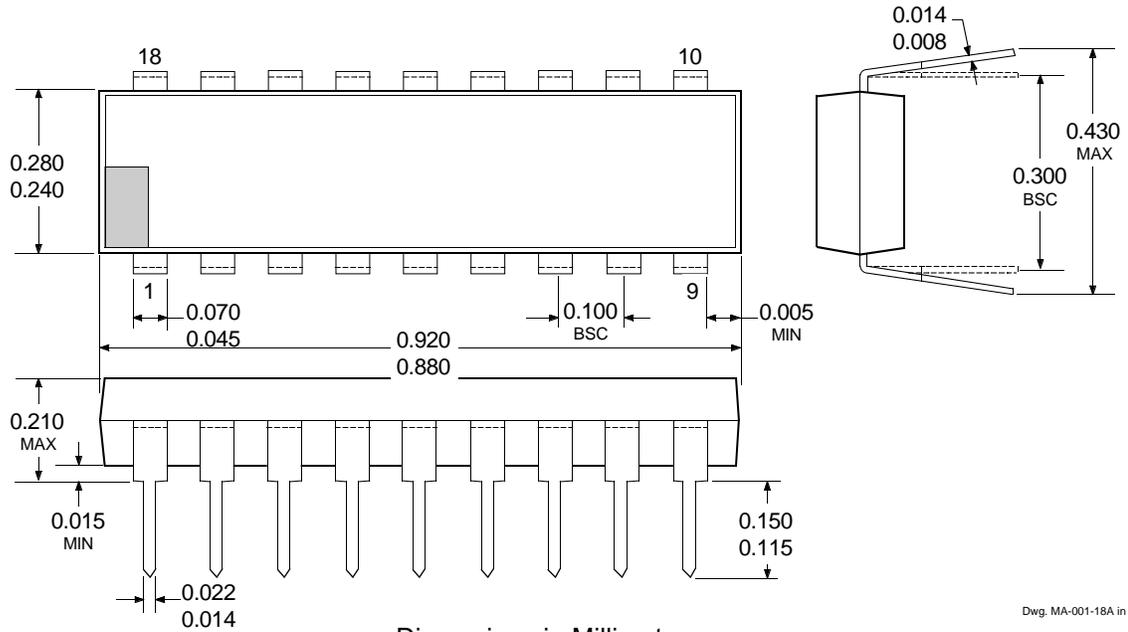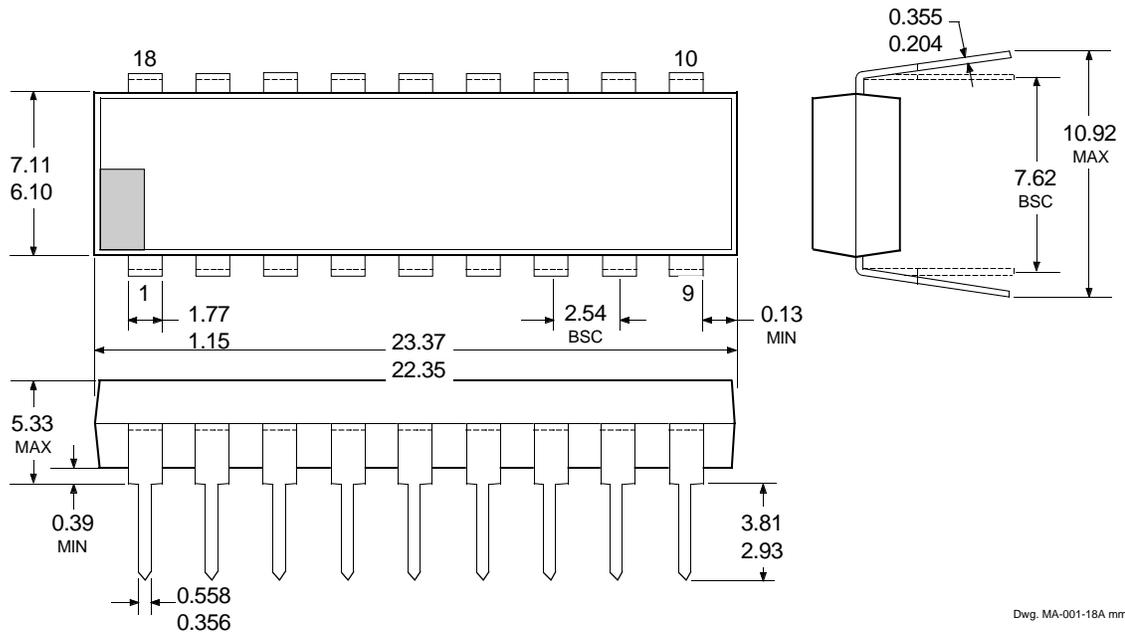
# 5810-F
## *10-BIT SERIAL-INPUT,*
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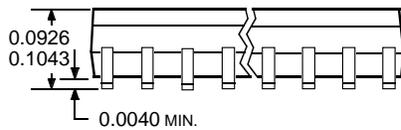### UCN5810AF

Dimensions in Inches
(controlling dimensions)

18   10

0.280
0.240

1   9

0.070
0.045

0.100
BSC

0.005
MIN

0.920
0.880

0.210
MAX

0.015
MIN

0.150
0.115

0.022
0.014

0.014
0.008

0.430
MAX

0.300
BSC

Dwg. MA-001-18A in

Dimensions in Millimeters
(for reference only)

18   10

7.11
6.10

1   9

1.77
1.15

2.54
BSC

0.13
MIN

23.37
22.35

5.33
MAX

0.39
MIN

3.81
2.93

0.558
0.356

0.355
0.204

10.92
MAX

7.62
BSC

Dwg. MA-001-18A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.
4. Supplied in standard sticks/tubes of 21 devices.

# 5810-F
## *10-BIT SERIAL-INPUT,*
## *LATCHED SOURCE DRIVERS*
## *WITH ACTIVE-DMOS PULL-DOWNS*

## UCN5810EPF

### Dimensions in Inches
### (controlling dimensions)

0.021
0.013

0.169
0.141

0.395
0.385

0.032
0.026

0.356
0.350

0.050
BSC

0.169
0.141

0.020
MIN

0.180
0.165

13      9

14      8

INDEX AREA

18      4

19  20  1  2  3

0.356
0.350

0.395
0.385
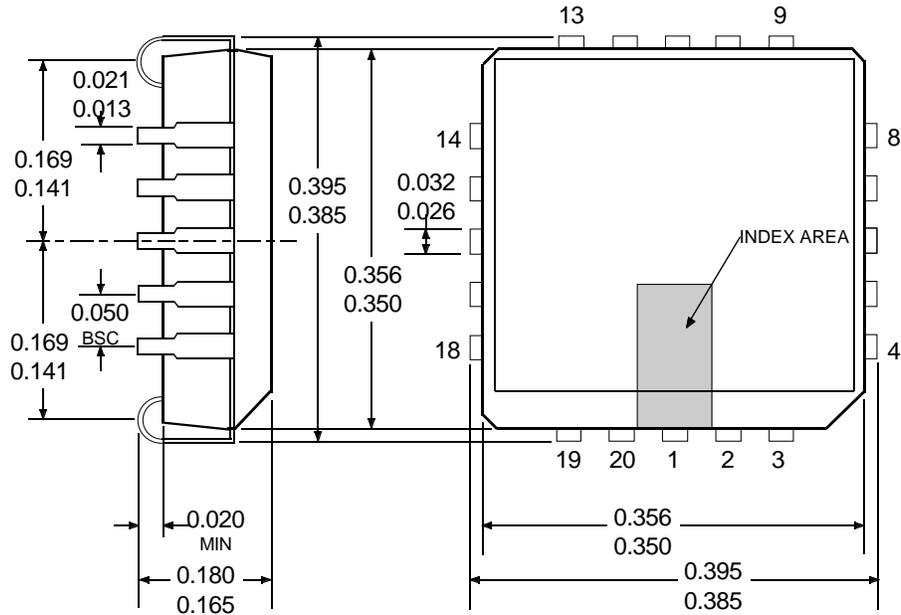
Dwg. MA-005-20A in

### Dimensions in Millimeters
### (for reference only)

0.533
0.331

4.29
3.58

10.03
9.78

0.812
0.661

9.042
8.890

1.27
BSC

4.29
3.58

0.51
MIN

4.57
4.20

13      9

14      8

INDEX AREA

18      4

19  20  1  2  3

9.042
8.890

10.03
9.78
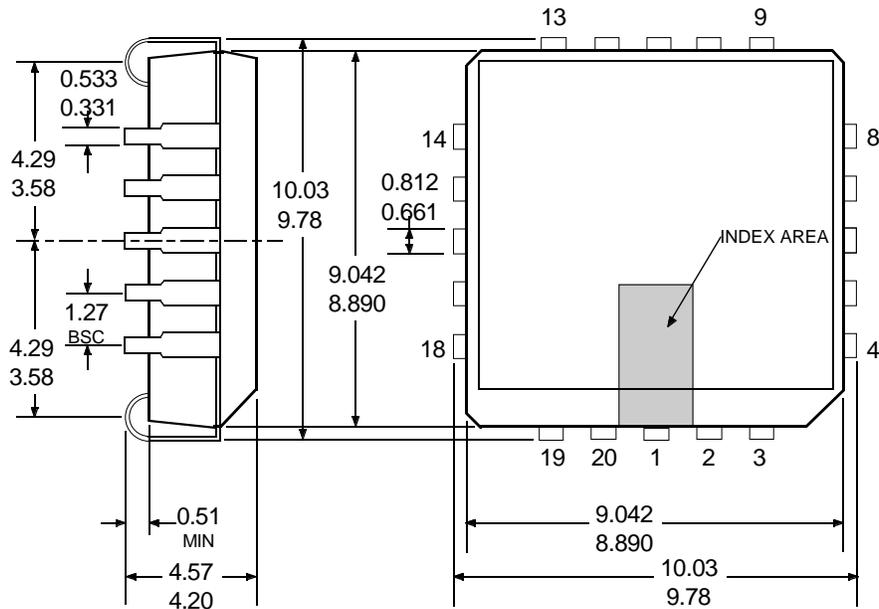
Dwg. MA-005-20A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 48 devices or add "TR" to part number for tape and reel.

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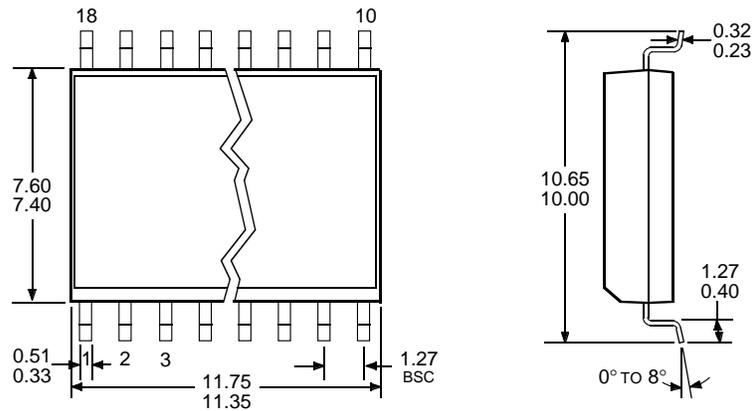Worcester, Massachusetts 01615-0036  (508) 853-5000

## UCN5810LWF

Dimensions in Inches
(for reference only)
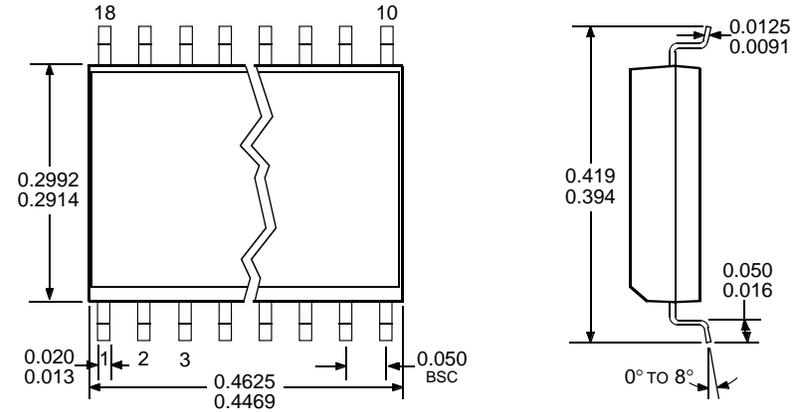


wg. MA-008-18A in

Dimensions in Millimeters
(controlling dimensions)
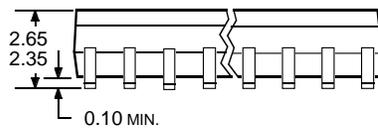


Dwg. MA-008-18A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 41 devices or add "TR" to part number for tape and reel.

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