

74ACT533

Octal Transparent Latch with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Eight latches in a single package
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24mA
- Inverted version of the ACT373
- TTL-compatible inputs

General Description

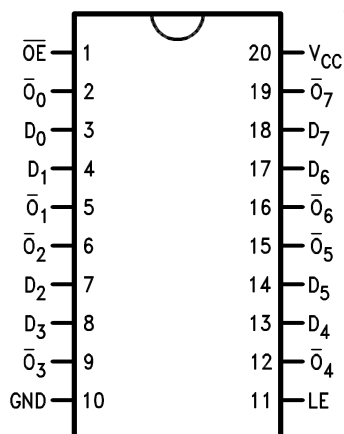
The ACT533 consists of eight latches with 3-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

Ordering Information

Order Number	Package Number	Package Description
74ACT533SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT533MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

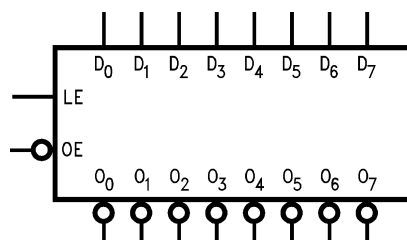
Connection Diagram



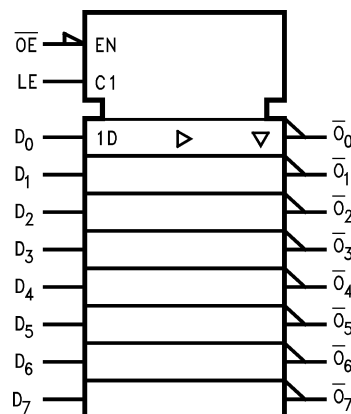
Pin Descriptions

Pin Names	Description
D_0 – D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
$\overline{O_0}$ – $\overline{O_7}$	3-STATE Latch Outputs

Logic Symbols



IEEE/IEC



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Functional Description

The ACT533 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	$\overline{O}_n$
X	H	X	Z
H	L	L	H
H	L	H	L
L	L	X	$\overline{O}_0$

H = HIGH Voltage Level

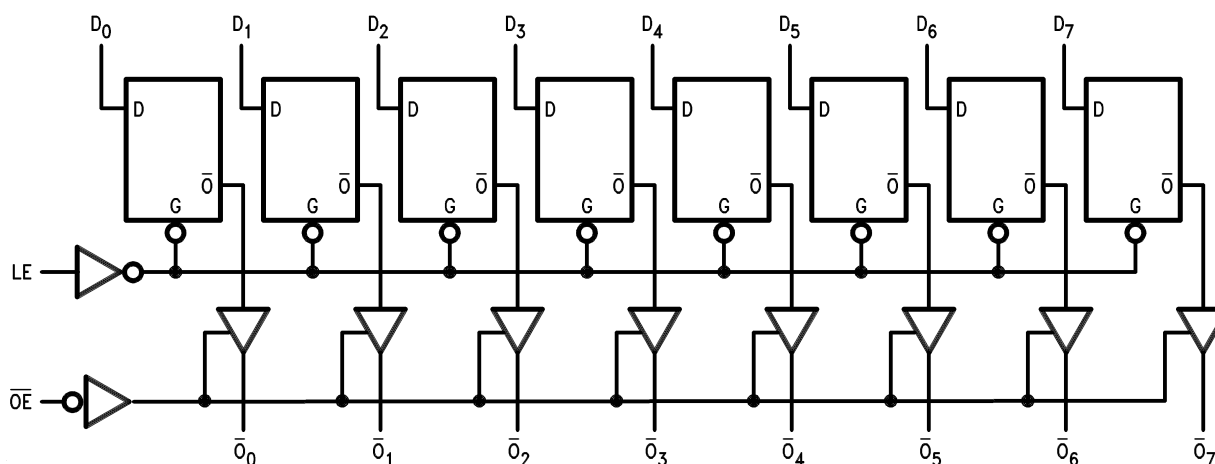
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

$\overline{O}_0$ = Previous $\overline{O}_0$ before HIGH-to-LOW transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	−20mA +20mA
V_I	DC Input Voltage	−0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	−20mA +20mA
V_O	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	−65°C to +150°C
	DC Latchup Source or Sink Current	±300mA
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = −40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = −50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V _{IN} = V _{IL} or V _{IH} ; I _{OH} = −24mA		3.86	3.76		
		5.5	I _{OH} = −24mA ⁽¹⁾		4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA		0.36	0.44		
		5.5	I _{OL} = 24mA ⁽¹⁾		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA
I _{OZ}	Maximum 3-STATE Leakage Current	5.5	V _I = V _{IL} , V _{IH} ; V _O = V _{CC} , GND		±0.25	±2.5		μA
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} − 2.1V	0.6		1.5		mA
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	V _{OLD} = 1.65V Max.			75		mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			−75		mA
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) ⁽³⁾	T _A = + 25°C, C _L = 50pF			T _A = - 40°C to + 85°C, C _L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t _{PHL} , t _{PLH}	Propagation Delay, D _n to O _n	5.0	2.0	6.0	8.0	2.0	8.5	ns
t _{PHL} , t _{PLH}	Propagation Delay, LE to O _n	5.0	2.5	7.0	9.0	2.5	9.5	ns
t _{PZL} , t _{PZH}	Output Enable Time	5.0	2.0	7.0	9.0	2.0	9.5	ns
t _{PHZ} , t _{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.0	10.5	ns

Note:

3. Voltage range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

Symbol	Parameter	V _{CC} (V) ⁽⁴⁾	T _A = + 25°C, C _L = 50pF		T _A = − 40°C to + 85°C, C _L = 50pF	Units
			Typ.	Guaranteed Minimum		
t _S	Setup Time, HIGH or LOW, D _n to LE	5.0	0	3.0	3.0	ns
t _H	Hold Time, HIGH or LOW, D _n to LE	5.0	0	1.5	1.5	ns
t _W	LE Pulse Width, HIGH	5.0	2.0	4.0	4.0	ns

Note:

4. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	40	pF

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

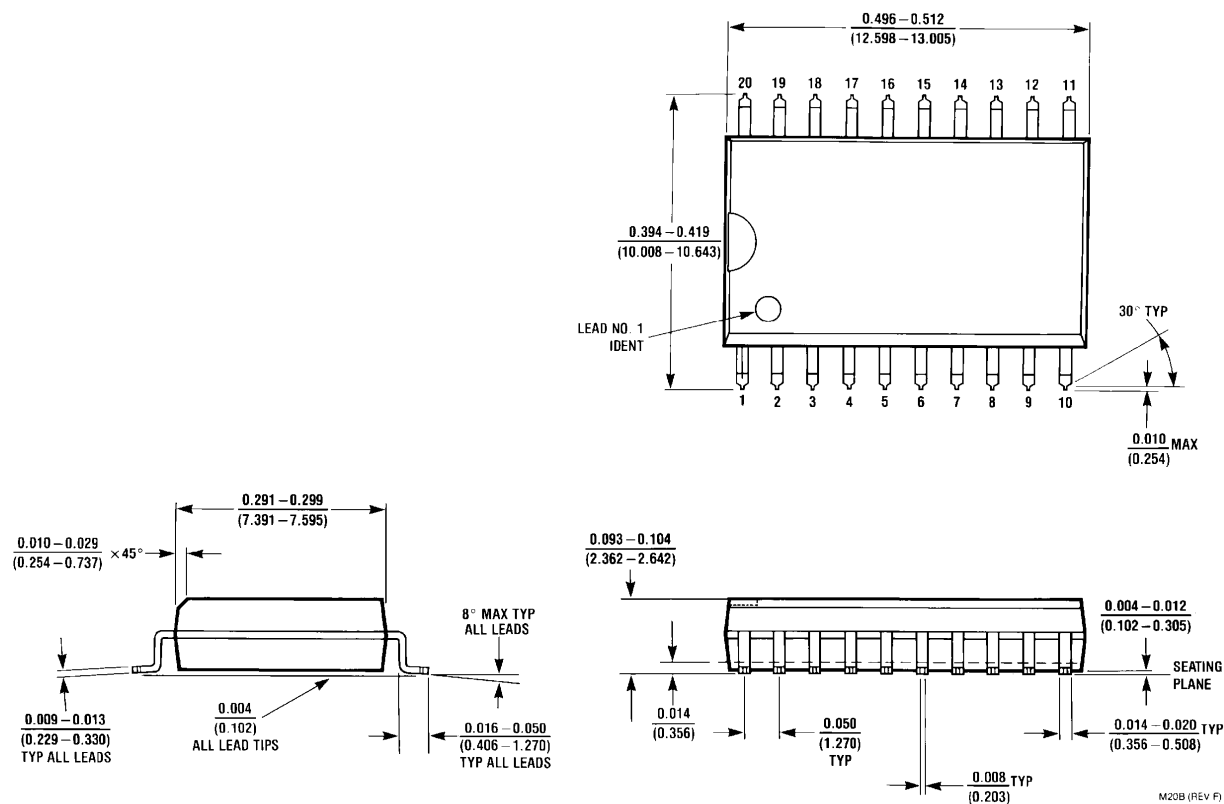
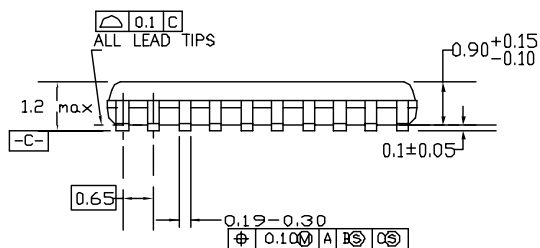
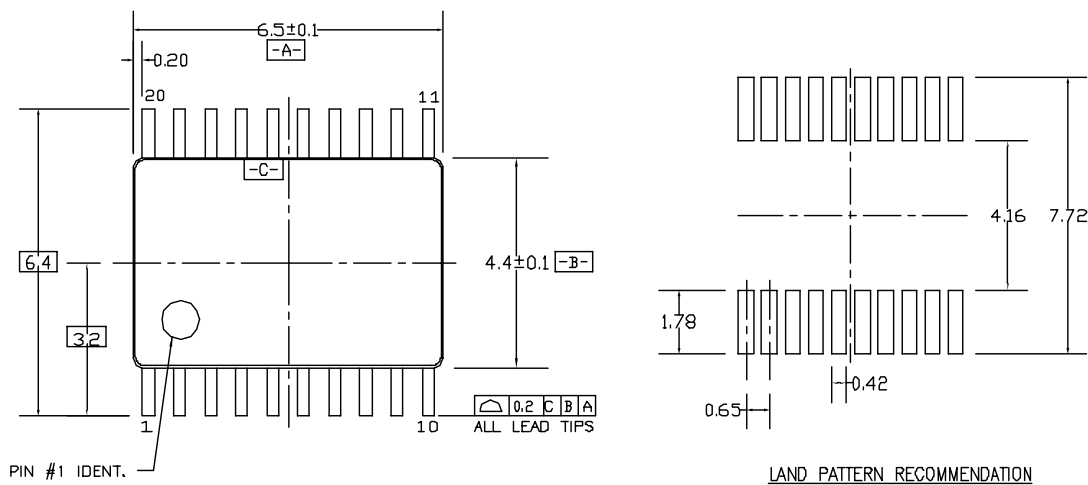


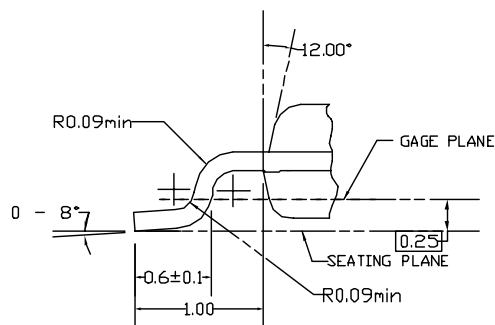
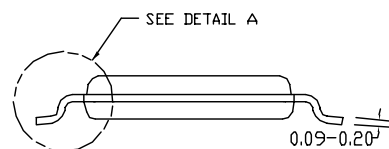
Figure 2. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20



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