# MAX16056–MAX16059

# 125nA Supervisory Circuits with Capacitor-Adjustable Reset and Watchdog Timeouts

## General Description

The MAX16056–MAX16059 are ultra-low-current 125nA (typ) microprocessor (µP) supervisory circuits that monitor a single system supply voltage. These devices assert an active-low reset signal whenever the $V_{CC}$ supply voltage drops below the factory-trimmed reset threshold, manual reset is pulled low, or the watchdog timer runs out (MAX16056/MAX16058). The reset output remains asserted for an adjustable reset timeout period after $V_{CC}$ rises above the reset threshold. Factory-trimmed reset threshold voltages are offered from 1.575V to 4.625V in approximately 100mV increments (see Table 1).

These devices feature adjustable reset and watchdog timeout using external capacitors. The MAX16056/MAX16058 contain a watchdog timer with a watchdog select input (WDS) that multiplies the watchdog timeout period by 128. The MAX16057/MAX16059 do not have the watchdog feature.

The MAX16056–MAX16059 are available in either push-pull or open-drain output-type configurations (see the *Ordering Information*). These devices are fully specified over the -40°C to +125°C automotive temperature range. The MAX16056/MAX16058 are available in an 8-pin TDFN package, and the MAX16057/MAX16059 are available in a 6-pin TDFN package.

## Applications

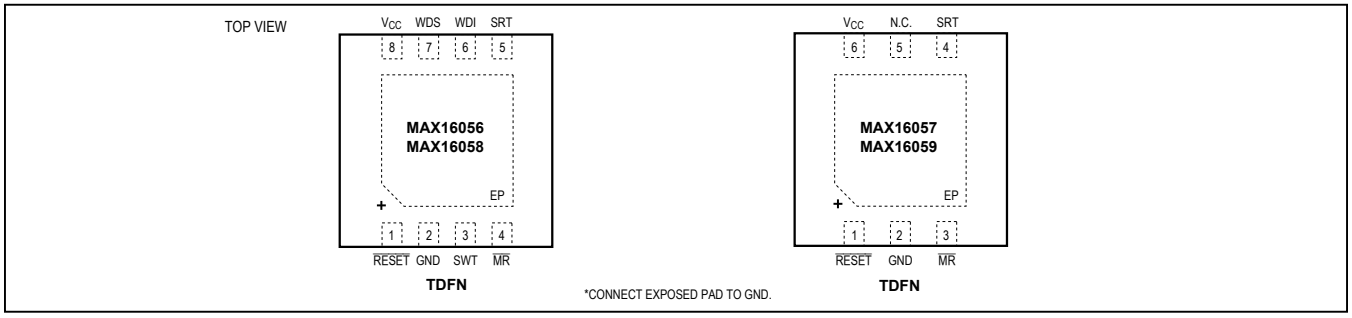
- Portable/Battery-Powered Equipment
- PDAs/Cell Phones
- MP3 Players/Pagers
- Glucose Monitors/Patient Monitors
- Metering/HVAC

## Benefits and Features

- Reduced Power Requirements
  - Ultra-Low 125nA (typ) Supply Current
  - 1.1V to 5.5V Operating Supply Range
- Configurable Circuit Enables Flexible Designs
  - Factory-Set Reset Threshold Options from 1.575V to 4.625V in Approximately 100mV Increments
  - Capacitor-Adjustable Reset Timeout
  - Capacitor-Adjustable Watchdog Timeout (MAX16056/MAX16058)
  - Watchdog Timer Capacitor Open Detect Function
  - Optional Watchdog Disable Function (MAX16056/MAX16058)
  - Manual-Reset Input
  - Push-Pull or Open-Drain $\overline{RESET}$ Output Options
- Integrated Features Increases System Robustness
  - Power-Supply Transient Immunity
  - Guaranteed $\overline{RESET}$ Valid for $V_{CC} \geq 1.1V$
- Saves Board Space
  - 3mm x 3mm TDFN Package

***Typical Operating Circuit* and *Ordering Information* appear at end of data sheet.***

## Pin Configurations



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## Absolute Maximum Ratings

$V_{CC}$ to GND .....-0.3V to +6V
SRT, SWT, WDS, MR, WDI, to GND.....-0.3V to ($V_{CC}$ + 0.3V)
$\overline{RESET}$ (Push-Pull) to GND .....-0.3V to ($V_{CC}$ + 0.3V)
$\overline{RESET}$ (Open-Drain) to GND .....-0.3V to +6V
Input Current (all pins).....±20mA
Output Current ($\overline{RESET}$).....±20mA
Continuous Power Dissipation ($T_A$ = +70°C)
6-Pin TDFN (derate 23.8mW/°C above +70°C) .....1905mW
8-Pin TDFN (derate 24.4mW/°C above +70°C) .....1951mW

Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 1)

6 TDFN
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....42°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$).....9°C/W

8 TDFN
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....41°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$).....8°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{CC}$ = 1.2V to 5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = 3.3V, $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | $T_A$ = 0°C to +125°C | | 1.1 | | 5.5 | V |
| | | $T_A$ = -40°C to 0°C | | 1.2 | | 5.5 | |
| Supply Current | $I_{CC}$ | $V_{CC}$ > $V_{TH}$ + 150mV, no load, reset output deasserted (Note 3) | $V_{CC}$ = 5.0V, $T_A$ = -40°C to +85°C | | 142 | 210 | nA |
| | | | $V_{CC}$ = 3.3V, $T_A$ = -40°C to +85°C | | 132 | 185 | |
| | | | $V_{CC}$ = 1.8V, $T_A$ = -40°C to +85°C | | 125 | 175 | |
| | | | $V_{CC}$ = 5.0V, $T_A$ = -40°C to +125°C | | 142 | 430 | |
| | | | $V_{CC}$ = 3.3V, $T_A$ = -40°C to +125°C | | 132 | 415 | |
| | | | $V_{CC}$ = 1.8V, $T_A$ = -40°C to +125°C | | 125 | 400 | |
| | | $V_{CC}$ < $V_{TH}$, no load, reset output asserted | | | 7 | 15 | µA |
| $V_{CC}$ Reset Threshold | $V_{TH}$ | $V_{CC}$ falling (see Table 1) | $T_A$ = +25°C | $V_{TH}$ - 1.5% | | $V_{TH}$ + 1.5% | V |
| | | | $T_A$ = -40°C to +125°C | $V_{TH}$ - 2.5% | | $V_{TH}$ + 2.5% | |
| Hysteresis | $V_{HYST}$ | $V_{CC}$ rising | | | 0.5 | | % |

## Electrical Characteristics (continued)

($V_{CC}$ = 1.2V to 5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = 3.3V, $T_A$ = +25°C.) (Note 2)

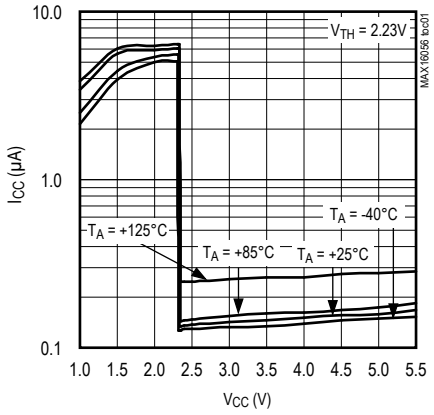
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ to Reset Delay | $t_{RD}$ | $V_{CC}$ falling from ($V_{TH}$ + 100mV) to ($V_{TH}$ - 100mV) at 10mV/µs | | | 80 | | µs |
| Reset Timeout Period | $t_{RP}$ | $C_{SRT}$ = 2700pF (Note 4) | | 10.5 | 14.18 | 17.0 | ms |
| SRT Ramp Current | $I_{RAMP1}$ | $V_{SRT}$ = 0V to $V_{RAMP1}$, $V_{CC}$ = 1.6V to 5V | $T_A$ = -40°C to +125°C | 197 | 240 | 282 | nA |
| | | | $T_A$ = +25°C | 210 | 240 | 270 | |
| SRT Ramp Threshold | $V_{RAMP1}$ | $V_{CC}$ = 1.6V to 5V ($V_{RAMP}$ rising) | | 1.173 | 1.235 | 1.297 | V |
| Watchdog Timeout Clock Period | $t_{WDPER}$ | $T_A$ = +25°C | | 5 | 6.4 | 8 | ms |
| | | $T_A$ = -40°C to +125°C | | 3.5 | 6.4 | 9.5 | |
| SWT Ramp Current | $I_{RAMP2}$ | $V_{SWT}$ = 0V to $V_{RAMP2}$, $V_{CC}$ = 1.6V to 5V | $T_A$ = -40°C to +125°C | 197 | 240 | 282 | nA |
| | | | $T_A$ = +25°C | 210 | 240 | 270 | |
| SWT Ramp Threshold | $V_{RAMP2}$ | $V_{CC}$ = 1.6V to 5V ($V_{RAMP2}$ rising) | | 1.173 | 1.235 | 1.297 | V |
| $\overline{RESET}$ Output Voltage | $V_{OL}$ | $V_{CC}$ ≥ 1.0V, $I_{SINK}$ = 50µA | | | | 0.3 | V |
| | | $V_{CC}$ ≥ 2.7V, $I_{SINK}$ = 1.2mA | | | | 0.3 | |
| | | $V_{CC}$ ≥ 4.5V, $I_{SINK}$ = 3.2mA | | | | 0.4 | |
| | $V_{OH}$ | MAX16056/MAX16057 | $V_{CC}$ ≥ 1.8V, $I_{SOURCE}$ = 200µA | 0.8 x $V_{CC}$ | | | |
| | | | $V_{CC}$ ≥ 2.25V, $I_{SOURCE}$ = 500µA | 0.8 x $V_{CC}$ | | | |
| | | | $V_{CC}$ ≥ 4.5V, $I_{SOURCE}$ = 800µA | 0.8 x $V_{CC}$ | | | |
| $\overline{RESET}$ Output-Leakage Current, Open Drain | $I_{LKG}$ | $V_{CC}$ > $V_{TH}$, reset not asserted, $V_{\overline{RESET}}$ = 5.5V (MAX16058/MAX16059) | | | | 1.0 | µA |
| Input-Logic Levels | $V_{IH}$ | | | 0.7 x $V_{CC}$ | | | V |
| | $V_{IL}$ | | | | | 0.3 x $V_{CC}$ | |
| $\overline{MR}$ Minimum Pulse Width | $t_{MPW}$ | | | 1 | | | µs |
| $\overline{MR}$ Glitch Rejection | | | | | 200 | | ns |
| $\overline{MR}$-to-$\overline{RESET}$ Delay | $t_{MRD}$ | | | | 250 | | ns |
| WDI Minimum Pulse Width | | (Note 5) | | 150 | | | ns |
| Input Leakage Current | | $\overline{MR}$, WDI, WDS is connected to GND or $V_{CC}$ | | -100 | | +100 | nA |

**Note 2:** Devices are production tested at $T_A$ = +25°C. Specifications over temperature limits are guaranteed by design.
**Note 3:** WDI input period is 1s with $t_{RISE}$ and $t_{FALL}$ < 50ns.
**Note 4:** Worst case of SRT ramp current and voltage is used to guarantee minimum and maximum limits.
**Note 5:** Guaranteed by design, not production tested.

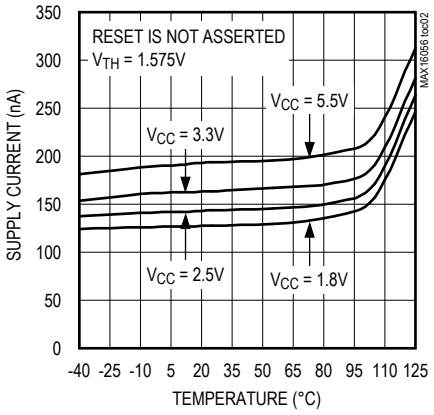
## Typical Operating Characteristics

($V_{CC}$ = 2.5V, $T_A$ = +25°C, unless otherwise noted.)

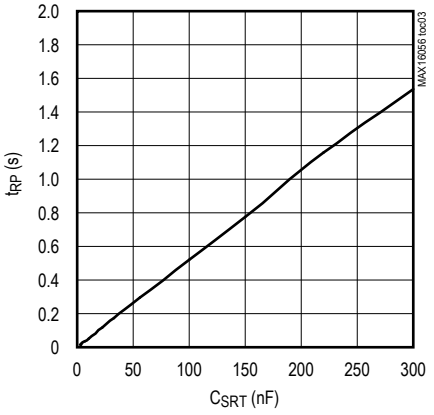
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



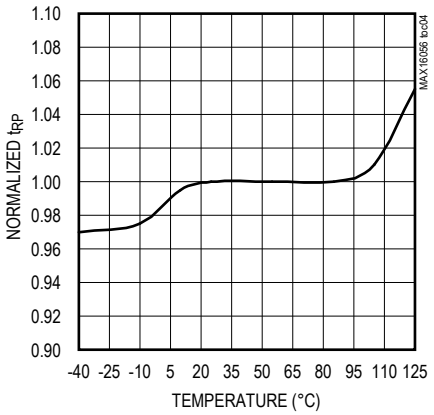

**SUPPLY CURRENT vs. TEMPERATURE**



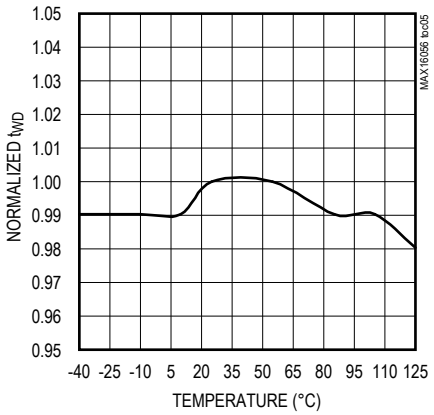

**RESET TIMEOUT PERIOD vs. $C_{SRT}$**



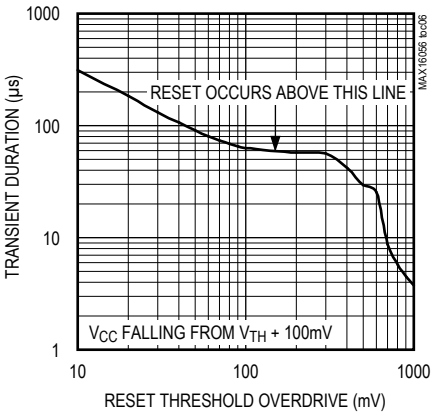

**NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE**



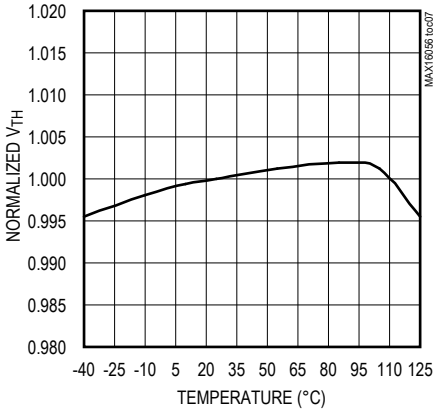

**NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE**



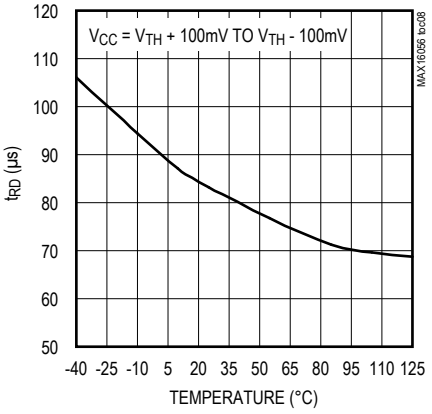

**MAXIMUM $V_{CC}$ TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE**




**NORMALIZED RESET THRESHOLD VOLTAGE vs. TEMPERATURE**



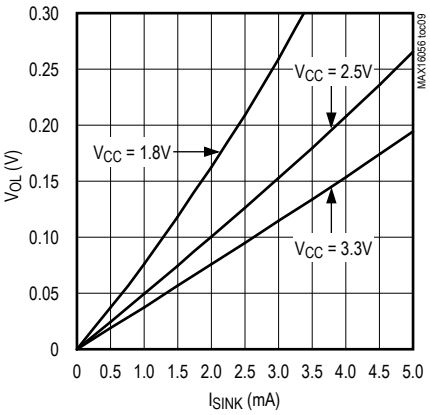

**$V_{CC}$ TO RESET DELAY vs. TEMPERATURE**



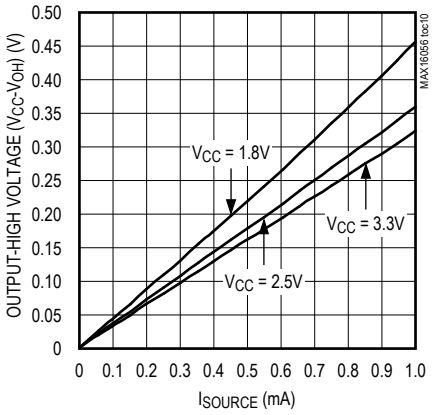
## Typical Operating Characteristics (continued)

($V_{CC}$ = 2.5V, $T_A$ = +25°C, unless otherwise noted.)

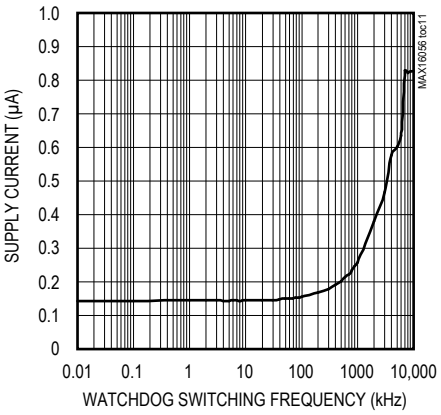
**$\overline{RESET}$ OUTPUT-LOW VOLTAGE vs. SINK CURRENT**



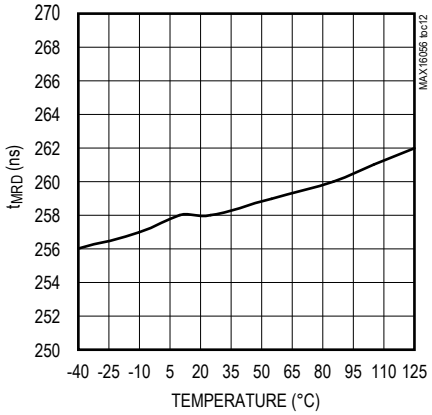

**$\overline{RESET}$ OUTPUT-HIGH VOLTAGE vs. SOURCE CURRENT**



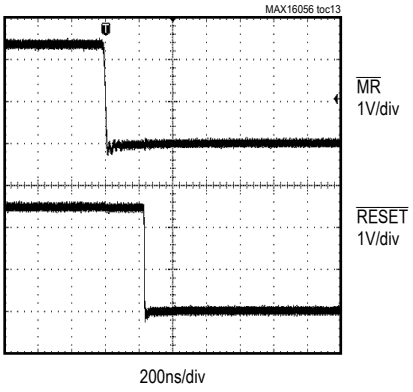

**SUPPLY CURRENT vs. WATCHDOG SWITCHING FREQUENCY**



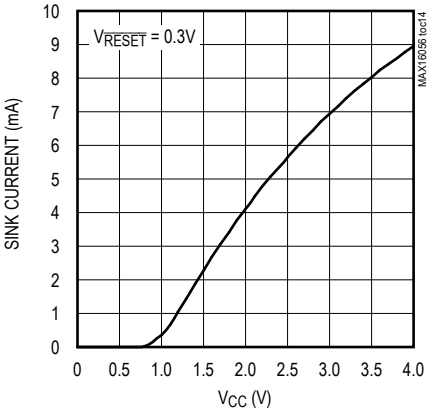

**MANUAL-RESET DELAY vs. TEMPERATURE**



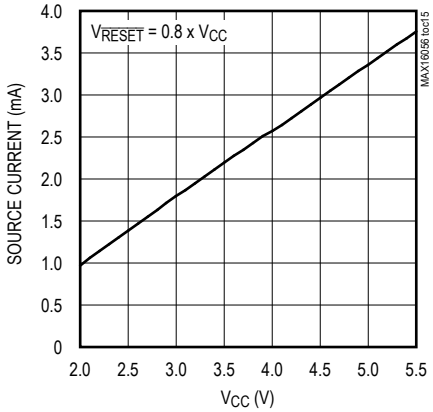

**MANUAL-RESET DELAY**




**$\overline{RESET}$ SINK CAPABILITY vs. SUPPLY VOLTAGE**




**$\overline{RESET}$ SOURCE CAPABILITY vs. SUPPLY VOLTAGE**



## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX16056/ MAX16058 | MAX16057/ MAX16059 | | |
| 1 | 1 | $\overline{\text{RESET}}$ | Push-Pull or Open-Drain Reset Output. $\overline{\text{RESET}}$ asserts whenever $V_{CC}$ drops below the selected reset threshold voltage ($V_{TH}$) or manual reset is pulled low. $\overline{\text{RESET}}$ remains low for the reset timeout period after all reset conditions are deasserted, and then goes high. The watchdog timer triggers a reset pulse ($t_{RP}$) whenever a watchdog fault occurs (MAX16056/MAX16058). |
| 2 | 2 | GND | Ground |
| 3 | — | SWT | Watchdog Timeout Input. Connect a capacitor between SWT and GND to set the basic watchdog timeout period ($t_{WD}$). Determine the period by the formula $t_{WD}$ = Floor[$C_{SWT}$ x 5.15 x $10^6$/6.4ms] x 6.4ms + 3.2ms (Note 6) with $t_{WD}$ in seconds and $C_{SWT}$ in Farads, or use Table 2. Extend the basic watchdog timeout period by using the WDS input. Connect SWT to ground to disable the watchdog timer function. The value of the capacitor must be between 2275pF and 0.54µF to have a valid watchdog timeout period. |
| 4 | 3 | $\overline{\text{MR}}$ | Manual-Reset Input. Drive $\overline{\text{MR}}$ low to manually reset the device. $\overline{\text{RESET}}$ remains asserted for the reset timeout period after $\overline{\text{MR}}$ is released. There is no internal pullup on $\overline{\text{MR}}$. $\overline{\text{MR}}$ must not be left unconnected. Connect $\overline{\text{MR}}$ to $V_{CC}$ if not used. |
| 5 | 4 | SRT | Reset Timeout Input. Connect a capacitor from SRT to GND to select the reset timeout period. Determine the period as follows: $t_{RP}$ = 5.15 x $10^6$ x $C_{SRT}$ with $t_{RP}$ in seconds and $C_{SRT}$ in Farads, or use Table 2. The value of the capacitor must be between 39pF and 4.7µF. |
| 6 | — | WDI | Watchdog Input. A falling transition must occur on WDI within the selected watchdog timeout period or a reset pulse occurs. The watchdog timer clears when a falling transition occurs on WDI or whenever $\overline{\text{RESET}}$ is asserted. Connect SWT to ground to disable the watchdog timer function. |
| 7 | — | WDS | Watchdog Select Input. WDS selects the watchdog timeout mode. Connect WDS to ground to select normal mode. The watchdog timeout period is $t_{WD}$. Connect WDS to $V_{CC}$ to select extended mode, multiplying the basic timeout period ($t_{WD}$) by a factor of 128. A change in the state of WDS clears the watchdog timer. |
| 8 | 6 | $V_{CC}$ | Supply Voltage. $V_{CC}$ is the power-supply input and the input for fixed-threshold $V_{CC}$ monitor. For noisy systems, bypass $V_{CC}$ with a 0.1µF capacitor to GND. |
| — | 5 | N.C. | No Connection. Not internally connected. |
| — | — | EP | Exposed Pad. Connect EP to GND or leave unconnected. |

**Note 6:** Floor: take the integral value.

## Detailed Description

The MAX16056–MAX16059 are ultra-low-current 125nA (typ) µP supervisory circuits that monitor a single system supply voltage. These devices assert an active-low reset signal whenever the $V_{CC}$ supply voltage drops below the factory-trimmed reset threshold, manual reset is pulled low, or the watchdog timer runs out (MAX16056/MAX16058). The reset output remains asserted for an adjustable reset timeout period after $V_{CC}$ rises above the reset threshold. The reset and watchdog delay periods are adjustable using external capacitors.

### $\overline{\text{RESET}}$ Output

The MAX16056–MAX16059 µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. The reset output is guaranteed to be valid for $V_{CC}$ down to 1.1V.

When $V_{CC}$ falls below the reset threshold, the $\overline{\text{RESET}}$ output asserts low. Once $V_{CC}$ exceeds the reset threshold plus the hysteresis, an internal timer keeps the $\overline{\text{RESET}}$ output asserted for the capacitor-adjusted reset timeout period ($t_{RP}$), then after this interval the $\overline{\text{RESET}}$ output deasserts (Figure 1). The reset function features immunity to power-supply voltage transients.

### Manual-Reset Input ($\overline{\text{MR}}$)

Many µP-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. The MAX16056–MAX16059 feature an $\overline{\text{MR}}$ input. A logic-low on $\overline{\text{MR}}$ asserts a reset. $\overline{\text{RESET}}$ remains asserted while $\overline{\text{MR}}$ is low and for the timeout period ($t_{RP}$)after $\overline{\text{MR}}$ returns high. Connect $\overline{\text{MR}}$ to $V_{CC}$ if unused. $\overline{\text{MR}}$ can be driven with CMOS logic levels or with open-drain/collector outputs (with a pullup resistor). Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND and a resistor from $\overline{\text{MR}}$ to $V_{CC}$ to implement a manual-reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven by long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{\text{MR}}$ to GND to provide additional noise immunity.

### Watchdog Timer

The MAX16056/MAX16058's watchdog timer circuitry monitors the µP's activity. If the µP does not toggle (high to low) the watchdog input (WDI) within the capacitor-adjustable watchdog timeout period ($t_{WD}$), $\overline{\text{RESET}}$ asserts for the reset timeout period ($t_{RP}$). The internal watchdog timer is cleared by: 1) any event that asserts $\overline{\text{RESET}}$, 2) a falling transition at WDI (that can detect pulses as short as 150ns), or 3) a transition (high to low or low to high) at WDS. While $\overline{\text{RESET}}$ is asserted, the watchdog timer remains cleared and does not count. As soon as $\overline{\text{RESET}}$ deasserts, the watchdog timer resumes counting.

There are two modes of watchdog operation, normal mode and extended mode. In normal mode (Figure 2), the watchdog timeout period is determined by the value of the capacitor connected between SWT and ground. In extended mode (Figure 3), the watchdog timeout period is multiplied by 128. For example, in extended mode, a 0.33µF capacitor gives a watchdog timeout period of 217s (Table 2). To disable the watchdog timer function, connect SWT to ground.

When $V_{CC}$ ramps above $V_{TH}$ + $V_{HYST}$, the value of the external SWT capacitor is sampled after $\overline{\text{RESET}}$ goes high. When sampling is finished, the capacitor value is stored in the device and is used to set watchdog timeout. If $\overline{\text{RESET}}$ goes low before sampling is finished, the device interrupts sampling, and sampling is restarted when $\overline{\text{RESET}}$ goes high again.

If the external SWT capacitor is less than 470pF, the sampling result sets the watchdog timeout to zero. This causes the watchdog to assert $\overline{\text{RESET}}$ continuously after sampling is finished. If a PCB manufacturing defect caused the connection to $C_{SWT}$ to be broken, the capacitance is very low and $\overline{\text{RESET}}$ is continuously asserted. If the external SWT capacitor is greater than 0.47µF, the sampling result sets the watchdog timeout to be infinite, disabling the watchdog function.

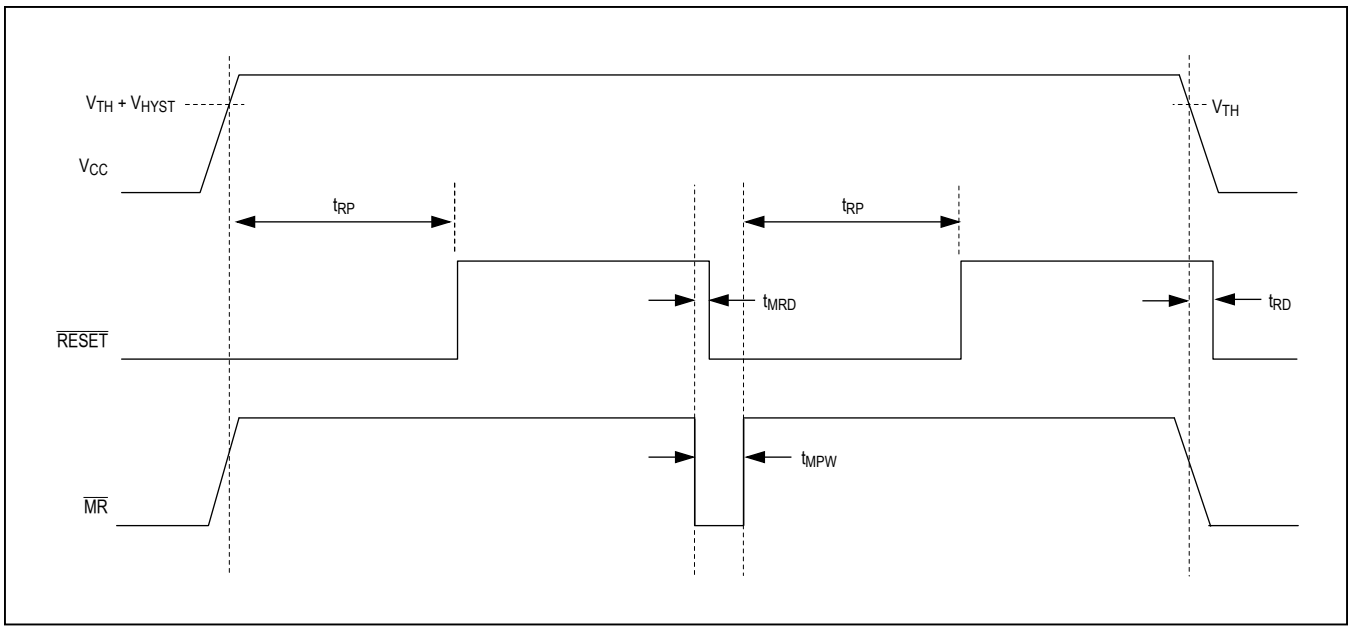



*Figure 1. $\overline{RESET}$ Timing Relationship*

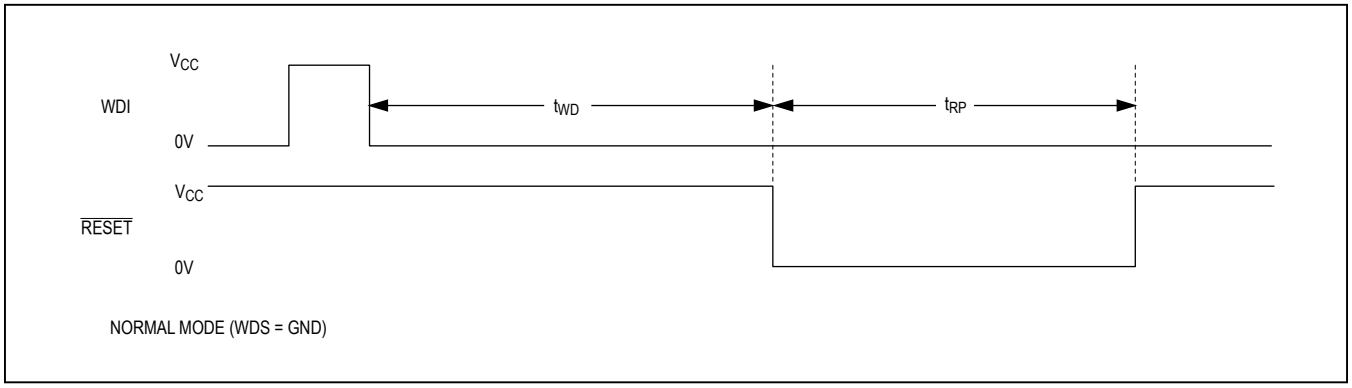



*Figure 2. Watchdog Timing Diagram, Normal Mode (WDS = GND)*

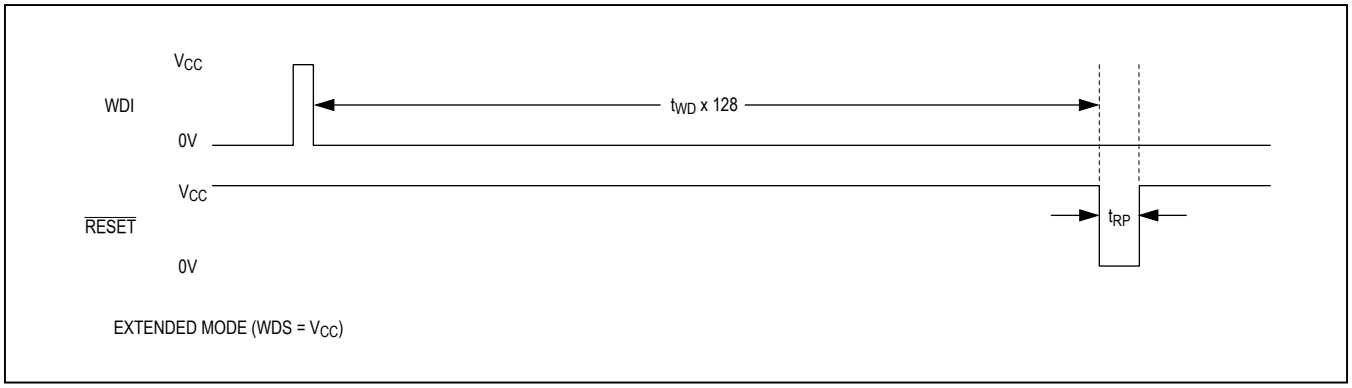



*Figure 3. Watchdog Timing Diagram, Extended Mode (WDS = $V_{CC}$)*

## Applications Information

### Selecting the Reset Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of µP applications. To adjust the reset timeout period ($t_{RP}$), connect a capacitor ($C_{SRT}$) between SRT and ground. The reset timeout capacitor is calculated as follows:

$$C_{SRT} = t_{RP}/(5.15 \times 10^6)$$

with $t_{RP}$ in seconds and $C_{SRT}$ in Farads.

$C_{SRT}$ must be a low-leakage (< 10nA) type capacitor. A ceramic capacitor with low temperature coefficient dielectric (i.e., X7R) is recommended.

### Selecting Watchdog Timeout Capacitor

The watchdog timeout period is adjustable to accommodate a variety of µP applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer can determine how often the watchdog timer should be serviced. Adjust the watchdog timeout period ($t_{WD}$) by connecting a capacitor ($C_{SWT}$) between SWT and GND. For normal mode operation, calculate the watchdog timeout as follows:

$t_{WD}$ = Floor[$C_{SWT}$ x 5.15 x $10^6$/6.4ms] x 6.4ms + 3.2ms

with $t_{WD}$ in seconds and $C_{SWT}$ in Farads.

(Floor: take the integral value) (Figures 2 and 3)

The maximum $t_{WD}$ is 296s. If the capacitor sets $t_{WD}$ greater than the 296s, $t_{WD}$ = infinite and the watchdog timer is disabled.

$C_{SWT}$ must be a low-leakage (< 10nA) type capacitor. A ceramic capacitor with low temperature coefficient dielectric (i.e., X7R) is recommended.

### Watchdog Timeout Accuracy

The watchdog timeout period is affected by the SWT ramp current ($I_{RAMP2}$) accuracy, the SWT ramp threshold ($V_{RAMP2}$), and the watchdog timeout clock period ($t_{WDPER}$). In the equation above, the constant 5.15 x $10^6$ is equal to $V_{RAMP2}/I_{RAMP2}$, and 6.4ms equals the watchdog timeout clock period. Calculate the timeout accuracy by substituting the minimum, typical, and maximum values into the equation.

For example, if $C_{SWT}$ = 100nF:

$t_{WDMIN}$ = Floor[100 x $10^{-9}$ x 1.173/(282 x $10^{-9}$)/9.5ms] x 3.5ms + 0.5 x 3.2ms = 141.7ms

$t_{WDNOM}$ = Floor[100 x $10^{-9}$ x 1.235/(240 x $10^{-9}$)/6.4ms] x 6.4ms + 0.5 x 6.4ms = 515.2ms

$t_{WDMAX}$ = Floor[100 x $10^{-9}$ x 1.297/(197 x $10^{-9}$)/3.5ms] x 9.5ms + 0.5 x 9.5ms = 1790.75ms

### Transient Immunity

For applications with higher slew rates on $V_{CC}$ during power-up, additional bypass capacitance may be required.

The MAX16056–MAX16059 are relatively immune to short-duration supply voltage transients, or glitches on $V_{CC}$. The Maximum $V_{CC}$ Transient Duration vs. Reset Threshold Overdrive graph in the *Typical Operating Characteristics* shows this transient immunity. The area below the curve of the graph is the region where these devices typically do not generate a reset pulse. This graph was generated using a falling pulse applied to $V_{CC}$, starting 100mV above the actual reset threshold ($V_{TH}$), and ending below this threshold (reset threshold overdrive). As the magnitude of the transient increases, the maximum allowable pulse width decreases. Typically, a 100mV $V_{CC}$ transient duration of 40µs or less does not cause a reset.

### Using the MAX16056–MAX16059 for Reducing System Power Consumption

Using the $\overline{\text{RESET}}$ output to control an external p-channel MOSFET to control the on-time of a power supply can result in lower system power consumption in systems that can be regularly put to sleep. By tying the WDI input to ground, the $\overline{\text{RESET}}$ output becomes a low-frequency clock output. When $\overline{\text{RESET}}$ is low, the MOSFET is turned on and power is applied to the system. When $\overline{\text{RESET}}$ is high, the MOSFET is turned off and no power is consumed by the system. This effectively reduces the shutdown current of the system to zero (Figure 4).

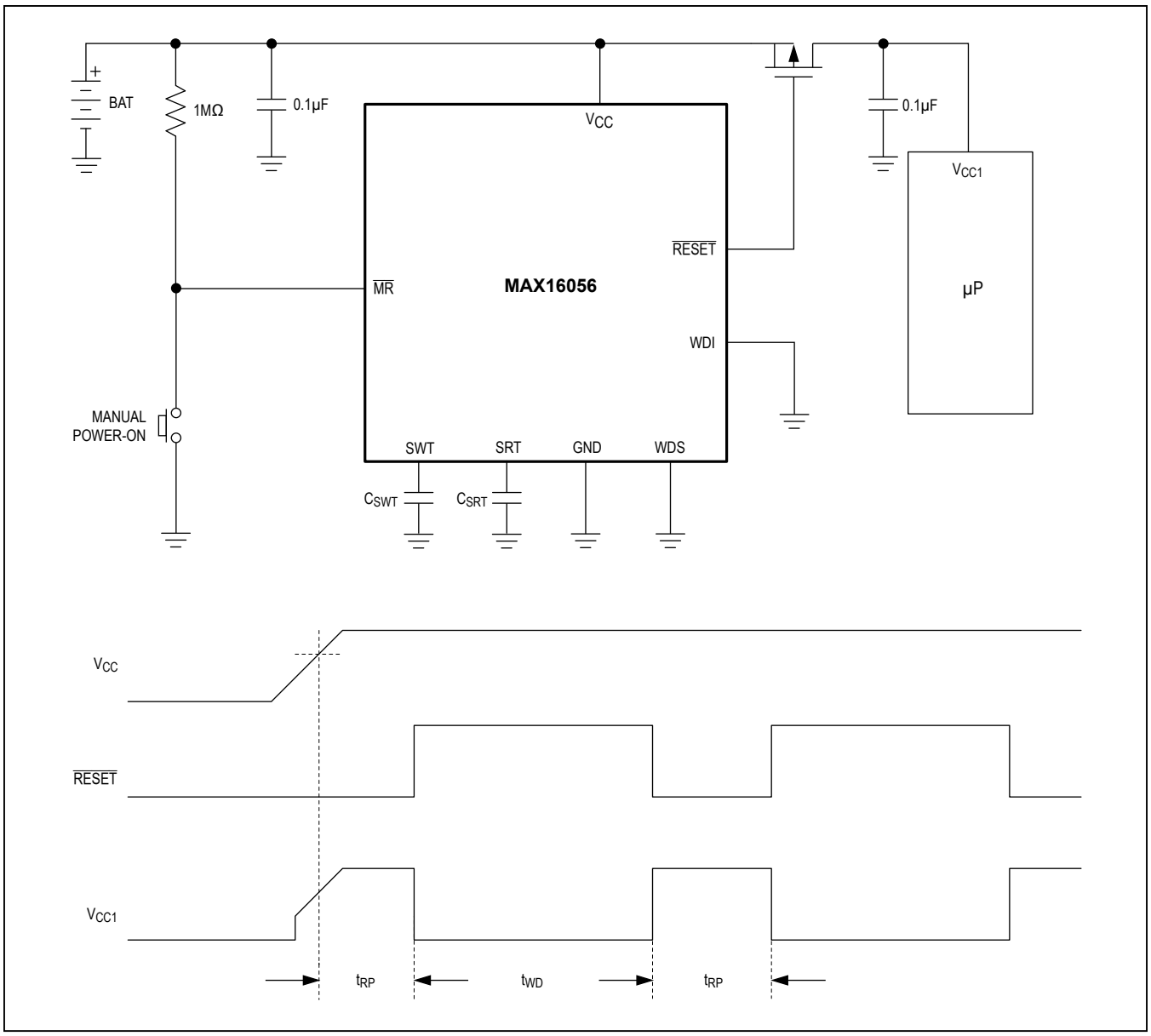



*Figure 4. Using MAX16056–MAX16059 to Reduce System Power Consumption*

### Interfacing to Other Voltages for Logic Compatibility

The open-drain $\overline{RESET}$ output can be used to interface to a µP with other logic levels. The open-drain output is connected to a voltage from 0 to 5.5V, as shown in Figure 5. Generally, the pullup resistor connected to $\overline{RESET}$ connects to the supply voltage that is being monitored at the device's $V_{CC}$ input. However, some systems use the open-drain output to level-shift from the supervisor's monitored supply to another supply voltage. As the supervisor's $V_{CC}$ decreases, so does the device's ability to sink current at $\overline{RESET}$.

### Ensuring a Valid $\overline{RESET}$ Down to $V_{CC}$ = 0V (Push-Pull $\overline{RESET}$)

When $V_{CC}$ falls below 1.1V, the current-sinking capability of $\overline{RESET}$ decreases drastically. The high-impedance CMOS logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problems in most applications, since most µPs and other circuitry do not operate with $V_{CC}$ below 1.1V. In those applications where $\overline{RESET}$ must be valid down to 0V, add a pulldown resistor between the MAX16056/MAX16057 push-pull $\overline{RESET}$ output and GND. The resistor sinks any stray leakage currents, holding $\overline{RESET}$ low (Figure 6). Choose a pulldown resistor that accommodates leakages, such that $\overline{RESET}$ is not significantly loaded and is capable of pulling to GND. The external pulldown cannot be used with the open-drain $\overline{RESET}$ output of the MAX16058/MAX16059.

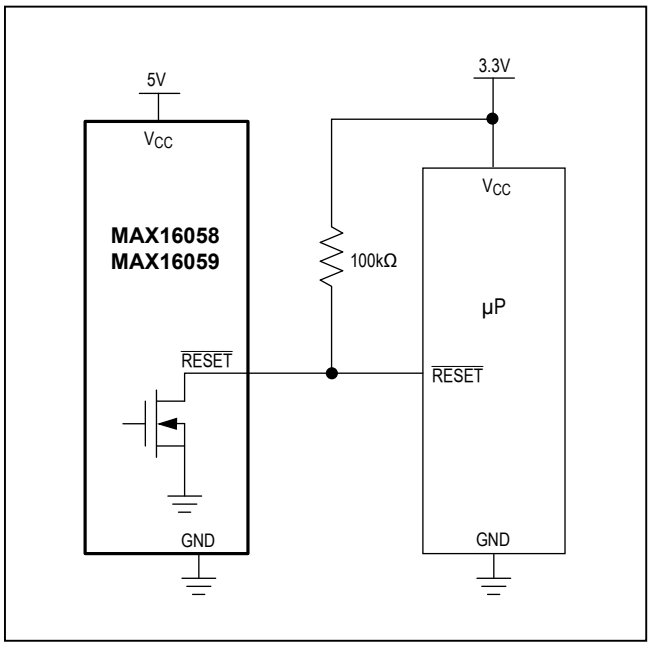



*Figure 5. Interfacing with Other Voltage Levels*

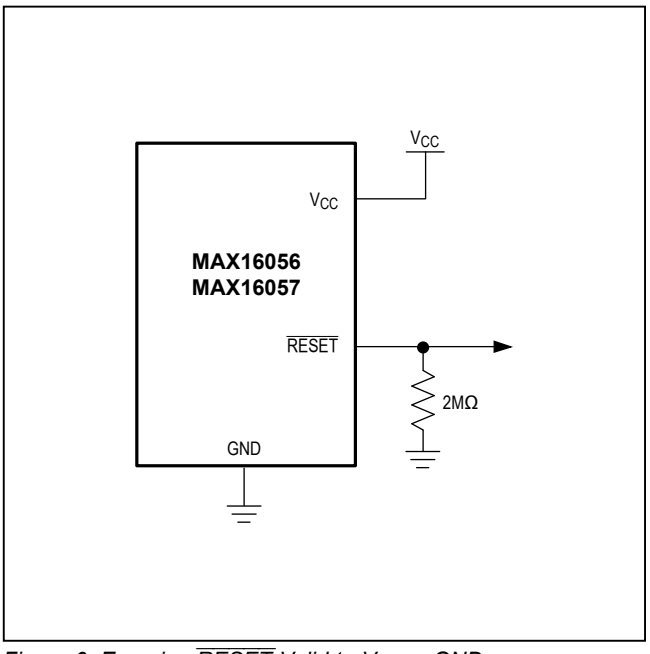



*Figure 6. Ensuring $\overline{RESET}$ Valid to $V_{CC}$ = GND*

## Table 1. Threshold Suffix Guide

| SUFFIX | $V_{CC}$ THRESHOLD FALLING (V) | | |
|---|---|---|---|
| | MIN | TYP | MAX |
| **46** | 4.509 | 4.625 | 4.741 |
| **45** | 4.388 | 4.500 | 4.613 |
| **44** | 4.266 | 4.375 | 4.484 |
| **43** | 4.193 | 4.300 | 4.408 |
| **42** | 4.095 | 4.200 | 4.305 |
| **41** | 3.998 | 4.100 | 4.203 |
| **40** | 3.900 | 4.000 | 4.100 |
| **39** | 3.802 | 3.900 | 3.998 |
| **38** | 3.705 | 3.800 | 3.895 |
| **37** | 3.608 | 3.700 | 3.793 |
| **36** | 3.510 | 3.600 | 3.690 |
| **35** | 3.413 | 3.500 | 3.588 |
| **34** | 3.315 | 3.400 | 3.485 |
| **33** | 3.218 | 3.300 | 3.383 |
| **32** | 3.120 | 3.200 | 3.280 |
| **31** | 2.998 | 3.075 | 3.152 |
| **30** | 2.925 | 3.000 | 3.075 |
| **29** | 2.852 | 2.925 | 2.998 |
| **28** | 2.730 | 2.800 | 2.870 |
| **27** | 2.633 | 2.700 | 2.768 |
| **26** | 2.559 | 2.625 | 2.691 |
| **25** | 2.438 | 2.500 | 2.563 |
| **24** | 2.340 | 2.400 | 2.460 |
| **23** | 2.255 | 2.313 | 2.371 |
| **225** | 2.180 | 2.235 | 2.290 |
| **22** | 2.133 | 2.188 | 2.243 |
| **21** | 2.048 | 2.100 | 2.153 |
| **20** | 1.950 | 2.000 | 2.050 |
| **19** | 1.853 | 1.900 | 1.948 |
| **18** | 1.755 | 1.800 | 1.845 |
| **17** | 1.623 | 1.665 | 1.707 |
| **16** | 1.536 | 1.575 | 1.614 |

## Table 2. Capacitor Selection Guide

<table>
<tr><th>CAPACITANCE (pF)</th><th>$t_{RP}$ (ms)</th><th>$t_{WD}$ (ms)</th><th>$t_{WD}$ x 128 (ms)</th></tr>
<tr><td>39</td><td rowspan="24">Not recommended</td><td colspan="2" rowspan="13">0<br>(no capacitor is connected)</td></tr>
<tr><td>47</td></tr>
<tr><td>56</td></tr>
<tr><td>68</td></tr>
<tr><td>82</td></tr>
<tr><td>100</td></tr>
<tr><td>120</td></tr>
<tr><td>150</td></tr>
<tr><td>180</td></tr>
<tr><td>220</td></tr>
<tr><td>270</td></tr>
<tr><td>330</td></tr>
<tr><td>390</td></tr>
<tr><td>470</td></tr>
<tr><td>560</td><td rowspan="11">Indeterminate<br>(0, 9.6, or 16)</td><td rowspan="11">Indeterminate<br>(0, 1228.8, or 1636)</td></tr>
<tr><td>680</td></tr>
<tr><td>820</td></tr>
<tr><td>1000</td></tr>
<tr><td>1200</td></tr>
<tr><td>1500</td></tr>
<tr><td>1800</td></tr>
<tr><td>2200</td></tr>
<tr><td>2700</td><td>14.18</td><td>16</td><td>1641</td></tr>
<tr><td>3300</td><td>16.99</td><td>16</td><td>1641</td></tr>
<tr><td>3900</td><td>20.1</td><td>22.4</td><td>2460</td></tr>
<tr><td>4700</td><td>24.21</td><td>22.4</td><td>2460</td></tr>
<tr><td>5600</td><td>28.84</td><td>28.8</td><td>3280</td></tr>
<tr><td>6800</td><td>35.00</td><td>35.2</td><td>4099</td></tr>
<tr><td>8200</td><td>42.23</td><td>41.6</td><td>4918</td></tr>
<tr><td>10,000</td><td>51.5</td><td>54.4</td><td>6556</td></tr>
<tr><td>12,000</td><td>61.8</td><td>60.8</td><td>7376</td></tr>
<tr><td>15,000</td><td>77.25</td><td>80</td><td>9833</td></tr>
<tr><td>18,000</td><td>92.7</td><td>92.8</td><td>11,472</td></tr>
</table>

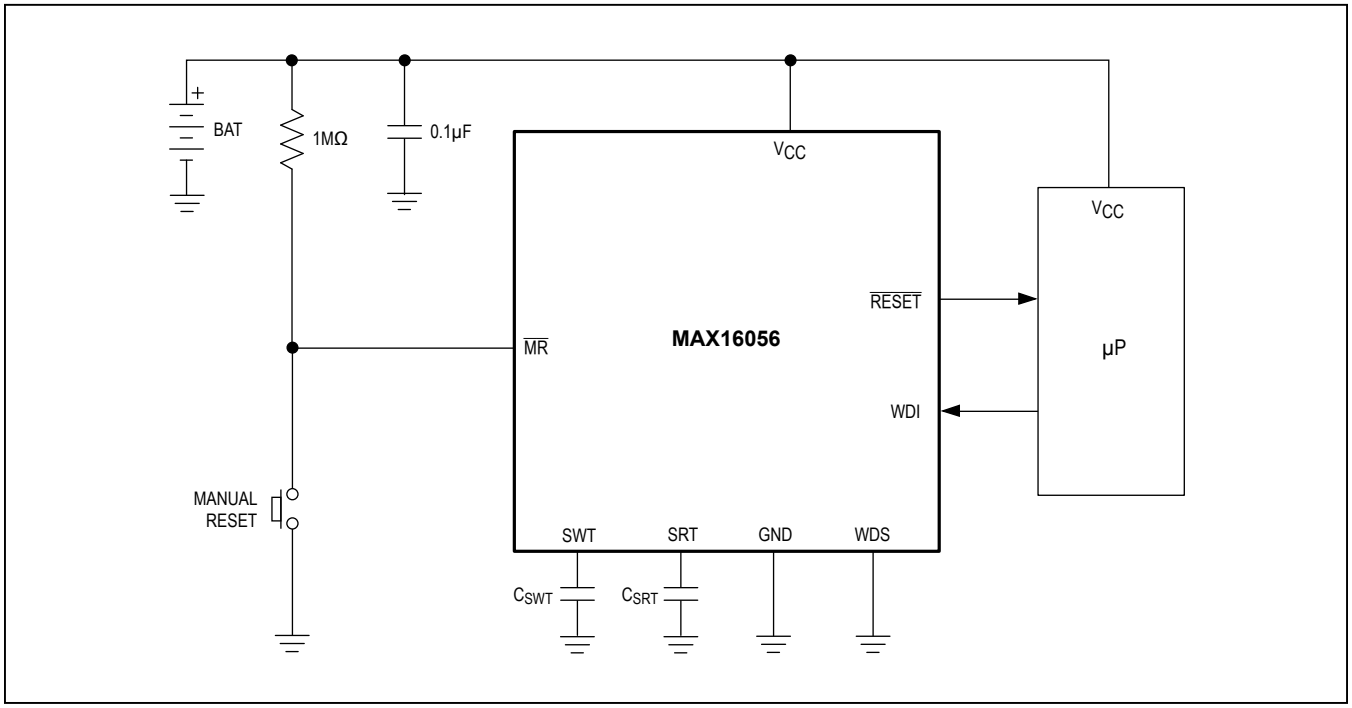
## Table 2. Capacitor Selection Guide (continued)

| CAPACITANCE (pF) | $t_{RP}$ (ms) | $t_{WD}$ (ms) | $t_{WD}$ x 128 (ms) |
|---|---|---|---|
| 22,000 | 113.3 | 112 | 13,929 |
| 27,000 | 139.05 | 137.6 | 17,206 |
| 33,000 | 169.95 | 169.6 | 21,302 |
| 39,000 | 200.85 | 201.6 | 25,398 |
| 47,000 | 242.05 | 240 | 30,313 |
| 56,000 | 288.4 | 291.2 | 36,867 |
| 68,000 | 350.2 | 348.8 | 44,240 |
| 82,000 | 422.3 | 419.2 | 53,251 |
| 100,000 | 515 | 515.2 | 65,539 |
| 120,000 | 618 | 617.6 | 78,646 |
| 150,000 | 772.5 | 771.2 | 98,307 |
| 180,000 | 927 | 924.8 | 117,968 |
| 220,000 | 1133 | 1129.6 | 144,182 |
| 270,000 | 1390.5 | 1392 | 177,769 |
| 330,000 | 1699.5 | 1699.2 | 217,091 |
| 390,000 | 2008.5 | 2006.4 | 256,412 |
| 470,000 | 2420.5 | 2416 | 308,841 |
| 680,000 | 3502 | Indeterminate (may be infinite and watchdog is disabled) | |
| 820,000 | 4223 | | |
| 1,000,000 | 5150 | | |
| 1,500,000 | 7725 | | |
| 2,200,000 | 11,330 | | |
| 3,300,000 | 16,995 | Infinite (watchdog is disabled) | |
| 4,700,000 | 24,205 | | |

## Table 3. Standard Versions

| PART | TOP MARK |
|---|---|
| MAX16056ATA17+ | BKZ |
| MAX16056ATA23+ | BLA |
| MAX16056ATA26+ | BLB |
| MAX16056ATA29+ | BLC |
| MAX16056ATA31+ | BLD |
| MAX16056ATA46+ | BLE |
| MAX16057ATT17+ | ATQ |
| MAX16057ATT23+ | ATR |
| MAX16057ATT26+ | ATS |
| MAX16057ATT29+ | ATT |
| MAX16057ATT31+ | ATU |
| MAX16057ATT46+ | ATV |
| MAX16058ATA16+ | BLF |
| MAX16058ATA22+ | BLG |
| MAX16058ATA26+ | BLH |
| MAX16058ATA29+ | BLI |
| MAX16058ATA31+ | BLJ |
| MAX16058ATA44+ | BLK |
| MAX16059ATT16+ | ATW |
| MAX16059ATT22+ | ATX |
| MAX16059ATT26+ | ATY |
| MAX16059ATT29+ | ATZ |
| MAX16059ATT31+ | AUA |
| MAX16059ATT44+ | AUB |

## Typical Operating Circuit




## Chip Information

PROCESS: BiCMOS

## Ordering Information

| PART | PIN-PACKAGE | RESET OUTPUT | WATCH-DOG TIMER |
|---|---|---|---|
| **MAX16056**ATA_ _+T | 8 TDFN-EP* | Push-Pull | Yes |
| **MAX16057**ATT_ _+T | 6 TDFN-EP* | Push-Pull | No |
| **MAX16058**ATA_ _+T | 8 TDFN-EP* | Open-Drain | Yes |
| **MAX16059**ATT_ _+T | 6 TDFN-EP* | Open-Drain | No |

***Note:*** *All devices are specified over the -40°C to +125°C operating temperature range.*
*+Denotes a lead(Pb)-free/RoHS-compliant package.*
*T = Tape and reel.*
**EP = Exposed pad.*
"_ _" *represents the two number suffix needed when ordering the reset threshold voltage value (see Table 1).*
*Standard versions and their package top marks are shown in Table 3 at the end of data sheet.*

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 6 TDFN-EP | T633-2 | 21-0137 | 90-0058 |
| 8 TDFN-EP | T833-2 | 21-0137 | 90-0059 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/09 | Initial release | — |
| 1 | 6/10 | Updated *Absolute Maximum Ratings*, *Electrical Characteristics*, and Table 3. | 2, 3, 15 |
| 2 | 4/13 | Removed Automotive Infotainment from *Applications* sections | 1 |
| 3 | 5/14 | Changed top mark in Table 3 for MAX16057ATT31+ and MAX16057ATT46+ | 15 |
| 4 | 4/15 | Revised *Benefits and Features* section | 1 |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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