DUAL MULTIPLEXED LVDS REPEATERS

FEATURES

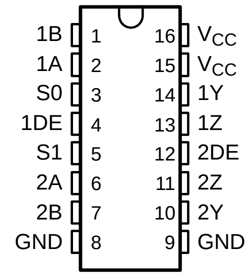
- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard
- Designed for Clock Rates up to 200 MHz (400 Mbps)
- Designed for Data Rates up to 250 Mbps
- Pin Compatible With SN65LVDS122 and SN65LVDT122, 1.5 Gbps 2x2 Crosspoint Switch From TI
- ESD Protection Exceeds 12 kV on Bus Pins
- Operates From a Single 3.3-V Supply
- Low-Voltage Differential Signaling With Output Voltages of 350 mV Into:
  - – 100-Ω Load (SN65LVDS22)
  - – 50-Ω Load (SN65LVDM22)
- Propagation Delay Time; 4 ns Typ
- Power Dissipation at 400 Mbps of 150 mW
- Bus Pins Are High Impedance When Disabled or With V_{CC} Less Than 1.5 V
- LVTTL Levels Are 5 V Tolerant
- Open-Circuit Fail Safe Receiver

DESCRIPTION

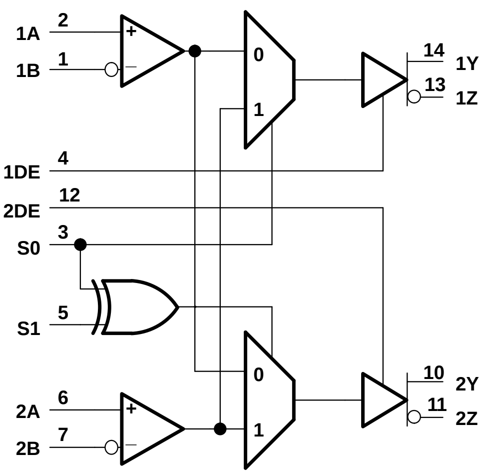
The SN65LVDS22 and SN65LVDM22 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The receiver outputs can be switched to either or both drivers through the multiplexer control signals S0 and S1. This allows the flexibility to perform splitter or signal routing functions with a single device.

The TIA/EIA-644 standard compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 100 mV signals with up to 1 V of ground potential difference between a transmitter and receiver. The SN65LVDM22 doubles the output drive current to achieve LVDS levels with a 50-Ω load.

SN65LVDS22D and SN65LVDS22PW (Marked as LVDS22)
SN65LVDM22D and SN65LVDM22PW (Marked as LVDM22)
(TOP VIEW)



logic diagram (positive logic)



MUX TRUTH TABLE

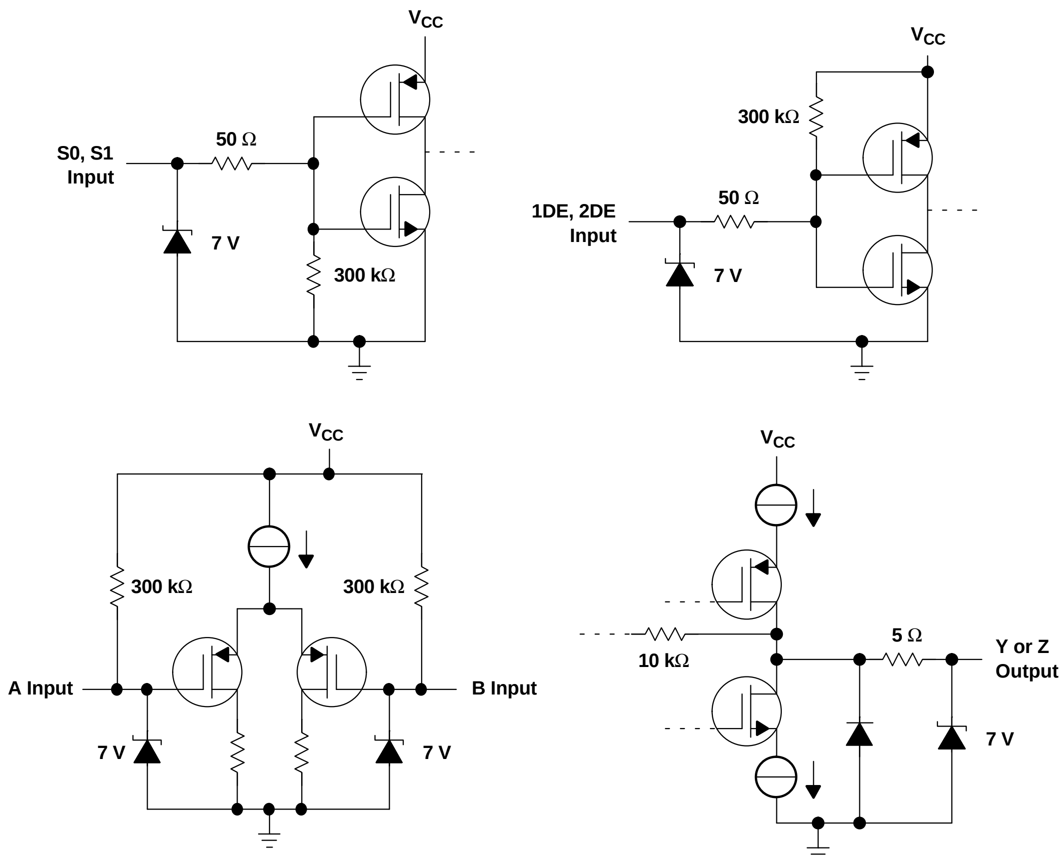
INPUT		OUTPUT		FUNCTION
S1	S0	1Y/1Z	2Y/2Z	
0	0	1A/1B	1A/1B	Splitter
0	1	2A/2B	2A/2B	Splitter
1	0	1A/1B	2A/2B	Router
1	1	2A/2B	1A/1B	Router

The intended application of these devices and signaling technique is for both point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The SN65LVDS22 and SN65LVDM22 are characterized for operation from –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage range, V_{CC} (see Note (2))		–0.5 V to 4 V
Voltage range	(DE, S0, S1)	–0.5 V to 6 V
	(Y, Z, A, and B)	–0.5 V to 4 V
Electrostatic discharge	A, B, Y, Z and GND (see Note (3))	Class 3, A:12 kV, B:600 V
	All pins	Class 3, A:5 kV, B:500 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

TEXAS INSTRUMENTS
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DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR[(1)] ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	1110 mW	8.9 mW/°C	577 mW
PW	839 mW	6.7 mW/°C	437 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	S0, S1, 1DE, 2DE	2			V
V_{IL}	Low-level input voltage	S0, S1, 1DE, 2DE			0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage		0.1		0.6	V
V_{IC}	Common-mode input voltage (see Figure 1)		$\frac{\|V_{ID}\|}{2}$		$2.4-\frac{\|V_{ID}\|}{2}$	V
					$V_{CC}-0.8$	V
T_A	Operating free-air temperature		40		85	°C

TIMING REQUIREMENTS

PARAMETER			MIN	NOM	MAX	UNIT
t_{su}	Input to select setup time	See Figure 6		1.6		ns
t_h	Input to select hold time			1		ns
t_{switch}	Select to switch output			3.2	5	ns

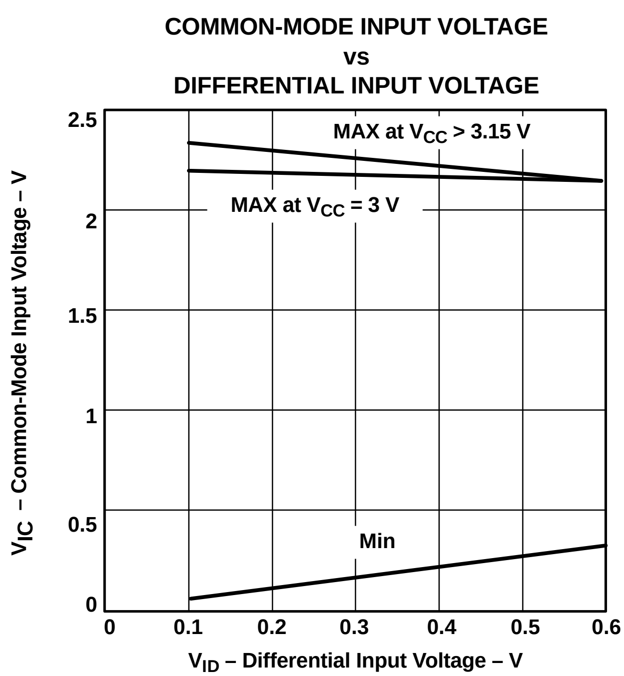


Figure 1. Common-Mode Input Voltage vs Differential Input Voltage

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold				100	mV
V_{IT-}	Negative-going differential input voltage threshold		100			mV
I_I	Input current (A or B inputs)	V_I = 0 V	2		20	μA
		V_I = 2.4 V	1.2			
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0 V			20	μA

RECEIVER/DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OD}	Differential output voltage magnitude		R_L = 100 Ω ('LVDS22), R_L = 50 Ω ('LVDM22)	See Figure 2	247	340	454	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states				–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage			See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				–50	3	50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage						150	mV
I_{CC}	Supply current		No Load			8	12	mA
			R_L = 100 Ω ('LVDS22)			13	20	
			R_L = 50 Ω ('LVDM22)			21	27	
			Disabled			3	6	
I_{IH}	High-level input current	DE	V_{IH} = 5 V				–10	μA
		S0, S1					20	
I_{IL}	Low-level input current	DE	V_{IL} = 0.8 V				–10	μA
		S0, S1					10	
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ} = 0 V, V_{OD} = 0 V ('LVDS22)				–10	mA
							–10	
			V_{OY} or V_{OZ} = 0 V, V_{OD} = 0 V ('LVDM22)				–10	
							–10	
I_{OZ}	High-impedance output current		V_{OD} = 600 mV			0.015	±1	μA
			V_O = 0 V or V_{CC}			0.015	±1	
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0 V,	V_O = 3.6 V		0.015	±1	μA
C_{IN}	Input capacitance					3		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

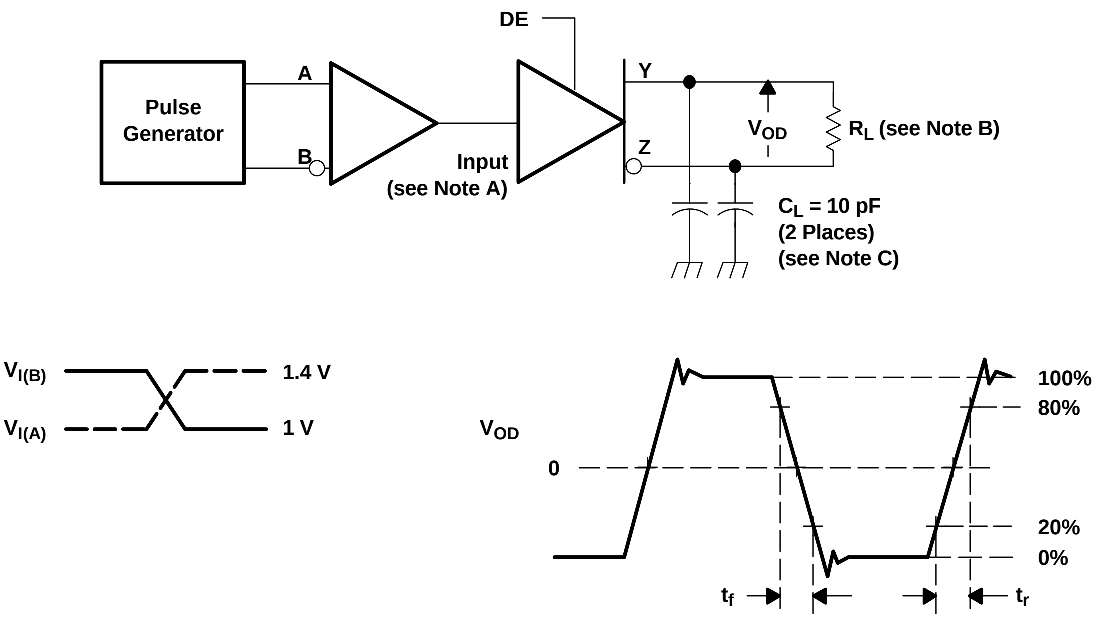
DIFFERENTIAL RECEIVER TO DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{PLH}	Differential propagation delay time, low-to-high		C_L = 10 pF, See Figure 4		4	6	ns
t_{PHL}	Differential propagation delay time, high-to-low				4	6	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL}$ - $t_{PLH}\|$)				0.2		ns
t_r	Transition time, low-to-high	SN65LVDS22			1	1.5	ns
t_r	Transition time, low-to-high	SN65LVDM22			0.8	1.3	ns
t_f	Transition time, high-to-low	SN65LVDS22			1	1.5	ns
t_f	Transition time, high-to-low	SN65LVDM22			0.8	1.3	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output		See Figure 5		4	10	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				5	10	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output				5	10	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output				6	10	ns
$t_{PHL\_R1\_Dx}$	Channel-to-channel skew, receiver to driver[2]				0.2		ns
$t_{PLH\_R1\_Dx}$					0.2		
$t_{PHL\_R2\_Dx}$					0.2		
$t_{PLH\_R2\_Dx}$					0.2		
f_{max}	Maximum operating frequency		All channels switching		200		MHz

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) These parametric values are measured over supply voltage and temperature ranges recommended for the device.

PARAMETER MEASUREMENT INFORMATION



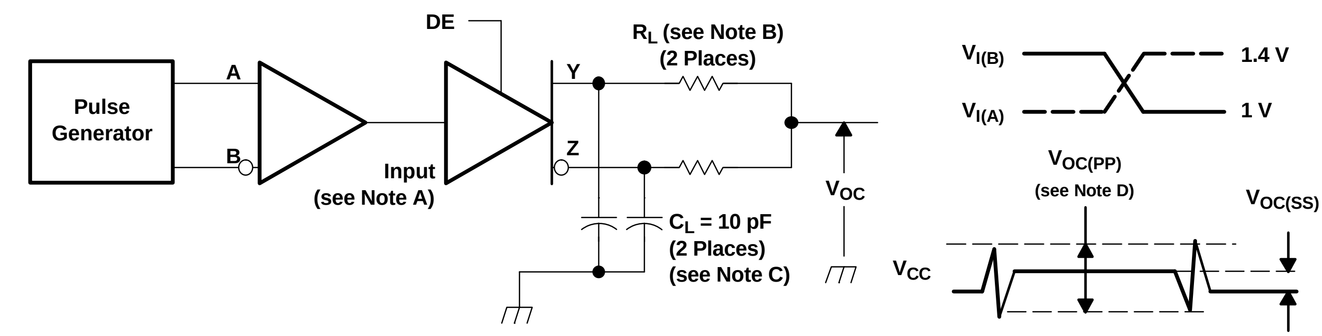
A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ±0.2 ns.

B. R_L = 100 Ω or 50 Ω ±1%

C. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 2. Test Circuit and Voltage Definitions for the Differential Output Signal

PARAMETER MEASUREMENT INFORMATION (continued)



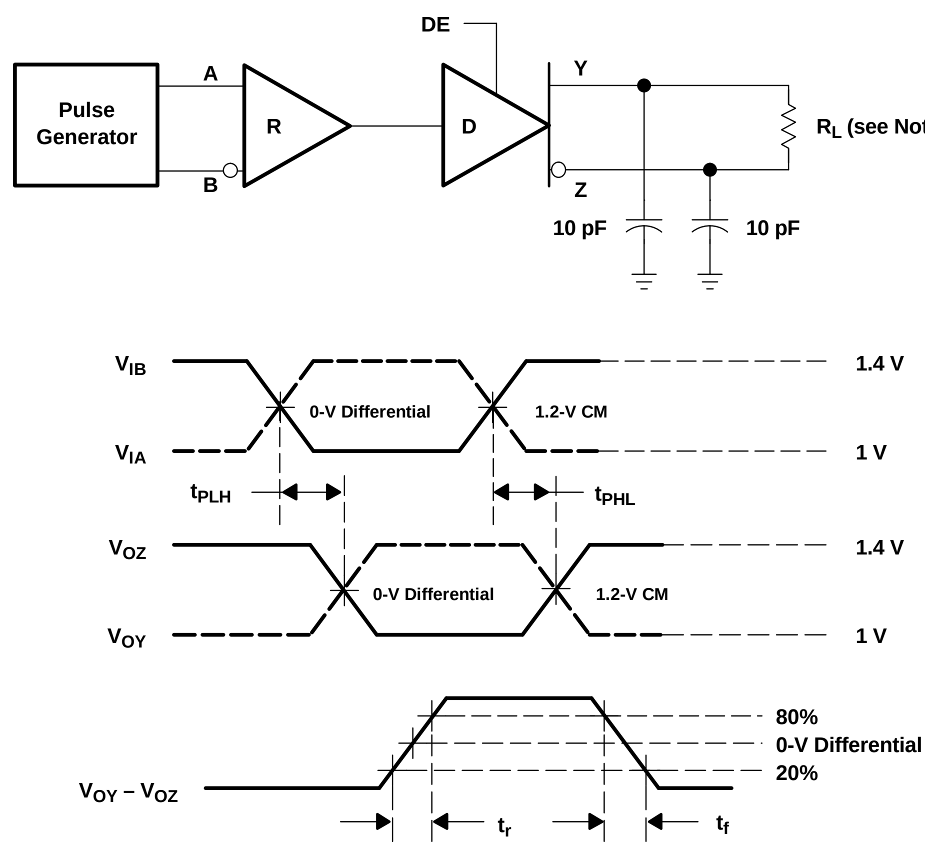
A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ±0.2 ns.

B. R_L = 100 Ω or 50 Ω ±1%

C. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

D. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

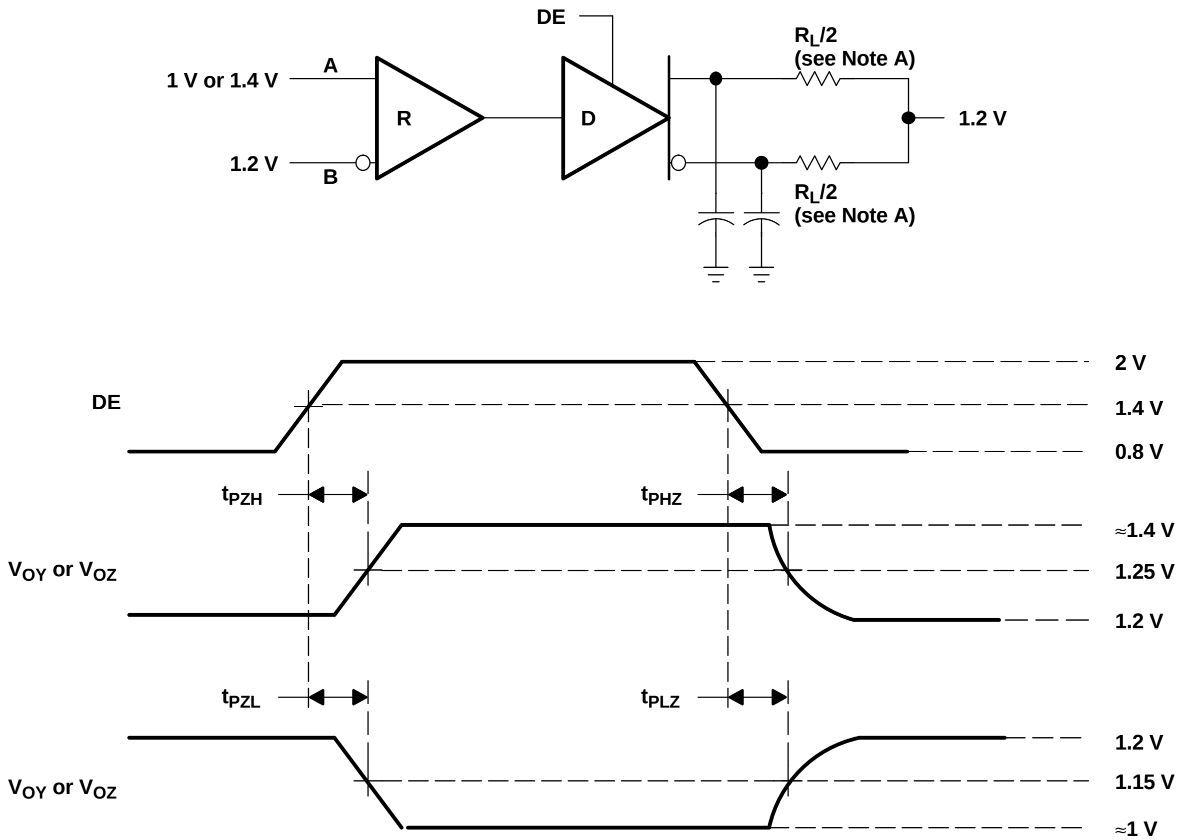


A. R_L = 100 Ω or 50 Ω ±1%

B. All input pulses are supplied by a generator having the following characteristics: pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ±0.2 ns.

Figure 4. Differential Receiver to Driver Propagation Delay and Driver Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

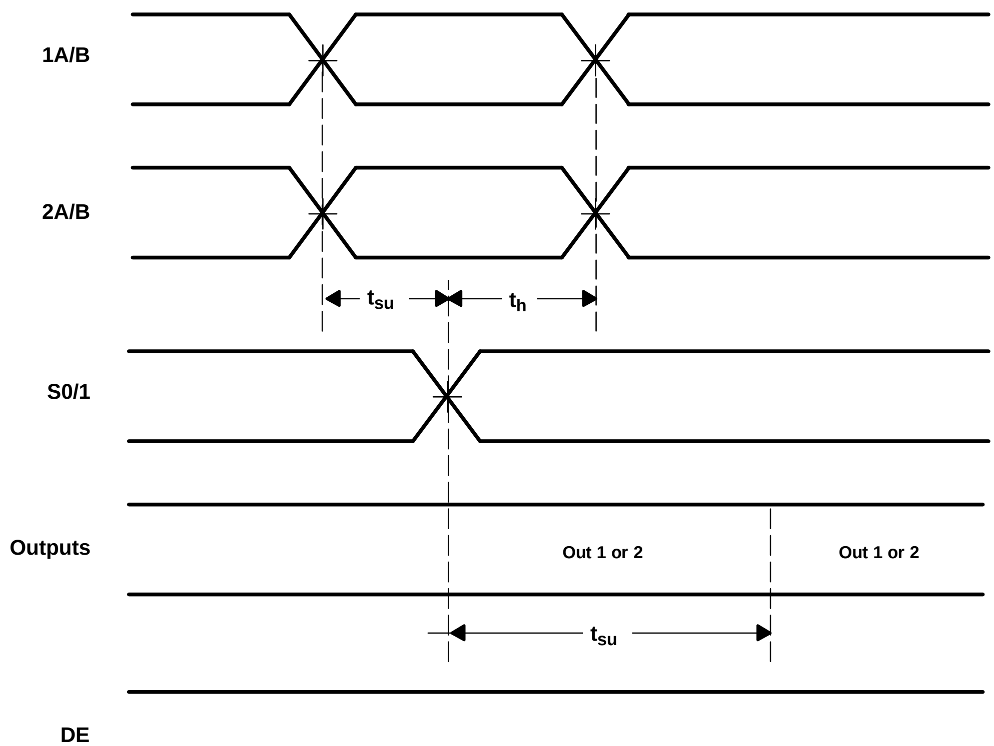


A. R_L = 100 Ω or 50 Ω ±1%

B. All input pulses are supplied by a generator having the following characteristics: pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns.

Figure 5. Enable and Disable Timing Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: t_{su} and t_h times specify that data must be in a stable state before and after MUX control switches.

Figure 6. Input-to-Select for Both Rising and Falling Edge Setup and Hold Times

TYPICAL CHARACTERISTICS

SN65LVDS22
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

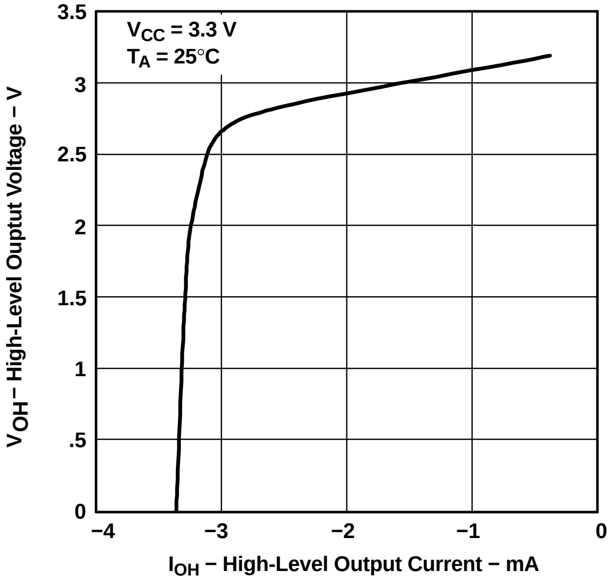


Figure 7.

SN65LVDS22
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

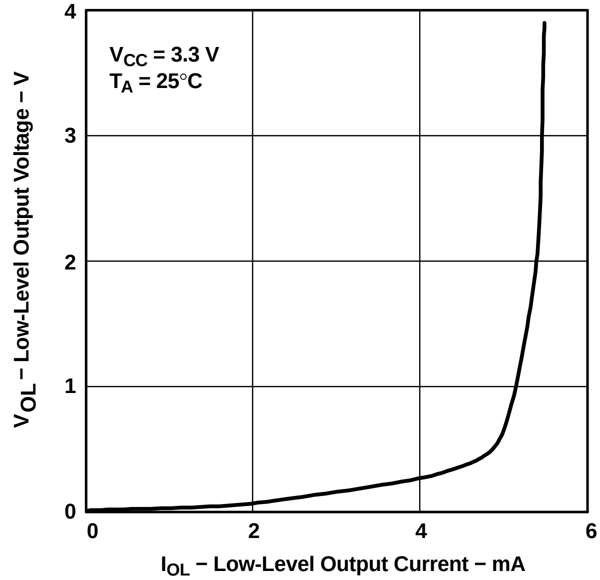


Figure 8.

SN65LVDM22
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

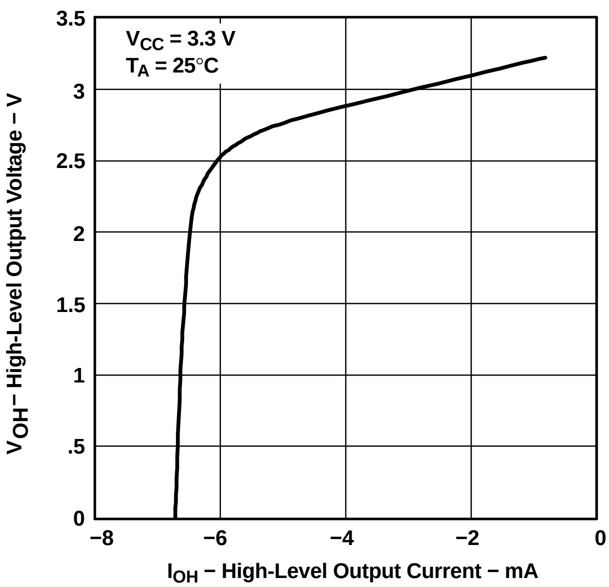


Figure 9.

SN65LVDM22
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

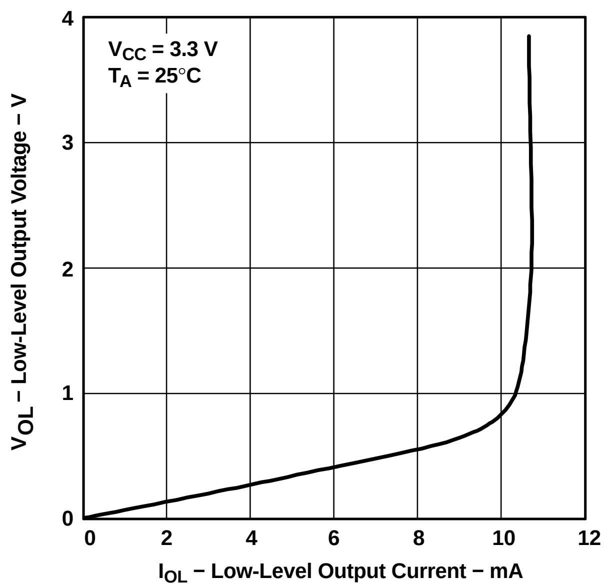


Figure 10.

APPLICATION INFORMATION

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. However, TI's LVDS receiver is different in how it handles the open-input circuit situation.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 11. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

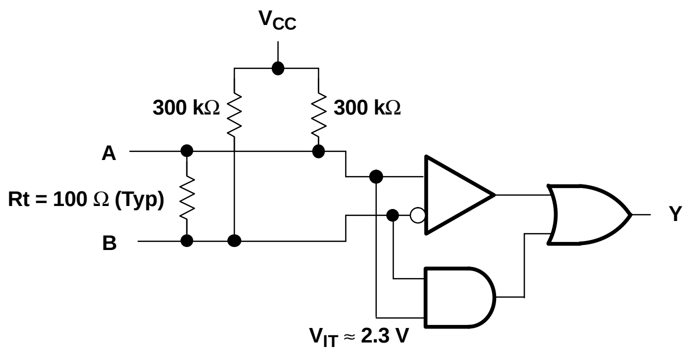


Figure 11. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in Figure 11. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDM22D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDM22DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDM22PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDM22PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS22D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS22DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS22DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS22DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS22PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS22PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS22PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS22PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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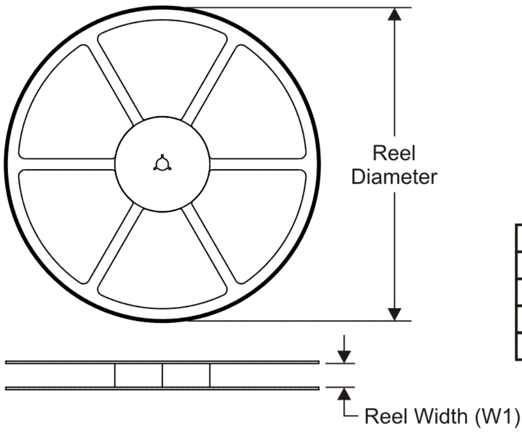
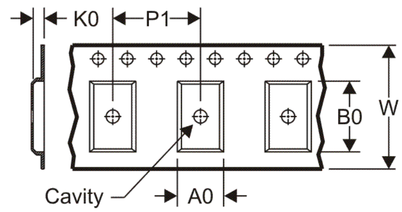
TAPE AND REEL INFORMATION

REEL DIMENSIONS

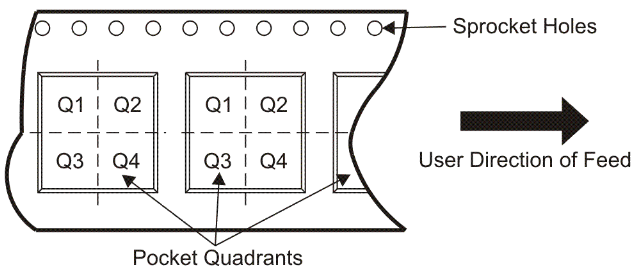


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

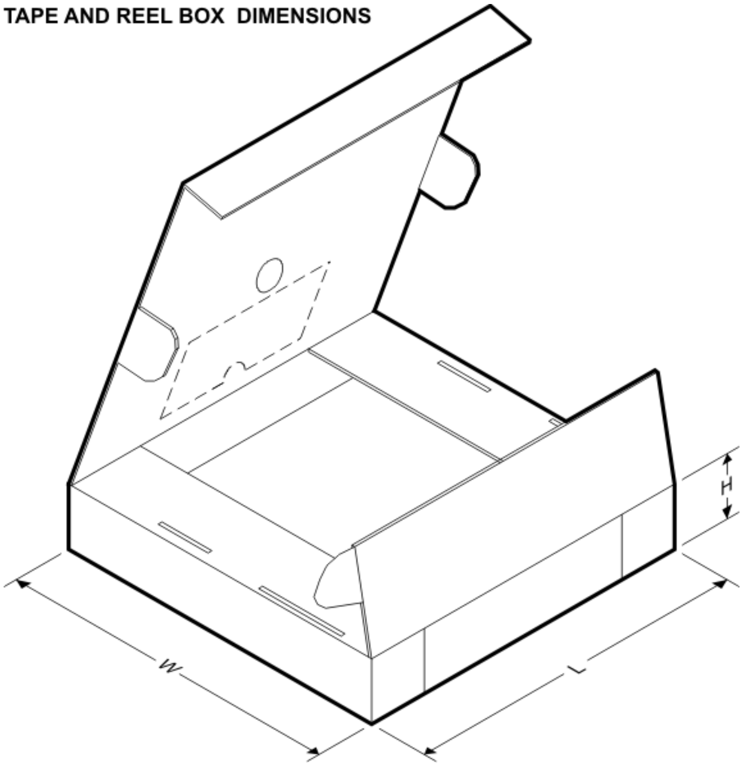
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS22DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS22PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS22DR	SOIC	D	16	2500	346.0	346.0	33.0
SN65LVDS22PWR	TSSOP	PW	16	2000	346.0	346.0	29.0