DS25BR150 3.125 Gbps LVDS Buffer

Check for Samples: DS25BR150

FEATURES

- **DC - 3.125 Gbps Low Jitter, High Noise Immunity, Low Power Operation**
- **On-Chip 100 Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count and Minimizes Board Space**
- **7 kV ESD on LVDS I/O Pins Protects Adjoining Components**
- **Small 3 mm x 3 mm WSON-8 Space Saving Package**

APPLICATIONS

- **Clock or Data Buffering / Repeating**
- **OC-48 / STM-16 Clock or Data Buffering / Repeating**
- **InfiniBand**
- **FireWire**

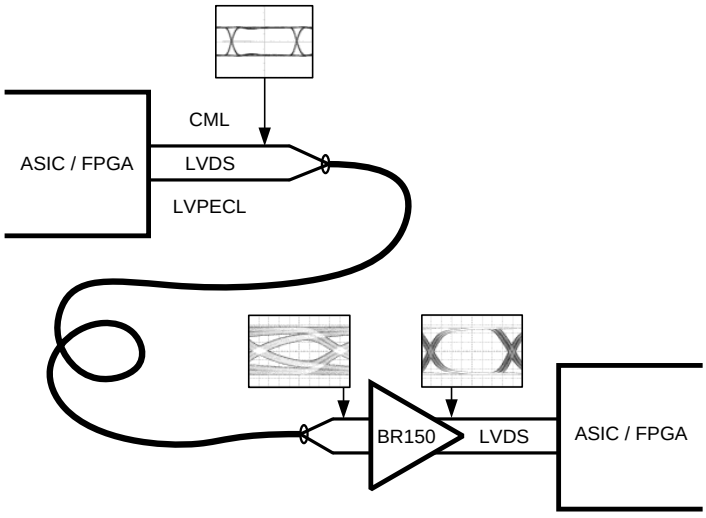
DESCRIPTION

The DS25BR150 is a single channel 3.125 Gbps LVDS buffer optimized for high-speed signal transmission over printed circuit boards and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

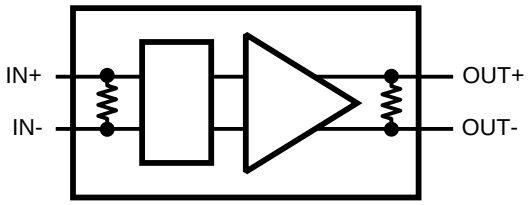
The DS25BR150 is a buffer/repeater with very low power consumption. Other LVDS devices with similar IO characteristics and with signal conditioning features include the following products. The DS25BR110 features four levels of equalization for use as an optimized receiver device, the DS25BR120 features four levels of pre-emphasis for use as an optimized driver device, and the DS25BR100 features both pre-emphasis and equalization for use as an optimized repeater device.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. The differential inputs and outputs are internally terminated with a 100Ω resistor to lower device input and output return losses, reduce component count, and further minimize board space.

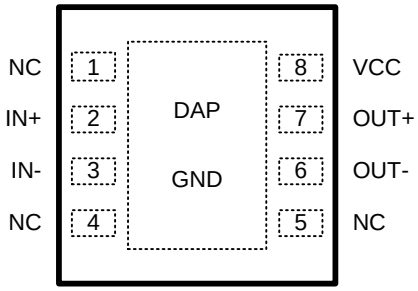
Typical Application



Block Diagram



Pin Diagram



WSON Package

PIN DESCRIPTION

Pin Name	Pin Name	Pin Type	Pin Description
NC	1	NA	"NO CONNECT" pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
NC	4	NA	"NO CONNECT" pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})		−0.3V to +4V
LVDS Input Voltage (IN+, IN−)		−0.3V to +4V
Differential Input Voltage |VID|		1V
LVDS Output Voltage (OUT+, OUT−)		−0.3V to (V_{CC} + 0.3V)
LVDS Differential Output Voltage ((OUT+) - (OUT−))		0V to 1V
LVDS Output Short Circuit Current Duration		5 ms
Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range	Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	NGQ Package	2.08W
	Derate NGQ Package	16.7 mW/°C above +25°C
Package Thermal Resistance	θ_{JA}	+60.0°C/W
	θ_{JC}	+12.3°C/W
ESD Susceptibility	HBM[3]	≥7 kV
	MM[4]	≥250V
	CDM[5]	≥1250V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current[4]	OUT to GND		-25	-50	mA
		OUT to V_{CC}		7.5	50	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS INPUT DC SPECIFICATIONS (IN+, IN-)						
V_{ID}	Input Differential Voltage		0		1	V
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V or V_{CC}-0.05V		0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input Current	V_{IN} = 3.6V or 0V V_{CC} = 3.6V or 0V		±1	±10	µA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
SUPPLY CURRENT						
I_{CC}	Supply Current			27	35	mA

AC Electrical Characteristics(1)

Over recommended operating supply and temperature ranges unless otherwise specified.(2)(3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)							
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω			370	520	ps
t_{PLHD}	Differential Propagation Delay Low to High				355	520	ps
t_{SKD1}	Pulse Skew $\|t_{PLHD} - t_{PHLD}\|$(4)				15	100	ps
t_{SKD2}	Part to Part Skew(5)				45	160	ps
t_{LHT}	Rise Time	R_L = 100Ω			80	150	ps
t_{HLT}	Fall Time				80	150	ps
JITTER PERFORMANCE (Figure 5)							
t_{DJ1}	Deterministic Jitter (Peak-to-Peak Value)(6)	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		11	33	ps
t_{DJ2}			3.125 Gbps		15	41	ps
t_{RJ1}	Random Jitter (RMS Value)(7)	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	1.25 GHz		0.5	1	ps
t_{RJ2}			1.5625 GHz		0.5	1	ps
t_{TJ1}	Total Jitter (Peak to Peak Value)(8)	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ)	2.5 Gbps		0.04	0.11	UI_{P-P}
t_{TJ2}			3.125 Gbps		0.07	0.15	UI_{P-P}

(1) Specification is ensured by characterization and is not tested in production.
(2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2}, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(6) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(7) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
(8) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC TEST CIRCUITS

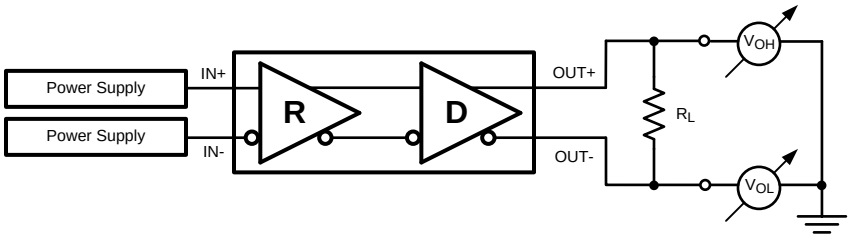


Figure 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

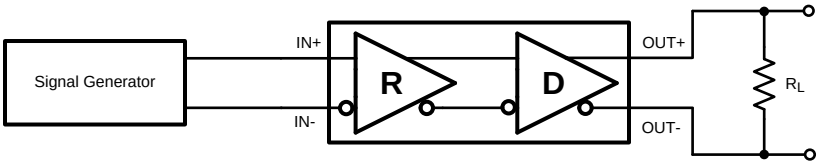


Figure 2. Differential Driver AC Test Circuit

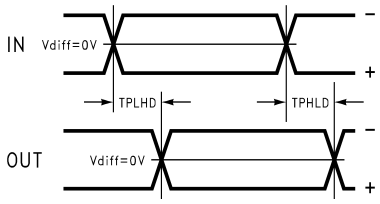


Figure 3. Propagation Delay Timing Diagram

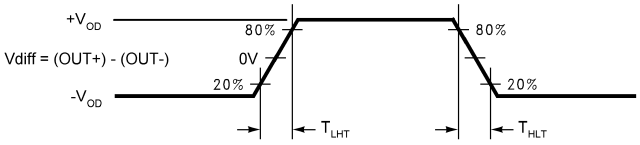


Figure 4. LVDS Output Transition Times

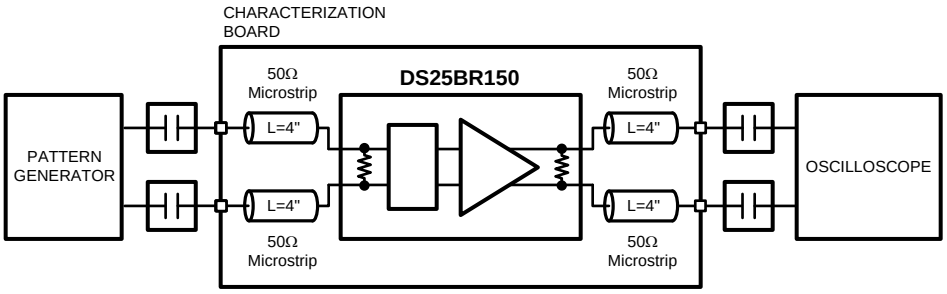


Figure 5. Jitter Measurements Test Circuit

Device Operation

INPUT INTERFACING

The DS25BR150 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR150 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR150 inputs are internally terminated with a 100Ω resistor.

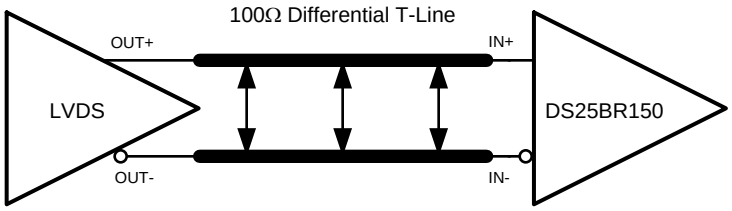


Figure 6. Typical LVDS Driver DC-Coupled Interface to DS25BR150 Input

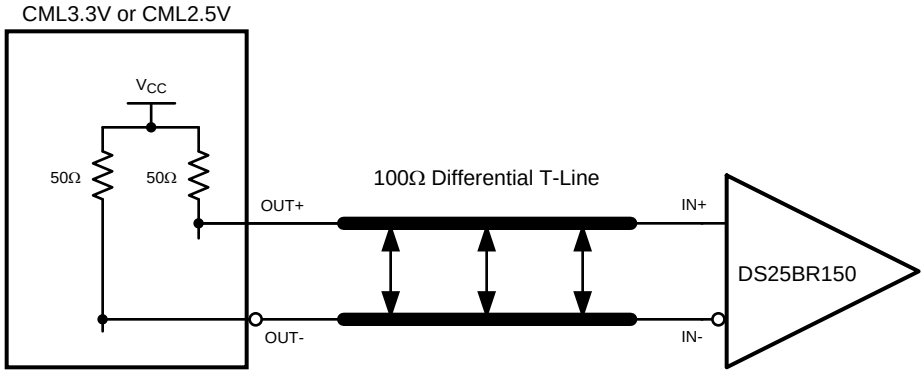


Figure 7. Typical CML Driver DC-Coupled Interface to DS25BR150 Input

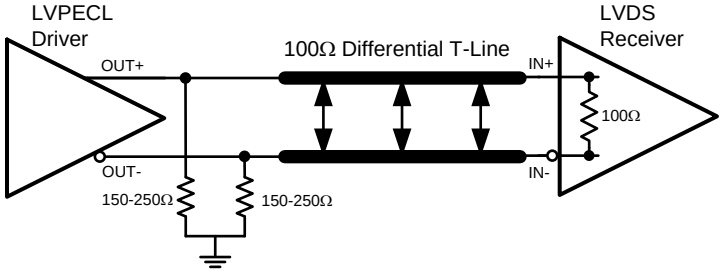


Figure 8. Typical LVPECL Driver DC-Coupled Interface to DS25BR150 Input

OUTPUT INTERFACING

The DS25BR150 outputs signals are compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's data sheet prior to implementing the suggested interface implementation.

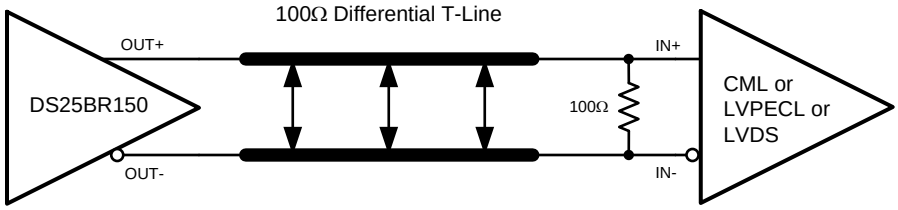


Figure 9. Typical DS25BR150 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance Characteristics

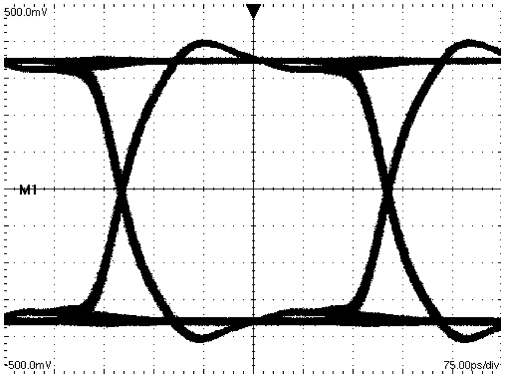


Figure 10. A 2.5 Gbps NRZ PRBS-7 Output Eye Diagram V:100 mV / DIV, H:75 ps / DIV

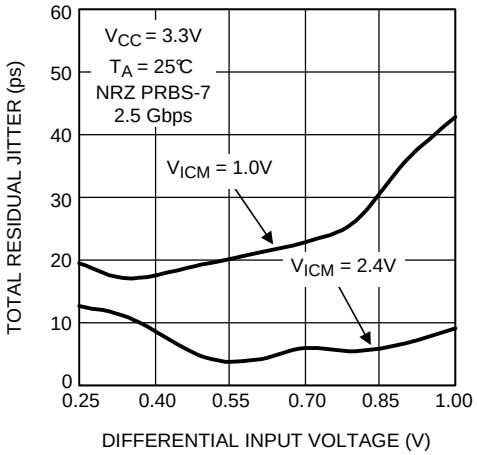


Figure 11. Total Jitter as a Function of Input Amplitude

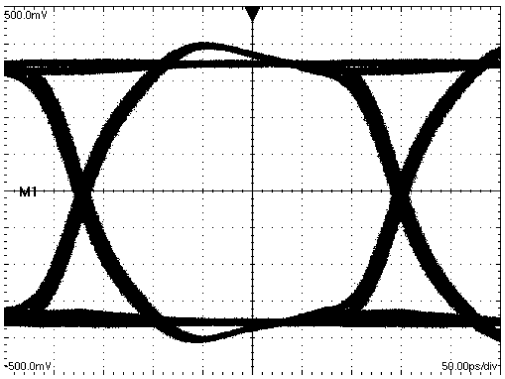


Figure 12. A 3.125 Gbps NRZ PRBS-7 Output Eye Diagram V:100 mV / DIV, H:50 ps / DIV

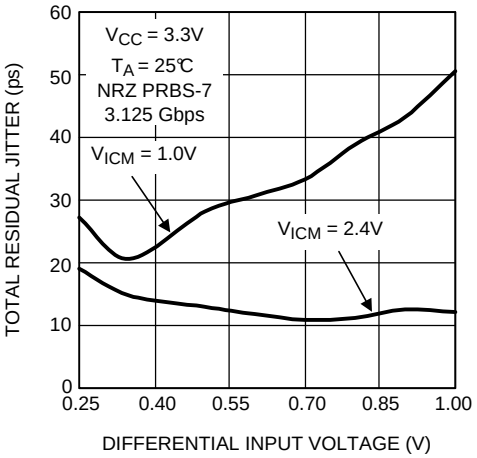


Figure 13. Total Jitter as a Function of Input Amplitude

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS25BR150TSD/NOPB	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	2R150
DS25BR150TSD/NOPB.A	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	2R150

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

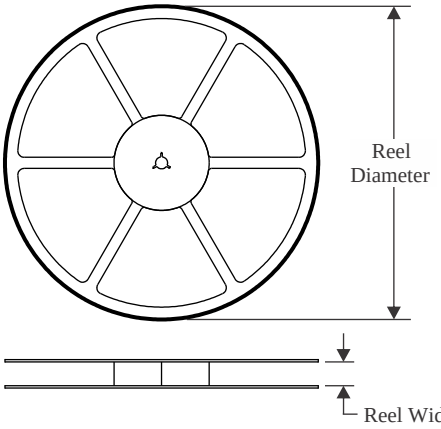
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

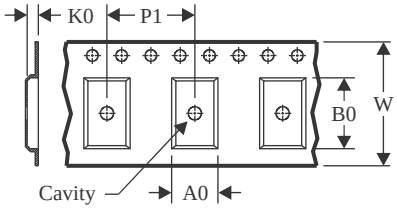
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

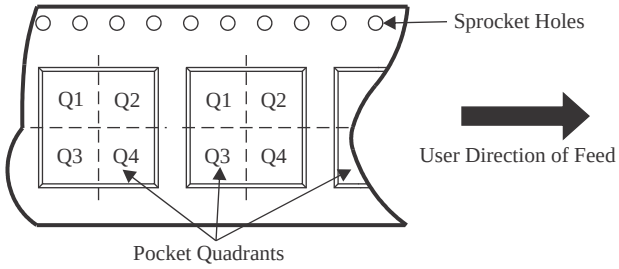


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

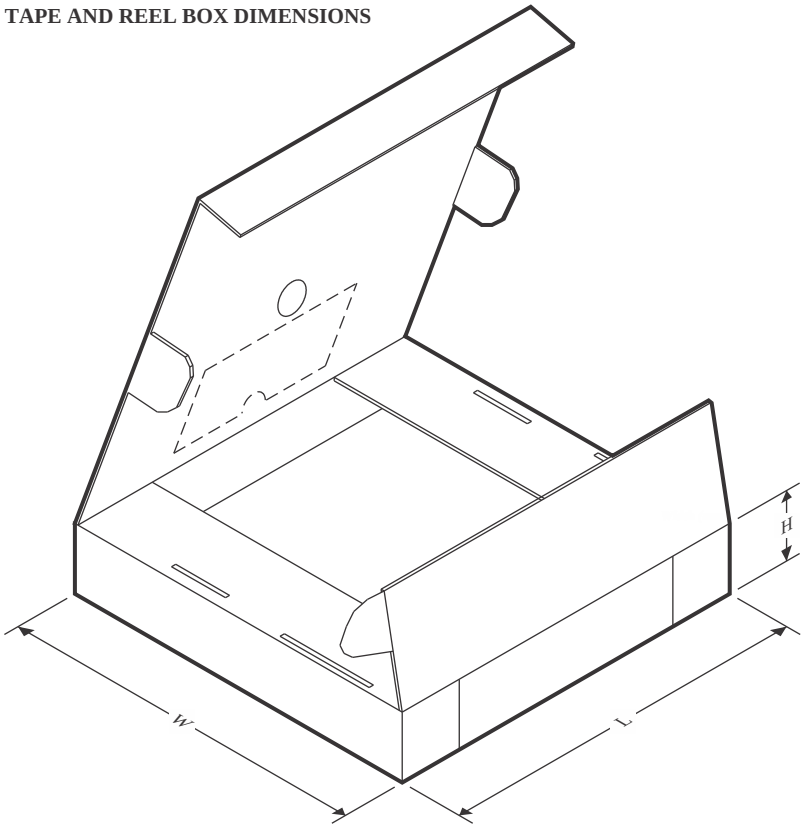
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25BR150TSD/NOPB	WSON	NGQ	8	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

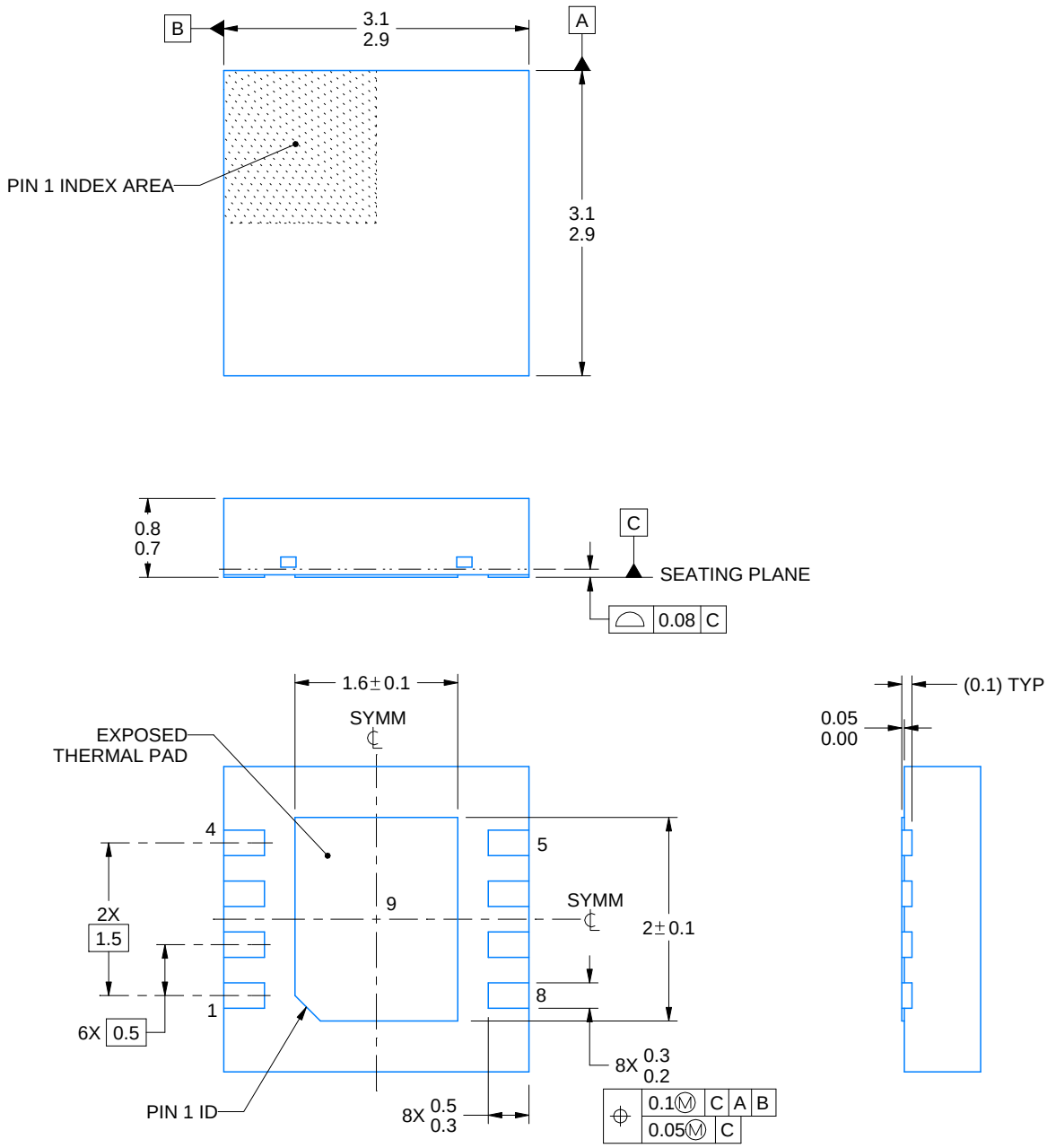
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25BR150TSD/NOPB	WSON	NGQ	8	1000	208.0	191.0	35.0

PACKAGE OUTLINE

NGQ0008A

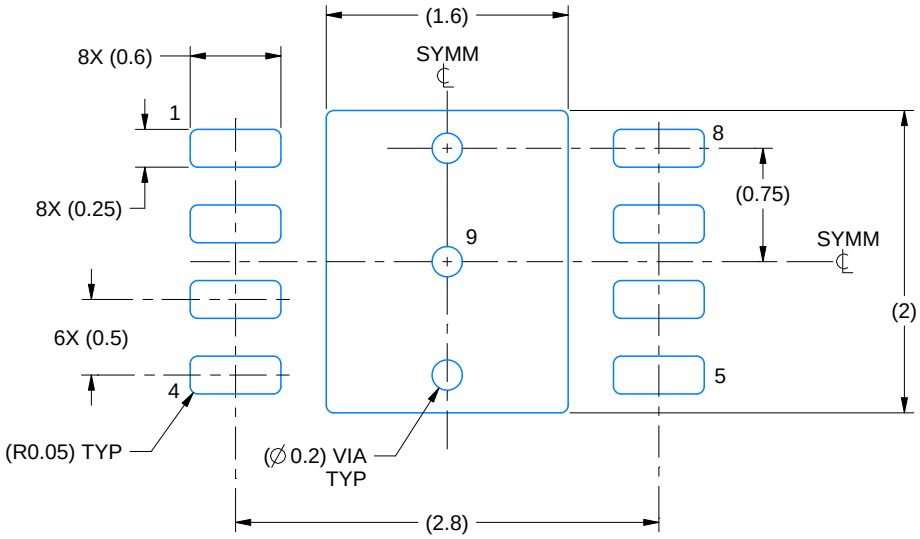
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

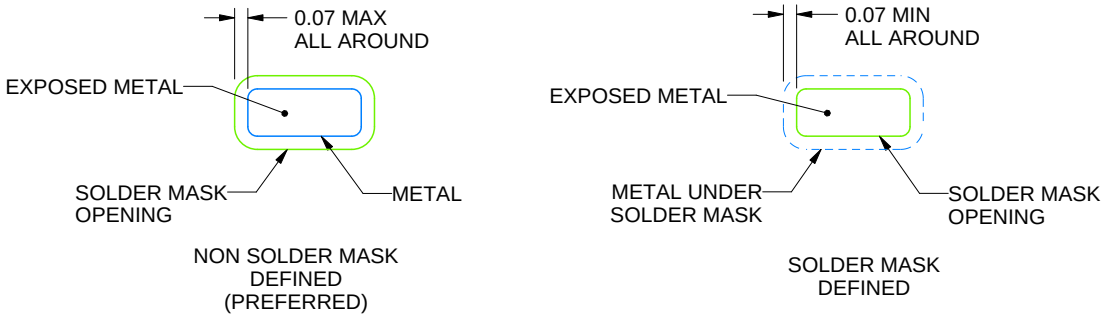


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

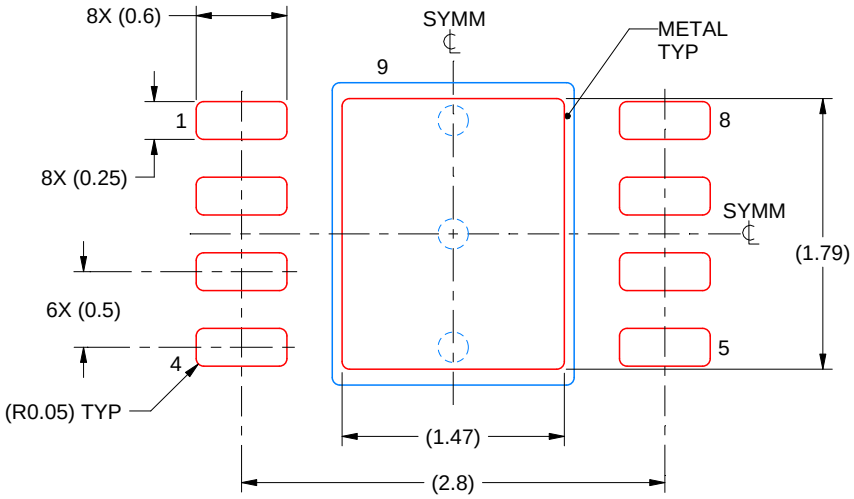


SOLDER MASK DETAILS

4214922/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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