DDR SDRAM SODIMM

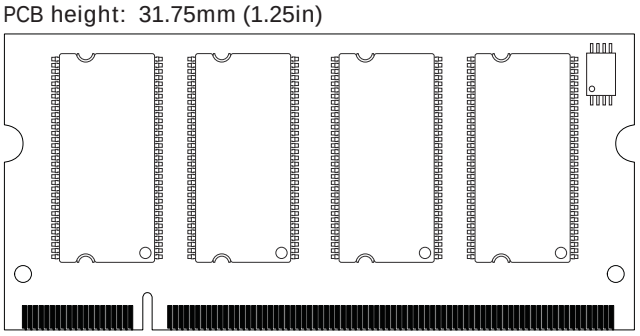
MT8VDDT3264HD – 256MB[1]
MT8VDDT6464HD – 512MB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 200-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2100, PC2700, or PC3200
- 256MB (32 Meg x 64), 512MB (64 Meg x 64)
- $V_{DD} = V_{DD}Q = +2.5V$
  (-40B: $V_{DD} = V_{DD}Q = +2.6V$)
- $V_{DDSPD} = +2.3V$ to $+3.6V$
- 2.5V I/O (SSTL_2-compatible)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/ received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Selectable burst lengths (BL): 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 7.8125µs maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Dual rank
- Gold edge contacts

Figure 1: 200-Pin SODIMM (MO-224)



Options — Marking

- Operating temperature[2]
  - Commercial ($0°C \le T_A \le +70°C$) — None
  - Industrial ($–40°C \le T_A \le +85°C$) — I
- Package
  - 200-pin DIMM (standard) — G
  - 200-pin DIMM (lead-free) — Y
- Memory clock, speed, CAS latency
  - 5.0ns (200 MHz), 400 MT/s, CL = 3 — -40B
  - 6.0ns (167 MHz), 333 MT/s, CL = 2.5 — -335
  - 7.5ns (133 MHz), 266 MT/s, CL = 2[1] — -26A
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.5[1] — -265

Notes: 1. Not recommended for new designs.
2. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			^tRCD (ns)	^tRP (ns)	^tRC (ns)	Notes
		CL = 3	CL = 2.5	CL = 2				
-40B	PC3200	400	333	266	15	15	55	
-335	PC2700	–	333	266	18	18	60	1
-26A	PC2100	–	266	266	20	20	65	
-265	PC2100	–	266	200	20	20	65	

Notes: 1. The values of ^tRCD and ^tRP for -335 modules show 18ns to align with industry specifications; actual DDR SDRAM device specifications are 15ns.

Table 2: Addressing

Parameter	256MB	512MB
Refresh count	8K	8K
Row address	8K (A0–A12)	8K (A0–A12)
Device bank address	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	256Mb (16 Meg x 16)	512Mb (32 Meg x 16)
Column address	512 (A0–A8)	1K (A0–A9)
Module rank address	2 (S0#, S1#)	2 (S0#, S1#)

Table 3: Part Numbers and Timing Parameters – 256MB

Base device: MT46V16M16,[1] 256Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT8VDDT3264HDG-40B__	256MB	32 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT8VDDT3264HDY-40B__	256MB	32 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT8VDDT3264HDG-335__	256MB	32 Meg x 64	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT8VDDT3264HDY-335__	256MB	32 Meg x 64	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT8VDDT3264HDG-26A__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT8VDDT3264HDG-265__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT8VDDT3264HDY-265__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Table 4: Part Numbers and Timing Parameters – 512MB

Base device: MT46V32M16,[1] 512Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT8VDDT6464HDG-40B__	512MB	64 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT8VDDT6464HDY-40B__	512MB	64 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT8VDDT6464HDG-335__	512MB	64 Meg x 64	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT8VDDT6464HDY-335__	512MB	64 Meg x 64	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT8VDDT6464HDG-265__	512MB	64 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT8VDDT6464HDY-265__	512MB	64 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
   Example: MT8VDDT6464HDY-335F2.

Pin Assignments and Descriptions

Table 5: Pin Assignments

200-Pin SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	VSS	101	A9	151	DQ42
3	VSS	53	DQ19	103	VSS	153	DQ43
5	DQ0	55	DQ24	105	A7	155	VDD
7	DQ1	57	VDD	107	A5	157	VDD
9	VDD	59	DQ25	109	A3	159	VSS
11	DQS0	61	DQS3	111	A1	161	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48
15	VSS	65	DQ26	115	A10	165	DQ49
17	DQ3	67	DQ27	117	BA0	167	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6
21	VDD	71	NC	121	S0#	171	DQ50
23	DQ9	73	NC	123	NC	173	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51
27	VSS	77	NC	127	DQ32	177	DQ56
29	DQ10	79	NC	129	DQ33	179	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57
33	VDD	83	NC	133	DQS4	183	DQS7
35	CK0	85	NC	135	DQ34	185	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58
39	VSS	89	NC	139	DQ35	189	DQ59
41	DQ16	91	NC	141	DQ40	191	VDD
43	DQ17	93	VDD	143	VDD	193	SDA
45	VDD	95	CKE1	145	DQ41	195	SCL
47	DQS2	97	NC	147	DQS5	197	VDDSPD
49	DQ18	99	A12	149	VSS	199	NC

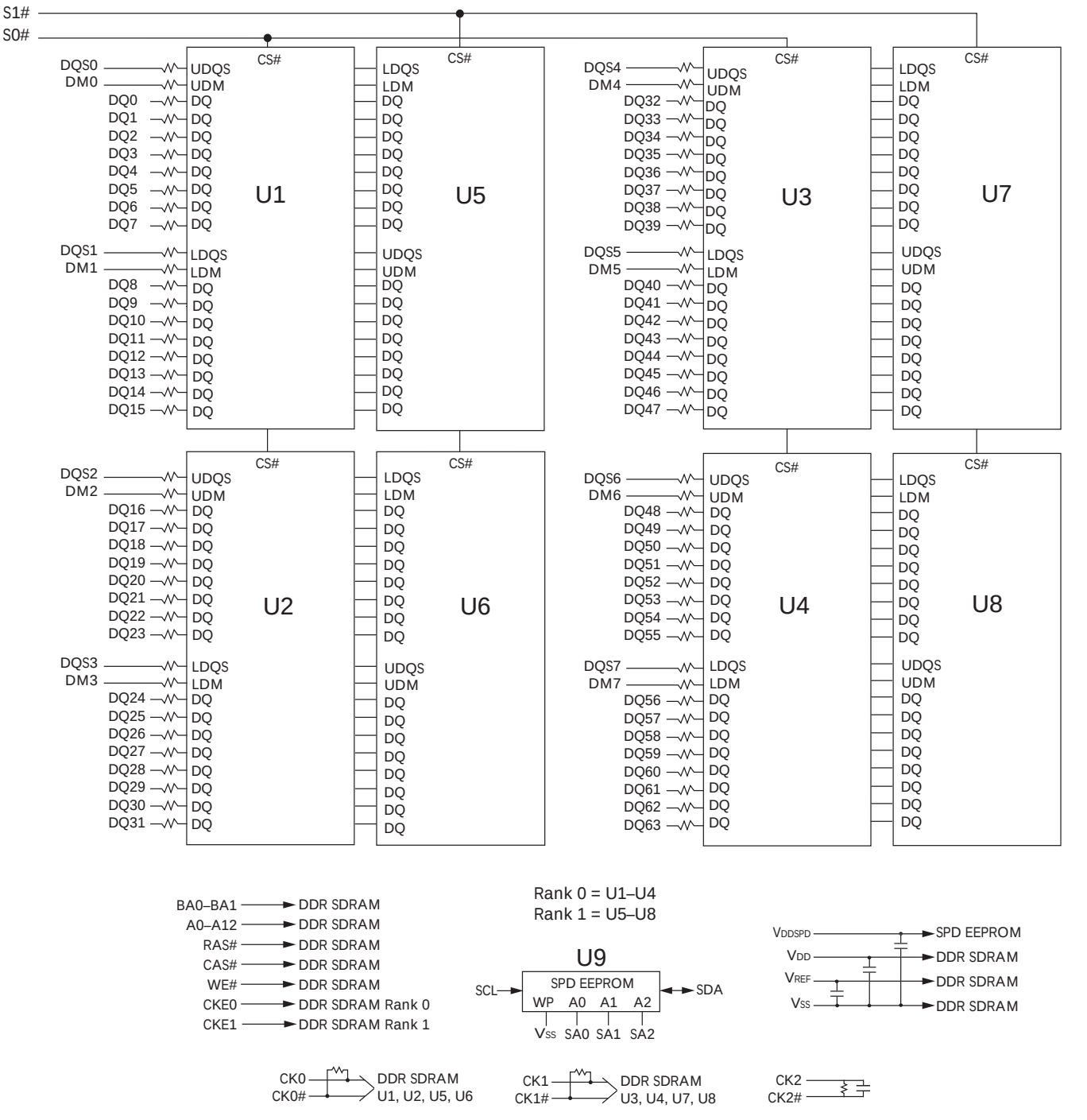
200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	VREF	52	VSS	102	A8	152	DQ46
4	VSS	54	DQ23	104	VSS	154	DQ47
6	DQ4	56	DQ28	106	A6	156	VDD
8	DQ5	58	VDD	108	A4	158	CK1#
10	VDD	60	DQ29	110	A2	160	CK1
12	DM0	62	DM3	112	A0	162	VSS
14	DQ6	64	VSS	114	VDD	164	DQ52
16	VSS	66	DQ30	116	BA1	166	DQ53
18	DQ7	68	DQ31	118	RAS#	168	VDD
20	DQ12	70	VDD	120	CAS#	170	DM6
22	VDD	72	NC	122	S1#	172	DQ54
24	DQ13	74	NC	124	NC	174	VSS
26	DM1	76	VSS	126	VSS	176	DQ55
28	VSS	78	NC	128	DQ36	178	DQ60
30	DQ14	80	NC	130	DQ37	180	VDD
32	DQ15	82	VDD	132	VDD	182	DQ61
34	VDD	84	NC	134	DM4	184	DM7
36	VDD	86	NC	136	DQ38	186	VSS
38	VSS	88	VSS	138	VSS	188	DQ62
40	VSS	90	VSS	140	DQ39	190	DQ63
42	DQ20	92	VDD	142	DQ44	192	VDD
44	DQ21	94	VDD	144	VDD	194	SA0
46	VDD	96	CKE0	146	DQ45	196	SA1
48	DM2	98	NC	148	DM5	198	SA2
50	DQ22	100	A11	150	VSS	200	NC

Table 6: Pin Descriptions

Symbol	Type	Description
A0–A12	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0 and BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
BA0, BA1	Input	**Bank address:** BA0 and BA1 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK0, CK0#, CK1, CK1#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input	**Clock enable:** CKE enables (registered HIGH) and CKE disables (registered LOW) the internal clock, input buffers, and output drivers.
DM0–DM7	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#, S1#	Input	**Chip selects:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** SCL is used to synchronize the presence-detect data transfer to and from the module.
DQ0–DQ63	I/O	**Data input/output:** Data bus.
DQS0–DQS7	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. Used to capture data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
V_{DD}	Supply	**Power supply:** +2.5V ±0.2V (-40B: +2.6V ±0.1V).
V_{DDSPD}	Supply	**Serial EEPROM power supply:** +2.3V to +3.6V.
V_{REF}	Supply	SSTL_2 reference voltage (V_{DD}/2).
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT8VDDT3264HD and MT8VDDT6464HD are high-speed, CMOS, dynamic random access 256MB and 512MB memory modules organized in a x64 configuration. These modules use DDR SDRAM devices with four internal banks.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various DDR SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}		–1.0	+3.6	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+3.2	V
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA	–16	+16	µA
		CK, CK#, S#, CKE	–8	+8	
		DM	–4	+4	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ $V_{DD}Q$; DQ are disabled	DQ, DQS	–10	+10	µA
T_A	DRAM ambient operating temperature[1]	Commercial	0	+70	°C
		Industrial	–40	+85	°C

Notes: 1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades
DDR components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-40B	-5B
-335	-6
-26A	-75Z
-265	-75

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

IDD Specifications

Table 9: IDD Specifications and Conditions – 256MB (Die Revision K)
Values are for the MT46V16M16 DDR SDRAM only and are computed from values specified in the 256Mb (16 Meg x 16) component data sheet

Parameter/Condition		Symbol	-40B	-335	Units
Operating one device bank active-precharge current: $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		$I_{DD}0^{1}$	416	376	mA
Operating one device bank active-read-precharge current: Burst = 4; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Iout = 0mA; Address and control inputs changing once per clock cycle		$I_{DD}1^{1}$	496	476	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = (LOW)		$I_{DD}2P^{2}$	32	32	mA
Idle standby current: CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS, and DM		$I_{DD}2F^{2}$	400	400	mA
Active power-down standby current: One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		$I_{DD}3P^{2}$	280	240	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		$I_{DD}3N^{2}$	480	440	mA
Operating burst read current: Burst = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); Iout = 0mA		$I_{DD}4R^{1}$	736	656	mA
Operating burst write current: Burst = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		$I_{DD}4W^{1}$	736	656	mA
Auto refresh burst current	$^{t}RFC = {}^{t}RFC$ (MIN)	$I_{DD}5^{2}$	1,280	1,280	mA
	^{t}RFC = 7.8125µs	$I_{DD}5A^{2}$	48	48	mA
Self refresh current: CKE ≤ 0.2V		$I_{DD}6^{2}$	32	32	mA
Operating bank interleave read current: Four device bank interleaving reads; (burst = 4) with auto precharge, $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands		$I_{DD}7^{1}$	1,176	1,096	mA

Notes:
1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Table 10: IDD Specifications and Conditions – 256MB (All other Die Revisons)
Values are for the MT46V16M16 DDR SDRAM only and are computed from values specified in the 256Mb (16 Meg x 16) component data sheet

Parameter/Condition		Symbol	-40B	-335	-26A/ -265	Units
Operating one device bank active-precharge current: $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		$I_{DD}0$[1]	556	516	496	mA
Operating one device bank active-read-precharge current: Burst = 4; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); Iout = 0mA; Address and control inputs changing once per clock cycle		$I_{DD}1$[1]	756	736	636	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^tCK = ^tCK$ (MIN); CKE = (LOW)		$I_{DD}2P$[2]	32	32	32	mA
Idle standby current: CS# = HIGH; All device banks idle; $^tCK = ^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		$I_{DD}2F$[2]	480	400	360	mA
Active power-down standby current: One device bank active; Power-down mode; $^tCK = ^tCK$ (MIN); CKE = LOW		$I_{DD}3P$[2]	320	240	200/ 240	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^tRC = ^tRAS$ (MAX); $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		$I_{DD}3N$[2]	560	480	400	mA
Operating burst read current: Burst = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); Iout = 0mA		$I_{DD}4R$[1]	1,056	896	756	mA
Operating burst write current: Burst = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		$I_{DD}4W$[1]	876	796	656	mA
Auto refresh burst current	$^tRFC = ^tRFC$ (MIN)	$I_{DD}5$[2]	2,080	2,040	1,880/ 1,960	mA
	^tRFC = 7.8125µs	$I_{DD}5A$[2]	48	48	48	mA
Self refresh current: CKE ≤ 0.2V		$I_{DD}6$[2]	32	32	32	mA
Operating bank interleave read current: Four device bank interleaving reads; (burst = 4) with auto precharge, $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); Address and control inputs change only during active READ or WRITE commands		$I_{DD}7$[1]	2,056	1,776	1,536/ 1,616	mA

Notes:
1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Table 11: IDD Specifications and Conditions – 512MB

Values are for the MT46V32M16 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 16) component data sheet

Parameter/Condition		Symbol	-40B	-335	-265	Units
Operating one device bank active-precharge current: $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		$I_{DD}0$[1]	640	540	480	mA
Operating one device bank active-read-precharge current: Burst = 4; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Iout = 0mA; Address and control inputs changing once per clock cycle		$I_{DD}1$[1]	800	660	600	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = (LOW)		$I_{DD}2P$[2]	40	40	40	mA
Idle standby current: CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		$I_{DD}2F$[2]	440	360	320	mA
Active power-down standby current: One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		$I_{DD}3P$[2]	360	280	240	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		$I_{DD}3N$[2]	480	400	360	mA
Operating burst read current: Burst = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); Iout = 0mA		$I_{DD}4R$[1]	860	680	600	mA
Operating burst write current: Burst = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		$I_{DD}4W$[1]	880	800	560	mA
Auto refresh burst current	$^{t}RFC = {}^{t}RFC$ (MIN)	$I_{DD}5$[2]	2,760	2,320	2,240	mA
	^{t}RFC = 7.8125µs	$I_{DD}5A$[2]	88	80	80	mA
Self refresh current: CKE ≤ 0.2V		$I_{DD}6$[2]	48	40	40	mA
Operating bank interleave read current: Four device bank interleaving reads; (burst = 4) with auto precharge, $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands		$I_{DD}7$[1]	1,940	1,640	1,420	mA

Notes:
1. Value calculated as one module rank in this operating condition; all other module ranks are in IDD2P (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.3	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–1.0	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
Standby current: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	µA
Power supply current: SCL clock frequency = 100 kHz	I_{CC}	–	2.0	mA

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	$^{t}HD:DAT$	200	–	ns	
SDA fall time	^{t}F	–	300	ns	2
SDA rise time	^{t}R	–	300	ns	2
Data-in hold time	$^{t}HD:DI$	0	–	µs	
Start condition hold time	$^{t}HD:STA$	0.6	–	µs	
Clock HIGH period	$^{t}HIGH$	0.6	–	µs	
Clock LOW period	^{t}LOW	1.3	–	µs	
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	$^{t}SU:DAT$	100	–	ns	
Start condition setup time	$^{t}SU:STA$	0.6	–	µs	3
Stop condition setup time	$^{t}SU:STO$	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	5	ms	4

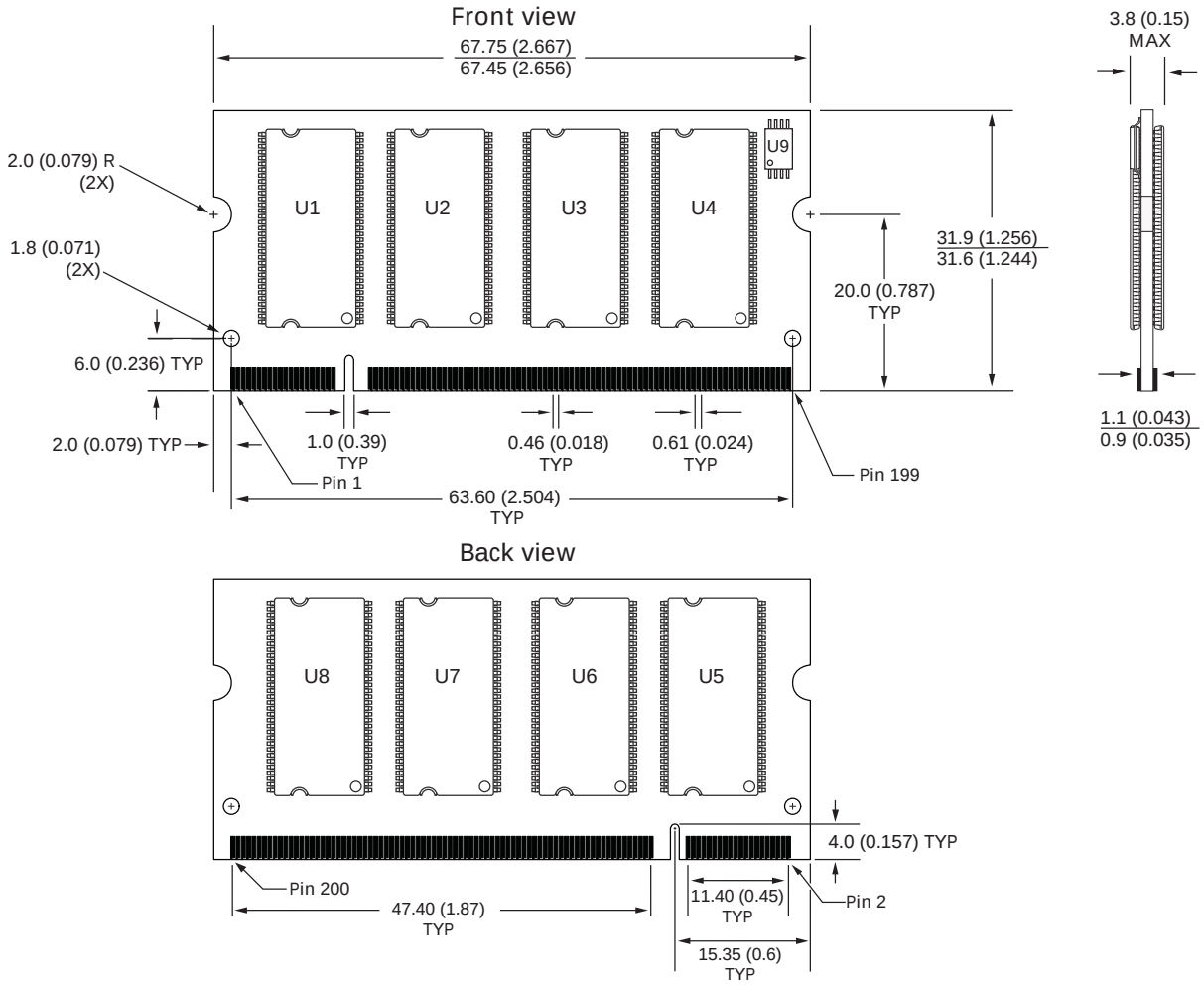
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 3: 200-Pin DDR SODIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.