



CMOS ± 5 V/+5 V/+3 V Triple SPDT Switch

ADG633

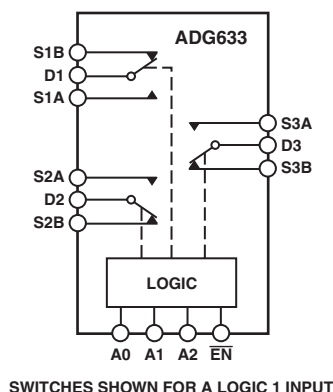
FEATURES

- ± 2 V to ± 6 V Dual Supply
- 2 V to 12 V Single Supply
- Automotive Temperature Range -40°C to $+125^{\circ}\text{C}$
- <0.2 nA Leakage Currents
- 52 Ω On Resistance over Full Signal Range
- Rail-to-Rail Switching Operation
- 16-Lead Chip Scale/TSSOP Packages
- Typical Power Consumption <0.1 μW
- TTL/CMOS Compatible Inputs
- Package Upgrades to 74HC4053 and MAX4053/MAX4583

APPLICATIONS

- Automotive Applications
- Automatic Test Equipment
- Data Acquisition Systems
- Battery Powered Systems
- Communication Systems
- Audio and Video Signal Routing
- Relay Replacement
- Sample-and-Hold Systems
- Industrial Control Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG633 is a low voltage CMOS device comprising three independently selectable SPDT (single pole double throw) switches. They are fully specified for ± 5 V, +5 V, and +3 V supplies. The ADG633 switches are turned on with a logic low (or high) on the appropriate control input. Each switch conducts equally well in both directions when ON and has an input signal range that extends to the supplies. An $\overline{\text{EN}}$ input is used to enable or disable the device. When disabled, all channels are switched off.

These parts are designed on an enhanced process that provides lower power dissipation yet gives high switching speeds. Low power consumption and an operating supply range of 2 V to 12 V make the ADG633 ideal for battery-powered portable instruments. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. All digital inputs have 0.8 V to 2.4 V logic thresholds, ensuring TTL/CMOS logic compatibility when using single +5 V or dual ± 5 V supplies.

The ADG633 is available in small 16-lead TSSOP packages and 16-lead 4 mm $\times$ 4 mm chip scale packages.

PRODUCT HIGHLIGHTS

1. Single- and dual-supply operation. The ADG633 offers high performance and is fully specified and guaranteed with ± 5 V, +5 V and +3 V supply rails.
2. Automotive temperature range -40°C to $+125^{\circ}\text{C}$.
3. Guaranteed break-before-make switching action.
4. Low power consumption, typically <0.1 μW .
5. Small 16-lead TSSOP and 16-lead 4 mm $\times$ 4 mm chip scale packages.

REV.0

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ADG633—SPECIFICATIONS

DUAL SUPPLY¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.)

Parameter	+25°C	B Version –40°C to +85°C	Y Version –40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			V_{SS} to V_{DD}	V	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
On Resistance (R_{ON})	52			Ω typ	$V_S = \pm 4.5\text{ V}$, $I_S = 1\text{ mA}$;
	75	90	100	Ω max	Test Circuit 1
On Resistance Match between	0.8			Ω typ	
Channels (ΔR_{ON})	1.3	1.8	2	Ω max	$V_S = +3.5\text{ V}$, $I_S = 1\text{ mA}$
On Resistance Flatness ($R_{FLAT(ON)}$)	9			Ω typ	$V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$;
	12	13	14	Ω max	$V_S = \pm 3\text{ V}$, $I_S = 1\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.005			nA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
	± 0.2		± 5	nA max	$V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$;
Drain OFF Leakage I_D (OFF)	± 0.005			nA typ	Test Circuit 2
	± 0.2		± 5	nA max	$V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$;
Channel ON Leakage I_D , I_S (ON)	± 0.005			nA typ	Test Circuit 3
	± 0.2		± 5	nA max	$V_D = V_S = \pm 4.5\text{ V}$; Test Circuit 4
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 1	μA max	
C_{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{TRANS}	60			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
	90	110	130	ns max	$V_S = 3\text{ V}$; Test Circuit 5
$t_{ON}(\overline{EN})$	70			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
	95	120	135	ns max	$V_S = 3\text{ V}$; Test Circuit 7
$t_{OFF}(\overline{EN})$	25			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
	40	45	50	ns max	$V_S = 3\text{ V}$; Test Circuit 7
Break-Before-Make Time Delay, t_{BBM}	40			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
			10	ns min	$V_{S1} = V_{S2} = 3\text{ V}$; Test Circuit 6
Charge Injection	2			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$,
	4			pC max	$C_L = 1\text{ nF}$; Test Circuit 8
Off Isolation	–90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$,
					$f = 1\text{ MHz}$; Test Circuit 9
Total Harmonic Distortion, THD + N	0.025			% typ	$R_L = 600\ \Omega$, 2 V p-p ,
					$f = 20\text{ Hz to } 20\text{ kHz}$
Channel-to-Channel Crosstalk	–90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$,
					$f = 1\text{ MHz}$; Test Circuit 11
–3 dB Bandwidth	580			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$;
					Test Circuit 10
C_S (OFF)	4			pF typ	$f = 1\text{ MHz}$
C_D (OFF)	7			pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	12			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.01			μA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
			1	μA max	Digital Inputs = 0 V or 5.5 V
I_{SS}	0.01			μA typ	Digital Inputs = 0 V or 5.5 V
			1	μA max	

NOTES

¹Temperature range is as follows: B Version: –40°C to +85°C. Y Version: –40°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.)

Parameter	+25°C	B Version –40°C to +85°C	Y Version –40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	$V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance (R_{ON})	85			Ω typ	$V_S = 0\text{ V}$ to 4.5 V , $I_S = 1\text{ mA}$;
	150	160	200	Ω max	Test Circuit 1
On Resistance Match between Channels (ΔR_{ON})	4.5			Ω typ	$V_S = +3.5\text{ V}$, $I_S = 1\text{ mA}$
	8	9	10	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	13	14	16	Ω typ	$V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1.5\text{ V}$ to 4 V , $I_S = 1\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.005			nA typ	$V_{DD} = 5.5\text{ V}$
	± 0.2		± 5	nA max	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$;
Drain OFF Leakage I_D (OFF)	± 0.005			nA typ	Test Circuit 2
	± 0.2		± 5	nA max	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$;
Channel ON Leakage I_D , I_S (ON)	± 0.005			nA typ	Test Circuit 3
	± 0.2		± 5	nA max	$V_S = V_D = 1\text{ V}$ or 4.5 V ; Test Circuit 4
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005			μA typ	
			± 1	μA max	
C_{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{TRANS}	100			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
	150	190	220	ns max	$V_S = 3\text{ V}$; Test Circuit 5
$t_{ON}(\overline{EN})$	100			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
	150	190	220	ns max	$V_S = 3\text{ V}$; Test Circuit 7
$t_{OFF}(\overline{EN})$	25			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
	35	45	50	ns max	$V_S = 3\text{ V}$; Test Circuit 7
Break-Before-Make Time Delay, t_{BBM}	90			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
			10	ns min	$V_{S1} = V_{S2} = 3\text{ V}$; Test Circuit 6
Charge Injection	0.5			pC typ	$V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$;
	1			pC max	Test Circuit 8
Off Isolation	–90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
					Test Circuit 9
Channel-to-Channel Crosstalk	–90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
					Test Circuit 11
–3 dB Bandwidth	520			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$;
					Test Circuit 10
C_S (OFF)	5			pF typ	$f = 1\text{ MHz}$
C_D (OFF)	8			pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	12			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.01			μA typ	$V_{DD} = 5.5\text{ V}$
			1	μA max	Digital Inputs = 0 V or 5.5 V

NOTES

¹Temperature range is as follows: B Version: –40°C to +85°C. Y Version: –40°C to +125°C.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG633—SPECIFICATIONS

SINGLE SUPPLY¹ ($V_{DD} = 2.7\text{ V}$ to 3.6 V , $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.)

Parameter	+25°C	B Version −40°C to +85°C	Y Version −40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	$V_{DD} = 2.7\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance (R_{ON})	185			Ω typ	$V_S = 0\text{ V}$ to 2.7 V , $I_S = 0.1\text{ mA}$;
	300	350	400	Ω max	Test Circuit 1
On Resistance Match between	2			Ω typ	$V_S = +1.5\text{ V}$, $I_S = 0.1\text{ mA}$
Channels (ΔR_{ON})	4.5	6	7	Ω max	
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.005			nA typ	$V_{DD} = 3.3\text{ V}$
	± 0.2		± 5	nA max	$V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$;
Drain OFF Leakage I_D (OFF)	± 0.005			nA typ	Test Circuit 2
	± 0.2		± 5	nA max	$V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$;
Channel ON Leakage I_D , I_S (ON)	± 0.005			nA typ	Test Circuit 3
	± 0.2		± 5	nA max	$V_S = V_D = 1\text{ V}$ or 3 V ; Test Circuit 4
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}			0.5	V max	
Input Current I_{INL} or I_{INH}	0.005			μA typ	
			± 1	μA max	
C_{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{TRANS}	170			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
	300	370	400	ns max	$V_S = 1.5\text{ V}$; Test Circuit 5
$t_{ON}(\overline{EN})$	200			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
	310	380	420	ns max	$V_S = 1.5\text{ V}$; Test Circuit 7
$t_{OFF}(\overline{EN})$	30			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
	40	55	75	ns max	$V_S = 1.5\text{ V}$; Test Circuit 7
Break-Before-Make Time Delay, t_{BBM}	180			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
			10	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$; Test Circuit 6
Charge Injection	1			pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$;
	2			pC max	Test Circuit 8
Off Isolation	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
					Test Circuit 9
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
					Test Circuit 11
−3 dB Bandwidth	500			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$;
					Test Circuit 10
C_S (OFF)	5			pF typ	$f = 1\text{ MHz}$
C_D (OFF)	8			pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	12			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.01			μA typ	$V_{DD} = 3.3\text{ V}$
			1	μA max	Digital Inputs = 0 V or 3.3 V

NOTES

¹Temperature range is as follows: B Version: −40°C to +85°C. Y Version: −40°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C, unless otherwise noted.)

V _{DD} to V _{SS}	13 V
V _{DD} to GND	–0.3 V to +13 V
V _{SS} to GND	+0.3 V to –6.5 V
Analog Inputs ²	V _{SS} – 0.3 V to V _{DD} + 0.3 V
Digital Inputs ²	GND – 0.3 V to V _{DD} + 0.3 V or 10 mA, whichever occurs first
Peak Current, S or D	40 mA (Pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	20 mA
Operating Temperature Range	
Automotive (Y Version)	–40°C to +125°C
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

Junction Temperature	150°C
θ _{JA} Thermal Impedance, 16-Lead TSSOP	150.4°C/W
θ _{JA} Thermal Impedance (4-Layer Board), 16-Lead LFCSP	70°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	4 kV

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at A_X, $\overline{\text{EN}}$, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG633 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG633YRU	–40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG633YCP	–40°C to +85°C	Chip Scale Package (LFCSP)	CP-16

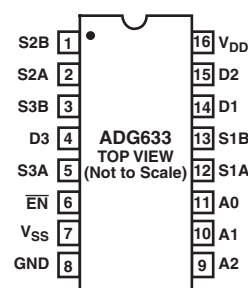
Table I. ADG633 Truth Table

A2	A1	A0	$\overline{\text{EN}}$	Switch Condition
X	X	X	1	NONE
0	0	0	0	D1–S1A, D2–S2A, D3–S3A
0	0	1	0	D1–S1B, D2–S2A, D3–S3A
0	1	0	0	D1–S1A, D2–S2B, D3–S3A
0	1	1	0	D1–S1B, D2–S2B, D3–S3A
1	0	0	0	D1–S1A, D2–S2A, D3–S3B
1	0	1	0	D1–S1B, D2–S2A, D3–S3B
1	1	0	0	D1–S1A, D2–S2B, D3–S3B
1	1	1	0	D1–S1B, D2–S2B, D3–S3B

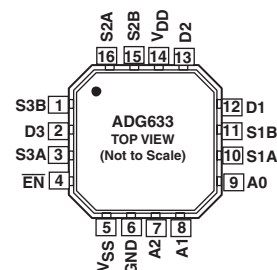
X = Don't Care

PIN CONFIGURATIONS

TSSOP



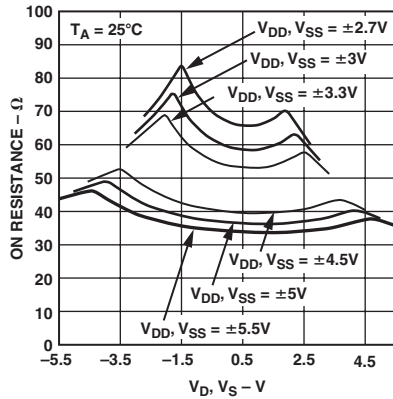
LFCSP



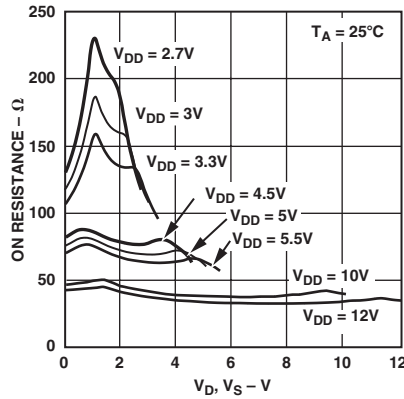
TERMINOLOGY

Parameter	Definition
V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply Potential.
I_{DD}	Positive Supply Current.
I_{SS}	Negative Supply Current.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
A_X	Logic Control Input.
$\overline{EN}$	Active Low Digital Input. When high, device is disabled and all switches are OFF. When low, A_X logic inputs determine ON switches.
V_D, V_S	Analog Voltage on Terminals D, S.
R_{ON}	Ohmic Resistance between D and S.
ΔR_{ON}	On Resistance Match between Any Two Channels, i.e., $R_{ON\ max} - R_{ON\ min}$.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of On Resistance as measured over the specified analog signal range.
$I_S\ (OFF)$	Source Leakage Current with the Switch OFF.
$I_D\ (OFF)$	Drain Leakage Current with the Switch OFF.
$I_D, I_S\ (ON)$	Channel Leakage Current with the Switch ON.
V_{INL}	Maximum Input Voltage for Logic 0.
V_{INH}	Minimum Input Voltage for Logic 1.
I_{INL}, I_{INH}	Input Current of the Digital Input.
$C_S\ (OFF)$	OFF Switch Source Capacitance. Measured with reference to ground.
$C_D\ (OFF)$	OFF Switch Drain Capacitance. Measured with reference to ground.
$C_D, C_S\ (ON)$	ON Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance.
$t_{ON}\ (\overline{EN})$	Delay between Applying the Digital Control Input and the Output Switching ON. See Test Circuit 7.
$t_{OFF}\ (\overline{EN})$	Delay between Applying the Digital Control Input and the Output Switching OFF.
t_{BBM}	ON Time, measured between 80% points of both switches when switching from one address state to another.
Charge Injection	A Measure of the Glitch Impulse Transferred from the Digital Input to the Analog Output during Switching.
OFF Isolation	A Measure of Unwanted Signal Coupling through an OFF Switch.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Bandwidth	The Frequency at which the Output Is Attenuated by 3 dB.
ON Response	The Frequency Response of the ON Switch.
Insertion Loss	The Loss Due to the On Resistance of the Switch.

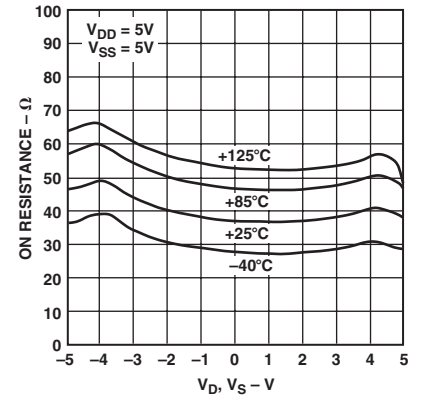
Typical Performance Characteristics—ADG633



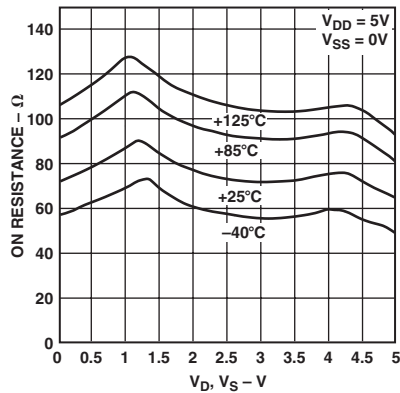
TPC 1. On Resistance vs. V_D (V_S) for Dual Supply



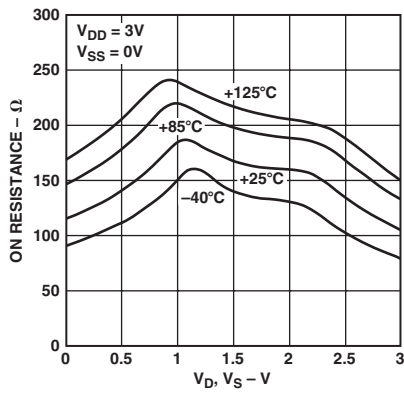
TPC 2. On Resistance vs. V_D (V_S) for Single Supply



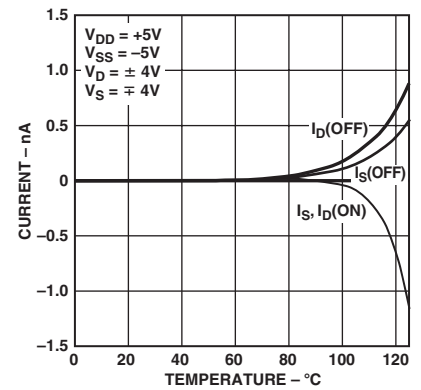
TPC 3. On Resistance vs. V_D (V_S) for Different Temperatures (Dual Supply)



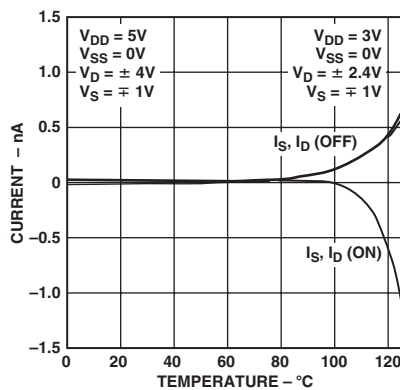
TPC 4. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)



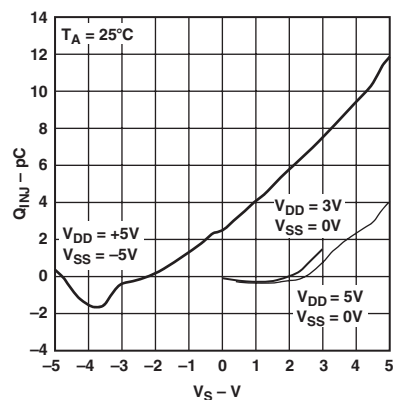
TPC 5. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)



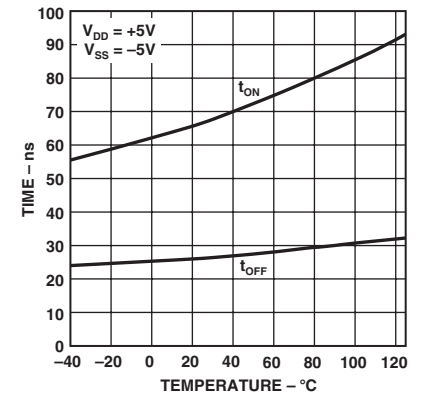
TPC 6. Leakage Currents vs. Temperature (Dual Supply)



TPC 7. Leakage Currents vs. Temperature (Single Supply)

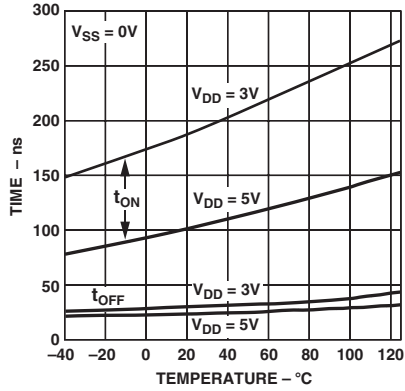


TPC 8. Charge Injection vs. Source Voltage

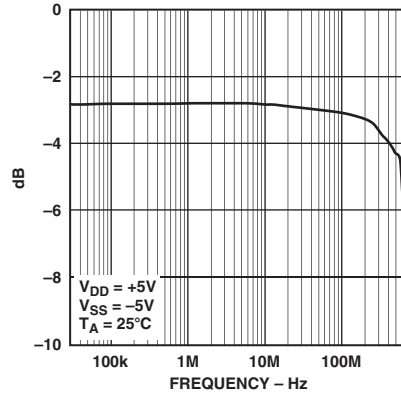


TPC 9. t_{ON}/t_{OFF} Times vs. Temperature (Dual Supply)

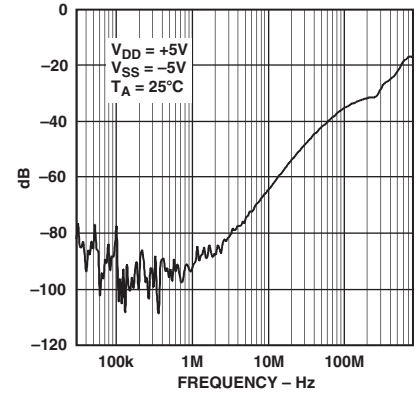
ADG633



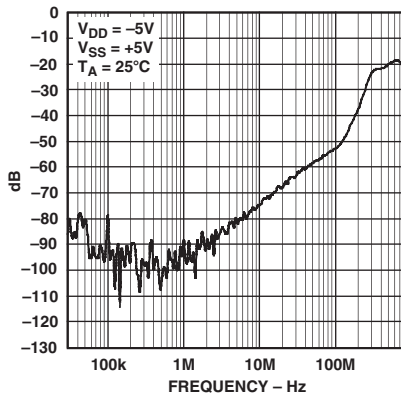
TPC 10. t_{ON}/t_{OFF} Times vs. Temperature (Single Supply)



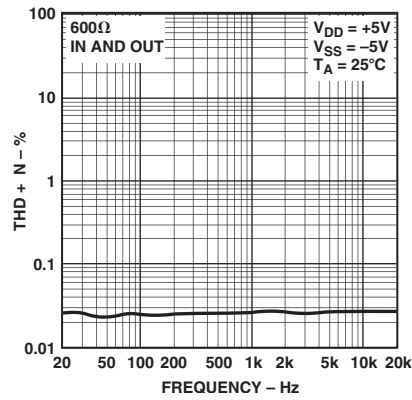
TPC 11. ON Response vs. Frequency



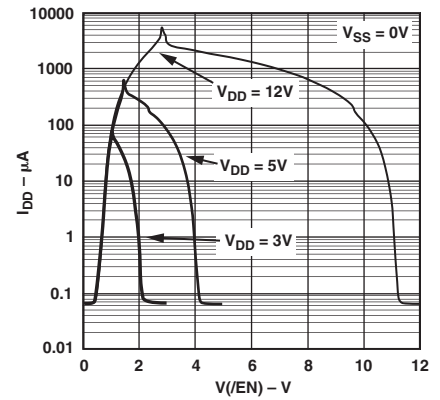
TPC 12. OFF Isolation vs. Frequency



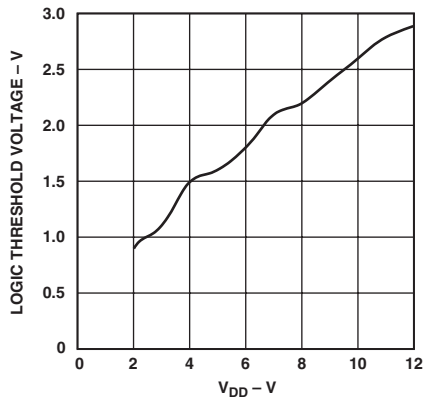
TPC 13. Crosstalk vs. Frequency



TPC 14. THD + Noise

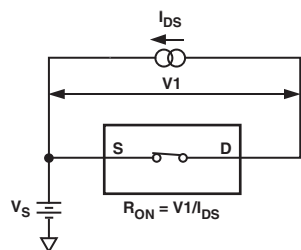


TPC 15. V_{DD} Current vs. Logic Level

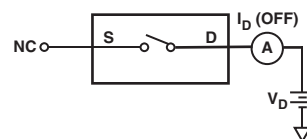


TPC 16. Logic Level Threshold vs. V_{DD}

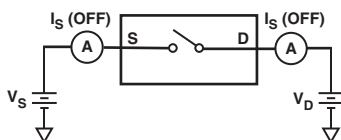
Test Circuits



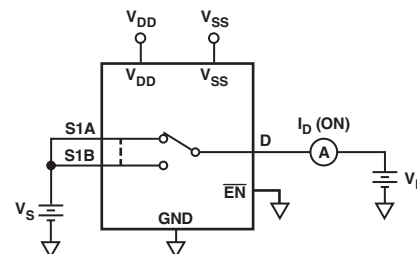
Test Circuit 1. On Resistance



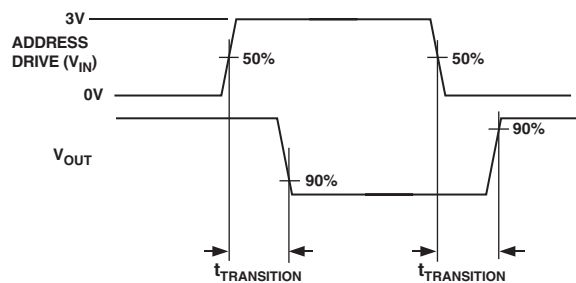
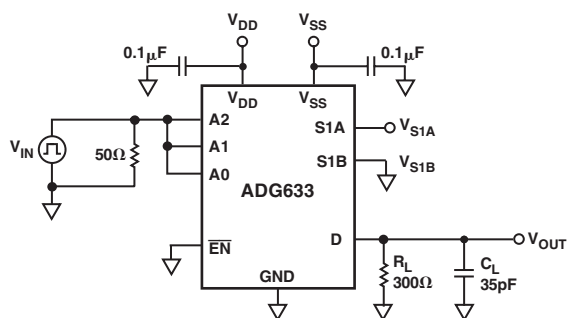
Test Circuit 3. I_D (OFF)



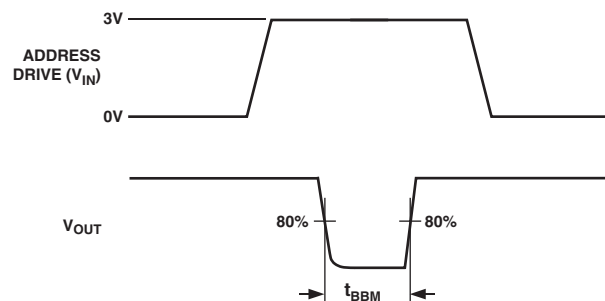
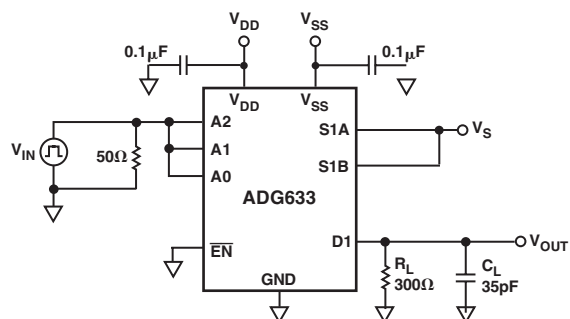
Test Circuit 2. I_S (OFF)



Test Circuit 4. I_D (ON)

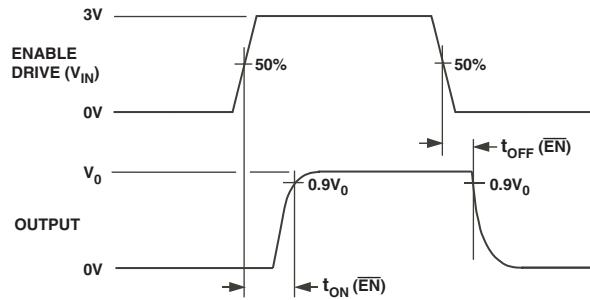
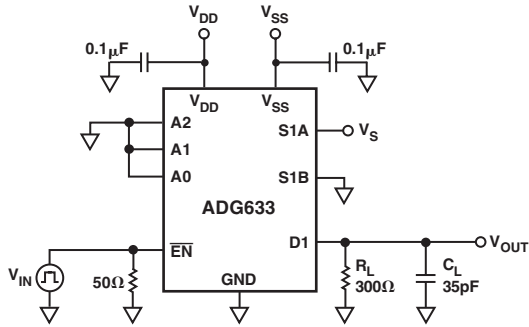


Test Circuit 5. Transition Time, $t_{\text{TRANSITION}}$

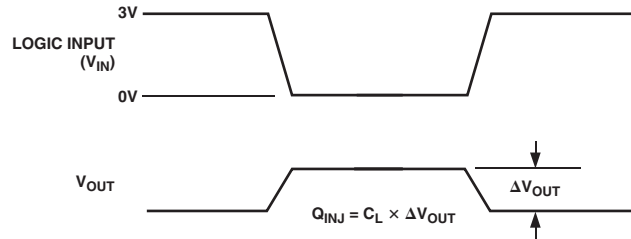
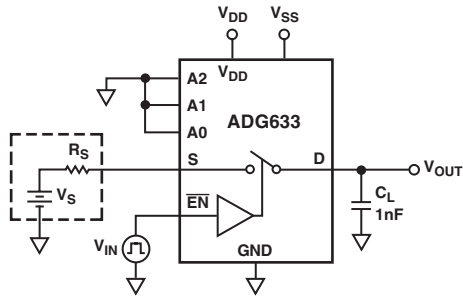


Test Circuit 6. Break-Before-Make Delay, t_{BBM}

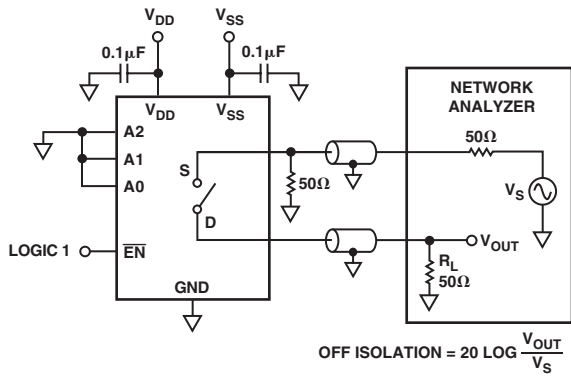
ADG633



Test Circuit 7. Enable Delay, $t_{ON}(\overline{EN})$, $t_{OFF}(\overline{EN})$

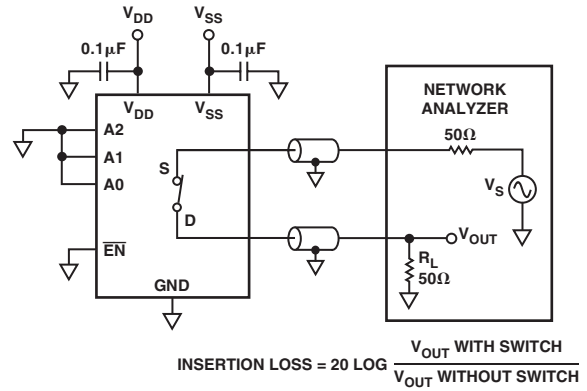


Test Circuit 8. Charge Injection



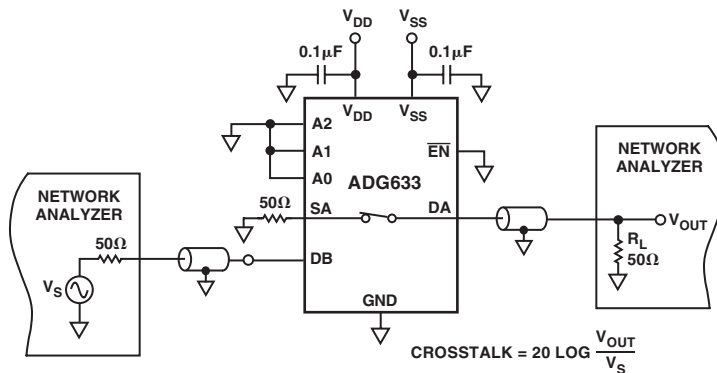
$$\text{OFF ISOLATION} = 20 \text{ LOG } \frac{V_{OUT}}{V_S}$$

Test Circuit 9. OFF Isolation



$$\text{INSERTION LOSS} = 20 \text{ LOG } \frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}}$$

Test Circuit 10. Bandwidth



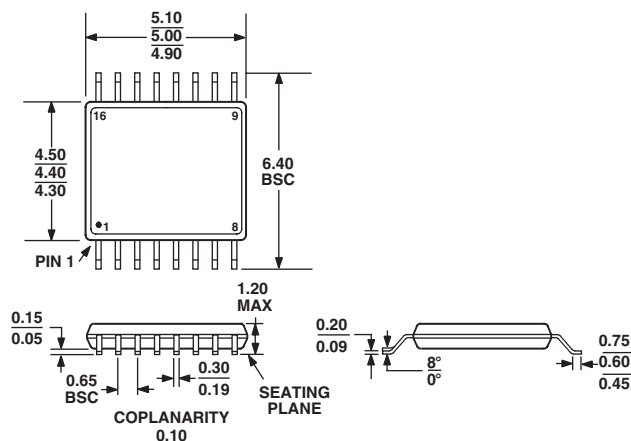
$$\text{CROSSTALK} = 20 \text{ LOG } \frac{V_{OUT}}{V_S}$$

Test Circuit 11. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

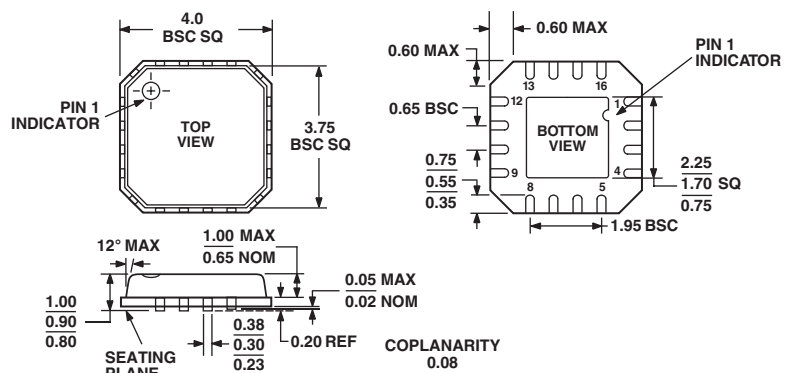
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB

16-Lead Frame Chip Scale Package [LFCSP] 4 mm × 4 mm Body (CP-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

