



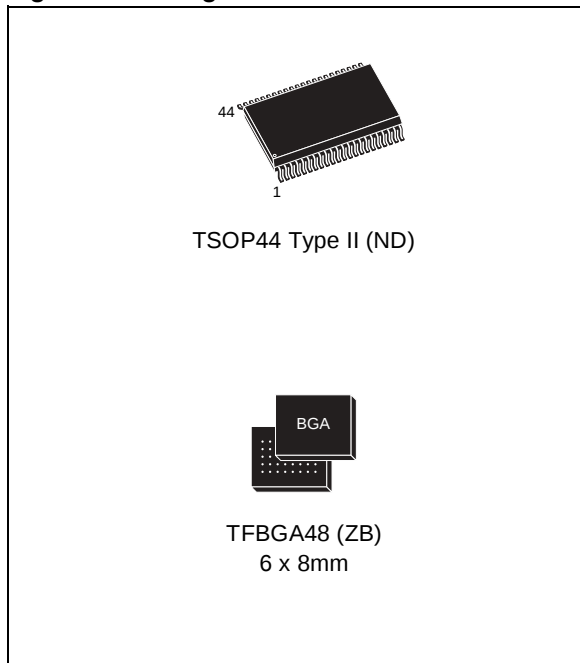
## M68AW128M

### 2 Mbit (128K x16) 3.0V Asynchronous SRAM

#### FEATURES SUMMARY

- SUPPLY VOLTAGE: 2.7 to 3.6V
- 128K x 16 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIME: 55ns
- SINGLE BYTE READ/WRITE
- LOW STANDBY CURRENT
- LOW  $V_{CC}$  DATA RETENTION: 1.5V
- TRI-STATE COMMON I/O
- AUTOMATIC POWER DOWN
- PACKAGES
  - Compliant with Lead-Free Soldering Processes
  - Lead-Free Versions

Figure 1. Packages



## TABLE OF CONTENTS

|                                                                                                       |           |
|-------------------------------------------------------------------------------------------------------|-----------|
| <b>FEATURES SUMMARY .....</b>                                                                         | <b>1</b>  |
| Figure 1. Packages.....                                                                               | 1         |
| <b>SUMMARY DESCRIPTION.....</b>                                                                       | <b>4</b>  |
| Figure 2. Logic Diagram .....                                                                         | 4         |
| Table 1. Signal Names .....                                                                           | 4         |
| Figure 3. TSOP Connections .....                                                                      | 5         |
| Figure 4. TFBGA Connections (Top view through package) .....                                          | 6         |
| Figure 5. Block Diagram .....                                                                         | 7         |
| <b>OPERATION .....</b>                                                                                | <b>8</b>  |
| <b>Read Mode .....</b>                                                                                | <b>8</b>  |
| <b>Write Mode .....</b>                                                                               | <b>8</b>  |
| Table 2. Operating Modes.....                                                                         | 8         |
| <b>MAXIMUM RATING.....</b>                                                                            | <b>9</b>  |
| Table 3. Absolute Maximum Ratings.....                                                                | 9         |
| <b>DC AND AC PARAMETERS.....</b>                                                                      | <b>10</b> |
| Table 4. Operating and AC Measurement Conditions.....                                                 | 10        |
| Figure 6. AC Measurement I/O Waveform .....                                                           | 10        |
| Figure 7. AC Measurement Load Circuit.....                                                            | 10        |
| Table 5. Capacitance.....                                                                             | 11        |
| Table 6. DC Characteristics .....                                                                     | 11        |
| Figure 8. Address Controlled, Read Mode AC Waveforms .....                                            | 12        |
| Figure 9. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.....                        | 12        |
| Figure 10. Chip Enable or $\overline{UB}/\overline{LB}$ Controlled, Standby Mode AC Waveforms .....   | 13        |
| Table 7. Read and Standby Mode AC Characteristics .....                                               | 13        |
| Figure 11. Write Enable Controlled, Write AC Waveforms.....                                           | 14        |
| Figure 12. Chip Enable Controlled, Write AC Waveforms .....                                           | 14        |
| Figure 13. $\overline{UB}/\overline{LB}$ Controlled, Write AC Waveforms .....                         | 15        |
| Table 8. Write Mode AC Characteristics .....                                                          | 16        |
| Figure 14. Low $V_{CC}$ Data Retention AC Waveforms .....                                             | 17        |
| Table 9. Low $V_{CC}$ Data Retention Characteristics.....                                             | 17        |
| <b>PACKAGE MECHANICAL .....</b>                                                                       | <b>18</b> |
| Figure 15. TSOP44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Outline .....         | 18        |
| Table 10. TSOP 44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Mechanical Data ..... | 18        |
| Figure 16. TFBGA48 6x8mm - 6x8 Active Ball Array, 0.75mm pitch, Bottom View Package Outline .....     | 19        |
| Table 11. TFBGA48 6x8mm - 6x8 Active Ball Array, 0.75mm pitch, Package Mechanical Data ..             | 19        |

|                                             |           |
|---------------------------------------------|-----------|
| <b>PART NUMBERING</b> .....                 | <b>20</b> |
| Table 12. Ordering Information Scheme ..... | 20        |
| <b>REVISION HISTORY</b> .....               | <b>21</b> |
| Table 13. Document Revision History .....   | 21        |

SUMMARY DESCRIPTION

The M68AW128M is a 2 Mbit (2,097,152 bit) CMOS SRAM, organized as 131,072 words by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.7 to 3.6V supply. This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AW128M is available in TFBGA48 (0.75 mm pitch) and in TSOP44 Type II packages. In addition to the standard version, the packages are also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECO-PACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive. All packages are compliant with Lead-free soldering processes.

Figure 2. Logic Diagram

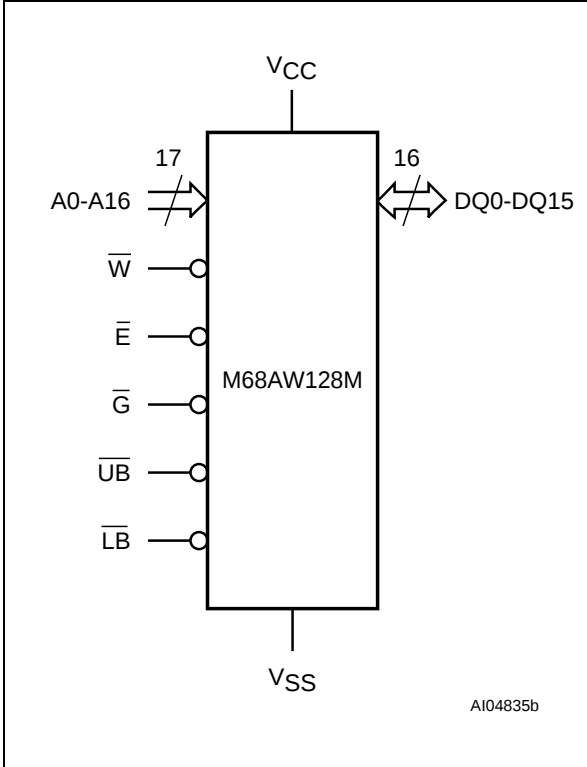


Table 1. Signal Names

|                 |                                   |
|-----------------|-----------------------------------|
| A0-A16          | Address Inputs                    |
| DQ0-DQ15        | Data Input/Output                 |
| $\overline{E}$  | Chip Enable                       |
| $\overline{G}$  | Output Enable                     |
| $\overline{W}$  | Write Enable                      |
| $\overline{UB}$ | Upper Byte Enable Input           |
| $\overline{LB}$ | Lower Byte Enable Input           |
| VCC             | Supply Voltage                    |
| VSS             | Ground                            |
| NC              | Not Connected Internally          |
| DU              | Don't Use as Internally Connected |

Figure 3. TSOP Connections

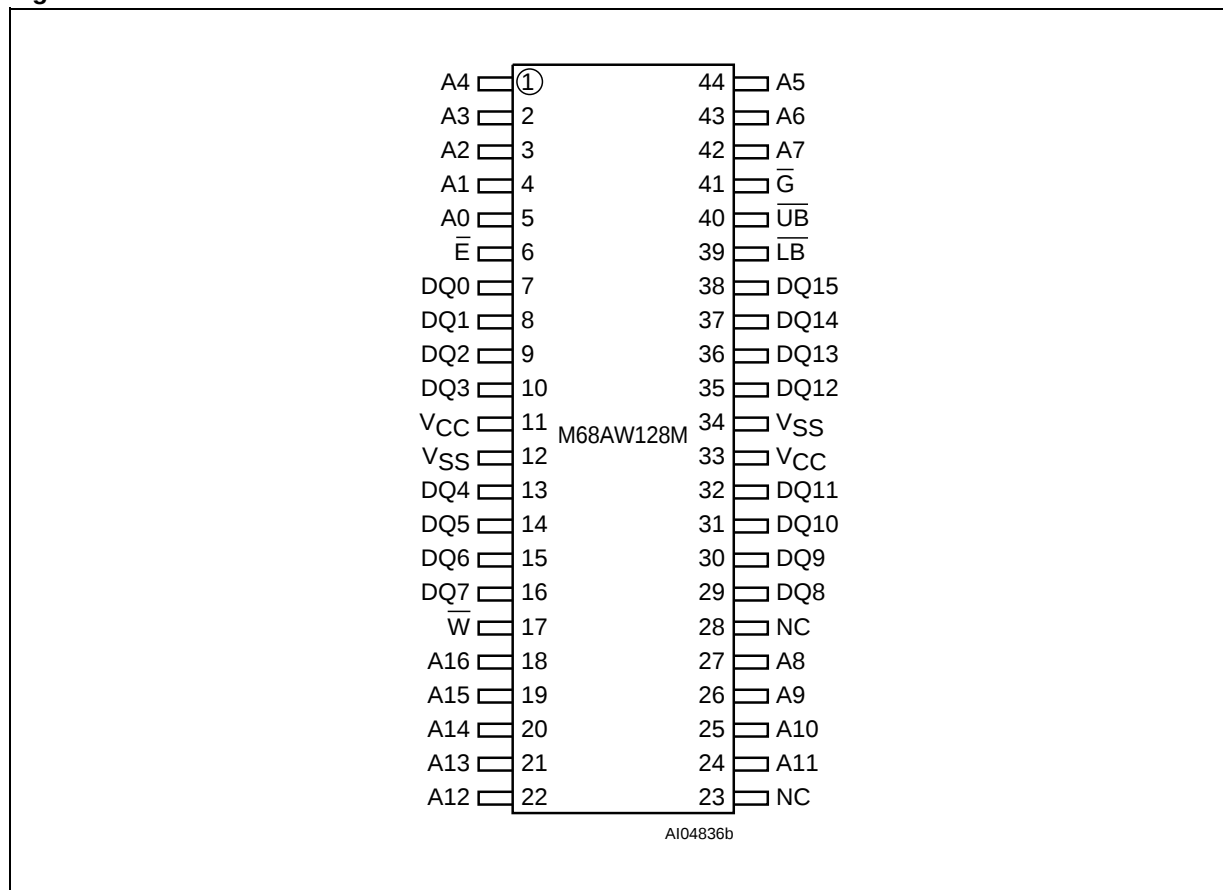


Figure 4. TFBGA Connections (Top view through package)

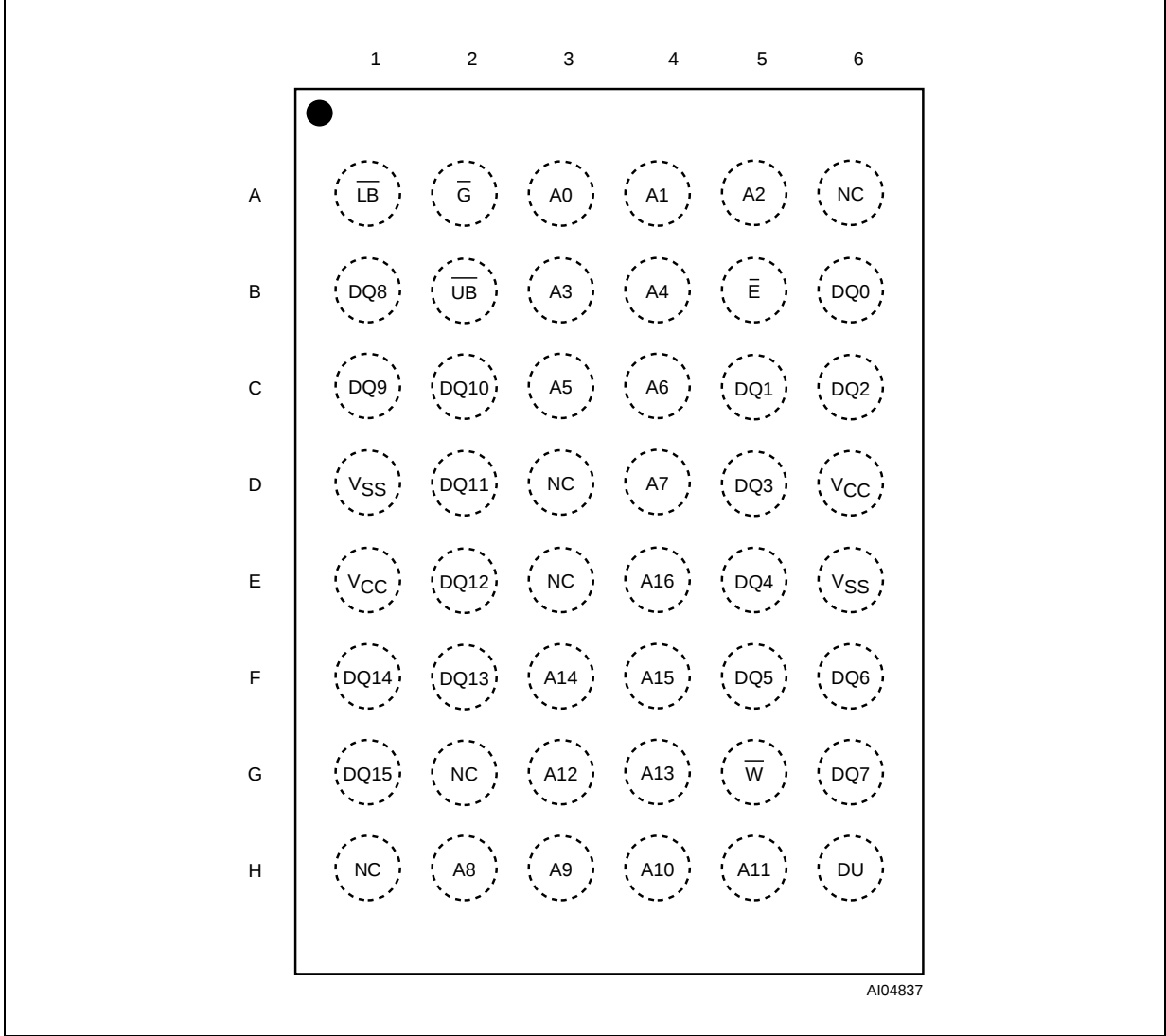
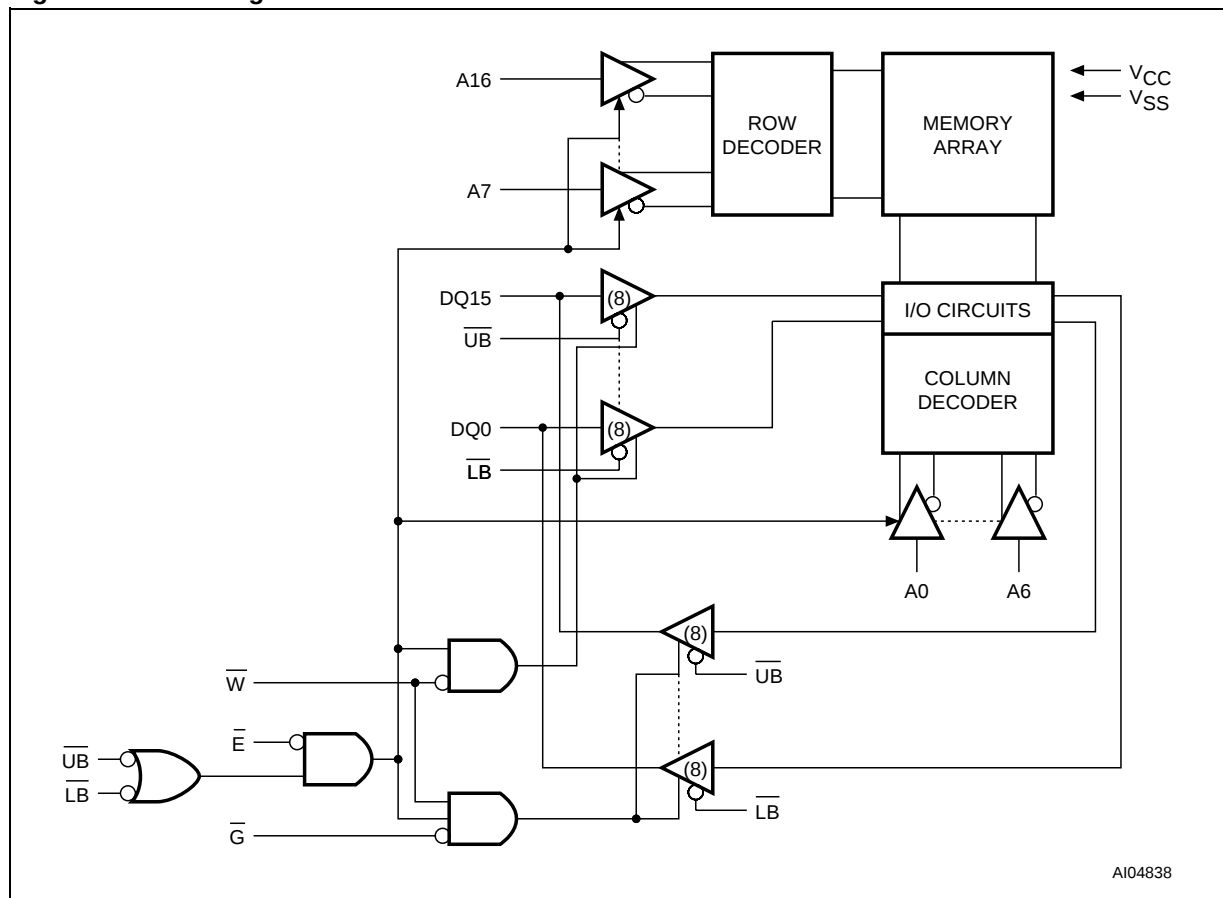


Figure 5. Block Diagram



## OPERATION

The M68AW128M has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ( $\overline{E}$  = High) or LB and UB are de-asserted (LB and UB = High). An Output Enable ( $\overline{G}$ ) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs  $\overline{W}$ ,  $\overline{E}$ ,  $\overline{LB}$  and  $\overline{UB}$  as summarized in the Operating Modes table (see Table 2).

### Read Mode

The M68AW128M is in the Read mode whenever Write Enable ( $\overline{W}$ ) is High with Output Enable ( $\overline{G}$ ) Low, and Chip Enable ( $\overline{E}$ ) is asserted. This provides access to data from eight or sixteen, depending on the status of the signal UB and LB, of the 2,097,152 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight or sixteen output pins within  $t_{AVQV}$  after the last stable address, providing  $\overline{G}$  is Low and  $\overline{E}$  is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter ( $t_{ELQV}$ ,  $t_{GLQV}$  or  $t_{BLQV}$ ) rather than the address. Data out

may be indeterminate at  $t_{ELQX}$ ,  $t_{GLQX}$  and  $t_{BLQX}$  but data lines will always be valid at  $t_{AVQV}$ .

### Write Mode

The M68AW128M is in the Write mode whenever the  $\overline{W}$  and  $\overline{E}$  are Low. Either the Chip Enable input ( $\overline{E}$ ) or the Write Enable input ( $\overline{W}$ ) must be de-asserted during Address transitions for subsequent write cycles. When  $\overline{E}$  ( $\overline{W}$ ) is Low, and UB or LB is Low, write cycle begins on the  $\overline{W}$  ( $\overline{E}$ )'s falling edge. When  $\overline{E}$  and  $\overline{W}$  are Low, and  $\overline{UB} = \overline{LB} = \text{High}$ , write cycle begins on the first falling edge of UB or LB. Therefore, address setup time is referenced to Write Enable, Chip Enable or UB/LB as  $t_{AVWL}$ ,  $t_{AVEL}$  and  $t_{AVBL}$  respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of  $\overline{E}$ ,  $\overline{W}$  or UB/LB.

If the Output is enabled ( $\overline{E} = \text{Low}$ ,  $\overline{G} = \text{Low}$ ,  $\overline{LB}$  or  $\overline{UB} = \text{Low}$ ), then  $\overline{W}$  will return the outputs to high impedance within  $t_{WLQZ}$  of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for  $t_{DVWH}$  before the rising edge of Write Enable, or for  $t_{DVEH}$  before the rising edge of  $\overline{E}$ , or for  $t_{DVBH}$  before the

**Table 2. Operating Modes**

| Operation        | $\overline{E}$ | $\overline{W}$ | $\overline{G}$ | $\overline{LB}$ | $\overline{UB}$ | DQ0-DQ7     | DQ8-DQ15    | Power                |
|------------------|----------------|----------------|----------------|-----------------|-----------------|-------------|-------------|----------------------|
| Deselected       | $V_{IH}$       | X              | X              | X               | X               | Hi-Z        | Hi-Z        | Standby ( $I_{SB}$ ) |
| Deselected       | X              | X              | X              | $V_{IH}$        | $V_{IH}$        | Hi-Z        | Hi-Z        | Standby ( $I_{SB}$ ) |
| Lower Byte Read  | $V_{IL}$       | $V_{IH}$       | $V_{IL}$       | $V_{IL}$        | $V_{IH}$        | Data Output | Hi-Z        | Active ( $I_{CC}$ )  |
| Lower Byte Write | $V_{IL}$       | $V_{IL}$       | X              | $V_{IL}$        | $V_{IH}$        | Data Input  | Hi-Z        | Active ( $I_{CC}$ )  |
| Output Disabled  | $V_{IL}$       | $V_{IH}$       | $V_{IH}$       | X               | X               | Hi-Z        | Hi-Z        | Active ( $I_{CC}$ )  |
| Upper Byte Read  | $V_{IL}$       | $V_{IH}$       | $V_{IL}$       | $V_{IH}$        | $V_{IL}$        | Hi-Z        | Data Output | Active ( $I_{CC}$ )  |
| Upper Byte Write | $V_{IL}$       | $V_{IL}$       | X              | $V_{IH}$        | $V_{IL}$        | Hi-Z        | Data Input  | Active ( $I_{CC}$ )  |
| Word Read        | $V_{IL}$       | $V_{IH}$       | $V_{IL}$       | $V_{IL}$        | $V_{IL}$        | Data Output | Data Output | Active ( $I_{CC}$ )  |
| Word Write       | $V_{IL}$       | $V_{IL}$       | X              | $V_{IL}$        | $V_{IL}$        | Data Input  | Data Input  | Active ( $I_{CC}$ )  |

Note: 1. X =  $V_{IH}$  or  $V_{IL}$ .

## MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for periods greater than 1s periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute Maximum Ratings**

| Symbol         | Parameter                         | Value                  | Unit |
|----------------|-----------------------------------|------------------------|------|
| $I_O^{(1)}$    | Output Current                    | 20                     | mA   |
| $P_D$          | Power Dissipation                 | 1                      | W    |
| $T_A$          | Ambient Operating Temperature     | -55 to 125             | °C   |
| $T_{STG}$      | Storage Temperature               | -65 to 150             | °C   |
| $T_{LEAD}$     | Lead Temperature during Soldering | (2)                    | °C   |
| $V_{CC}$       | Supply Voltage                    | -0.5 to 4.6            | V    |
| $V_{IO}^{(3)}$ | Input or Output Voltage           | -0.5 to $V_{CC} + 0.5$ | V    |

Note: 1. One output at time not to exceed 1 second duration.

2. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

3. Up to a maximum operating  $V_{CC}$  of 3.6V only.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. Operating and AC Measurement Conditions

| Parameter                                              |         | M68AW128M                                                                   |
|--------------------------------------------------------|---------|-----------------------------------------------------------------------------|
| V <sub>CC</sub> Supply Voltage                         |         | 2.7 to 3.6V                                                                 |
| Ambient Operating Temperature                          | Range 1 | 0 to 70°C                                                                   |
|                                                        | Range 6 | −40 to 85°C                                                                 |
| Load Capacitance (C <sub>L</sub> )                     |         | 30pF                                                                        |
| Output Circuit Protection Resistance (R <sub>1</sub> ) |         | 3.0kΩ                                                                       |
| Load Resistance (R <sub>2</sub> )                      |         | 3.1kΩ                                                                       |
| Input Rise and Fall Times                              |         | 1ns/V                                                                       |
| Input Pulse Voltages                                   |         | 0 to V <sub>CC</sub>                                                        |
| Input and Output Timing Ref. Voltages                  |         | V <sub>CC</sub> /2                                                          |
| Output Transition Timing Ref. Voltages                 |         | V <sub>RL</sub> = 0.3V <sub>CC</sub> ; V <sub>RH</sub> = 0.7V <sub>CC</sub> |

Figure 6. AC Measurement I/O Waveform

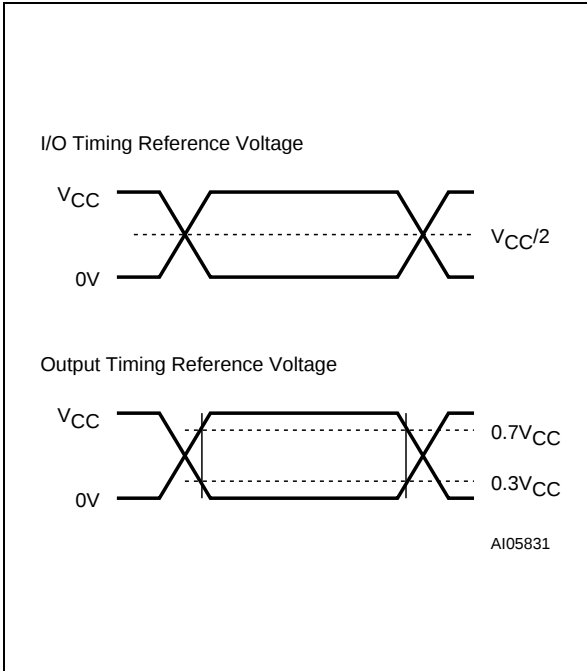


Figure 7. AC Measurement Load Circuit

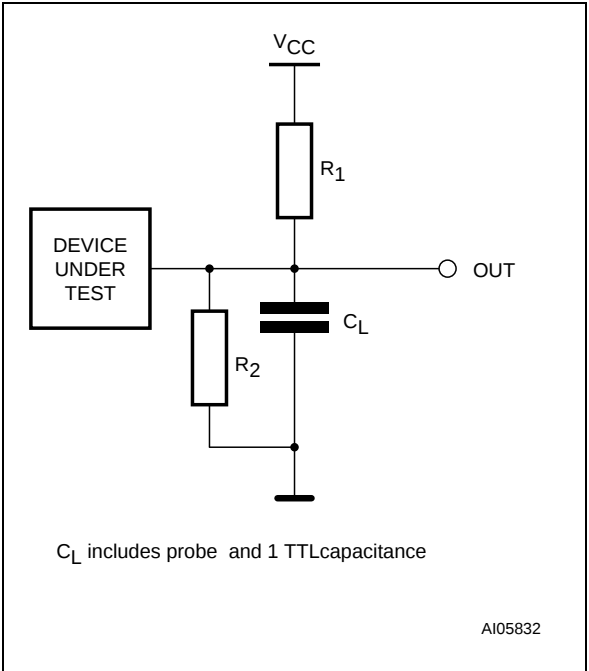


Table 5. Capacitance

| Symbol           | Parameter <sup>(1,2)</sup>                | Test Condition        | Min | Max | Unit |
|------------------|-------------------------------------------|-----------------------|-----|-----|------|
| C <sub>IN</sub>  | Input Capacitance on all pins (except DQ) | V <sub>IN</sub> = 0V  |     | 8   | pF   |
| C <sub>OUT</sub> | Output Capacitance                        | V <sub>OUT</sub> = 0V |     | 10  | pF   |

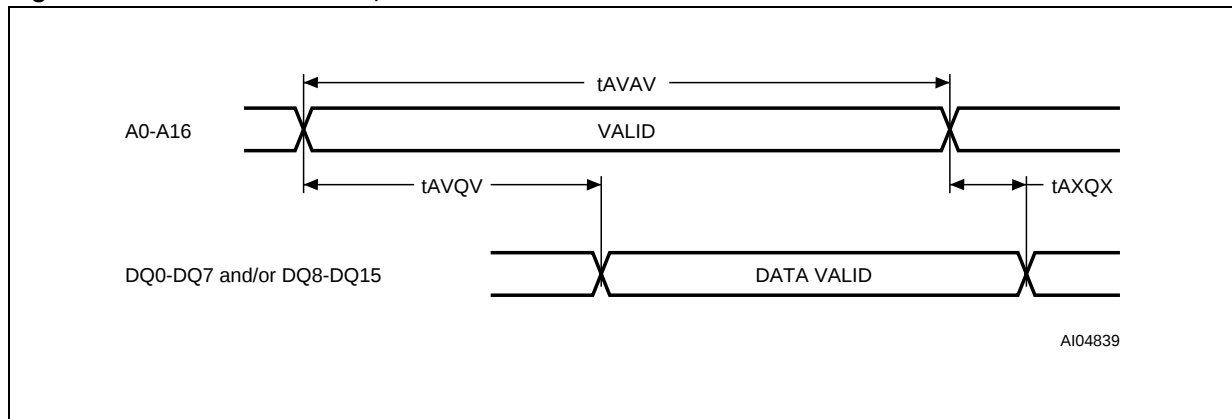
Note: 1. Sampled only, not 100% tested.  
 2. At T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 3.0V.

Table 6. DC Characteristics

| Symbol                            | Parameter                   | Test Condition                                                                                                               | Min  | Typ | Max                   | Unit |
|-----------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------|------|-----|-----------------------|------|
| I <sub>CC1</sub> <sup>(1,2)</sup> | Operating Supply Current    | V <sub>CC</sub> = 3.6V, f = 1/t <sub>AVAV</sub> ,<br>I <sub>OUT</sub> = 0mA                                                  | 70ns |     | 20                    | mA   |
|                                   |                             |                                                                                                                              | 55ns |     | 26                    | mA   |
| I <sub>CC2</sub> <sup>(3)</sup>   | Operating Supply Current    | V <sub>CC</sub> = 3.6V, f = 1MHz,<br>I <sub>OUT</sub> = 0mA                                                                  |      |     | 2                     | mA   |
| I <sub>SB</sub>                   | Standby Supply Current CMOS | V <sub>CC</sub> = 3.6V, f = 0,<br>$\overline{E} \geq V_{CC} - 0.2V$ or<br>$\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$ |      | 5   | 10                    | μA   |
| I <sub>LI</sub>                   | Input Leakage Current       | 0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                                                                       | −1   |     | 1                     | μA   |
| I <sub>LO</sub> <sup>(4)</sup>    | Output Leakage Current      | 0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>                                                                                      | −1   |     | 1                     | μA   |
| V <sub>IH</sub>                   | Input High Voltage          |                                                                                                                              | 2.2  |     | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub>                   | Input Low Voltage           |                                                                                                                              | −0.3 |     | 0.6                   | V    |
| V <sub>OH</sub>                   | Output High Voltage         | I <sub>OH</sub> = −1.0mA                                                                                                     | 2.4  |     |                       | V    |
| V <sub>OL</sub>                   | Output Low Voltage          | I <sub>OL</sub> = 2.1mA                                                                                                      |      |     | 0.4                   | V    |

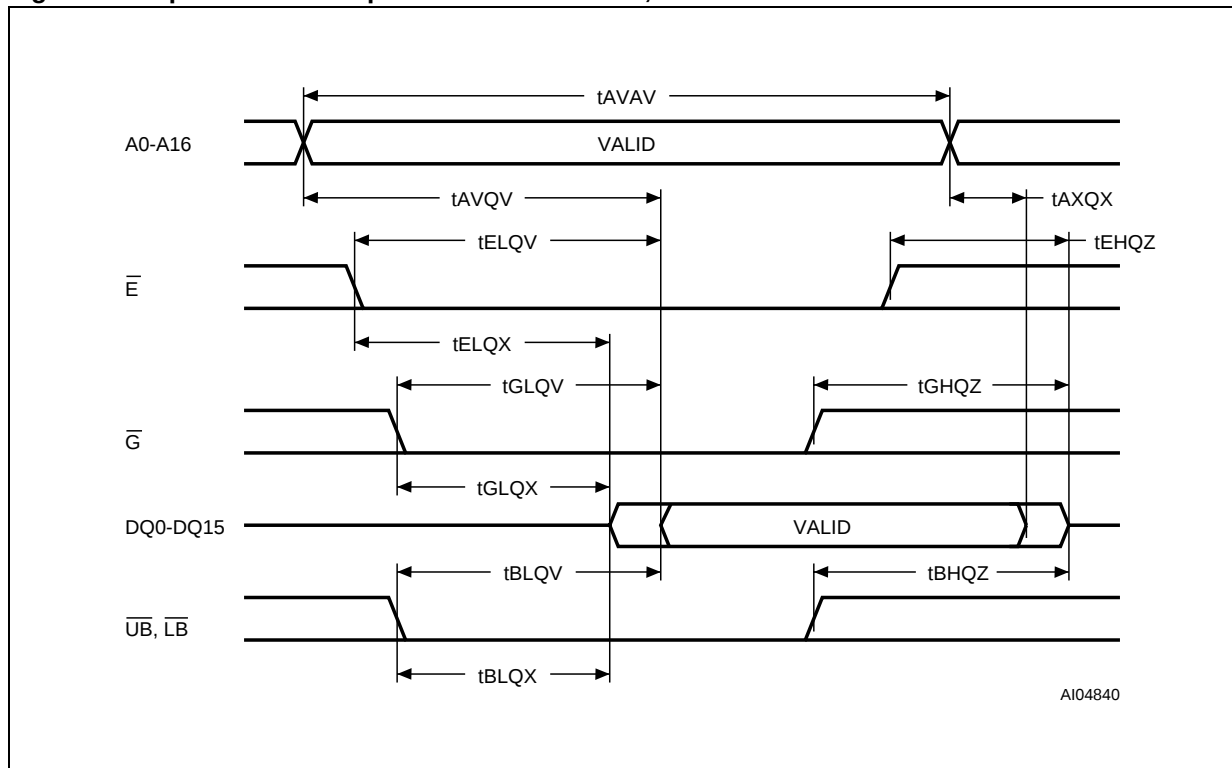
Note: 1. Average AC current, cycling at t<sub>AVAV</sub> minimum.  
 2.  $\overline{E} = V_{IL}$ ,  $\overline{LB}$  OR/AND  $\overline{UB} = V_{IL}$ , V<sub>IN</sub> = V<sub>IL</sub> OR V<sub>IH</sub>.  
 3.  $\overline{E} \leq 0.2V$ ,  $\overline{LB}$  OR/AND  $\overline{UB} \leq 0.2V$ , V<sub>IN</sub> ≤ 0.2V OR V<sub>IN</sub> ≥ V<sub>CC</sub> − 0.2V.  
 4. Output disabled.

Figure 8. Address Controlled, Read Mode AC Waveforms



Note:  $\overline{E}$  = Low,  $\overline{G}$  = Low,  $\overline{W}$  = High,  $\overline{UB}$  = Low and/or  $\overline{LB}$  = Low.

Figure 9. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.



Note: Write Enable ( $\overline{W}$ ) = High.

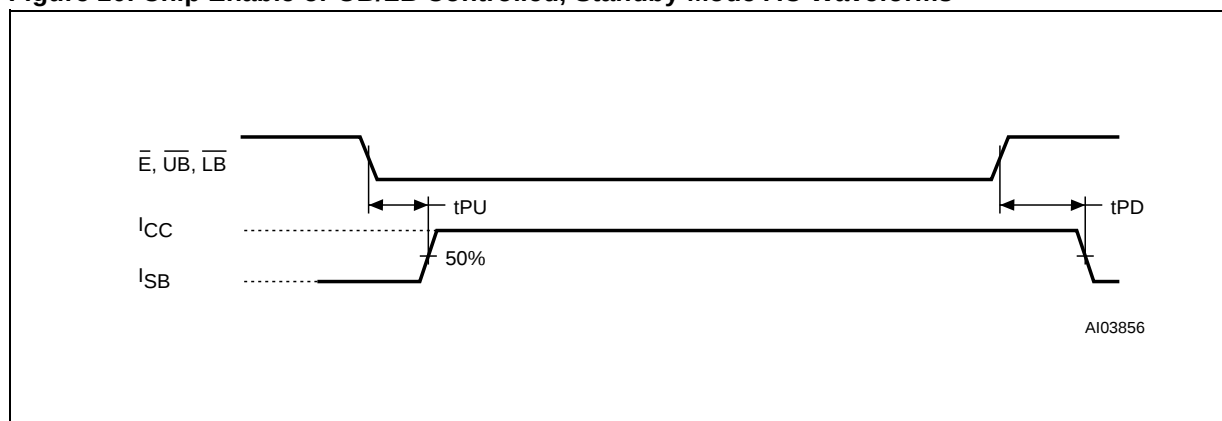
Figure 10. Chip Enable or  $\overline{UB}/\overline{LB}$  Controlled, Standby Mode AC Waveforms

Table 7. Read and Standby Mode AC Characteristics

| Symbol             | Parameter                                                       |     | M68AW128M |    | Unit |
|--------------------|-----------------------------------------------------------------|-----|-----------|----|------|
|                    |                                                                 |     | 55        | 70 |      |
| $t_{AVAV}$         | Read Cycle Time                                                 | Min | 55        | 70 | ns   |
| $t_{AVQV}$         | Address Valid to Output Valid                                   | Max | 55        | 70 | ns   |
| $t_{AXQX}^{(1)}$   | Data hold from address change                                   | Min | 5         | 5  | ns   |
| $t_{BHQZ}^{(2,3)}$ | Upper/Lower Byte Enable High to Output Hi-Z                     | Max | 20        | 25 | ns   |
| $t_{BLQV}$         | Upper/Lower Byte Enable Low to Output Valid                     | Max | 55        | 70 | ns   |
| $t_{BLQX}^{(1)}$   | Upper/Lower Byte Enable Low to Output Transition                | Min | 5         | 5  | ns   |
| $t_{EHQZ}^{(2,3)}$ | Chip Enable High to Output Hi-Z                                 | Max | 20        | 25 | ns   |
| $t_{ELQV}$         | Chip Enable Low to Output Valid                                 | Max | 55        | 70 | ns   |
| $t_{ELQX}^{(1)}$   | Chip Enable Low to Output Transition                            | Min | 5         | 5  | ns   |
| $t_{GHQZ}^{(2,3)}$ | Output Enable High to Output Hi-Z                               | Max | 20        | 25 | ns   |
| $t_{GLQV}$         | Output Enable Low to Output Valid                               | Max | 25        | 35 | ns   |
| $t_{GLQX}^{(2)}$   | Output Enable Low to Output Transition                          | Min | 5         | 5  | ns   |
| $t_{PD}$           | Chip Enable or $\overline{UB}/\overline{LB}$ High to Power Down | Max | 55        | 70 | ns   |
| $t_{PU}$           | Chip Enable or $\overline{UB}/\overline{LB}$ Low to Power Up    | Min | 0         | 0  | ns   |

Note: 1. Test conditions assume transition timing reference level =  $0.3V_{CC}$  or  $0.7V_{CC}$ .

2. At any given temperature and voltage condition,  $t_{GHQZ}$  is less than  $t_{GLQX}$ ,  $t_{BHQZ}$  is less than  $t_{BLQX}$  and  $t_{EHQZ}$  is less than  $t_{ELQX}$  for any given device.

3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 11. Write Enable Controlled, Write AC Waveforms

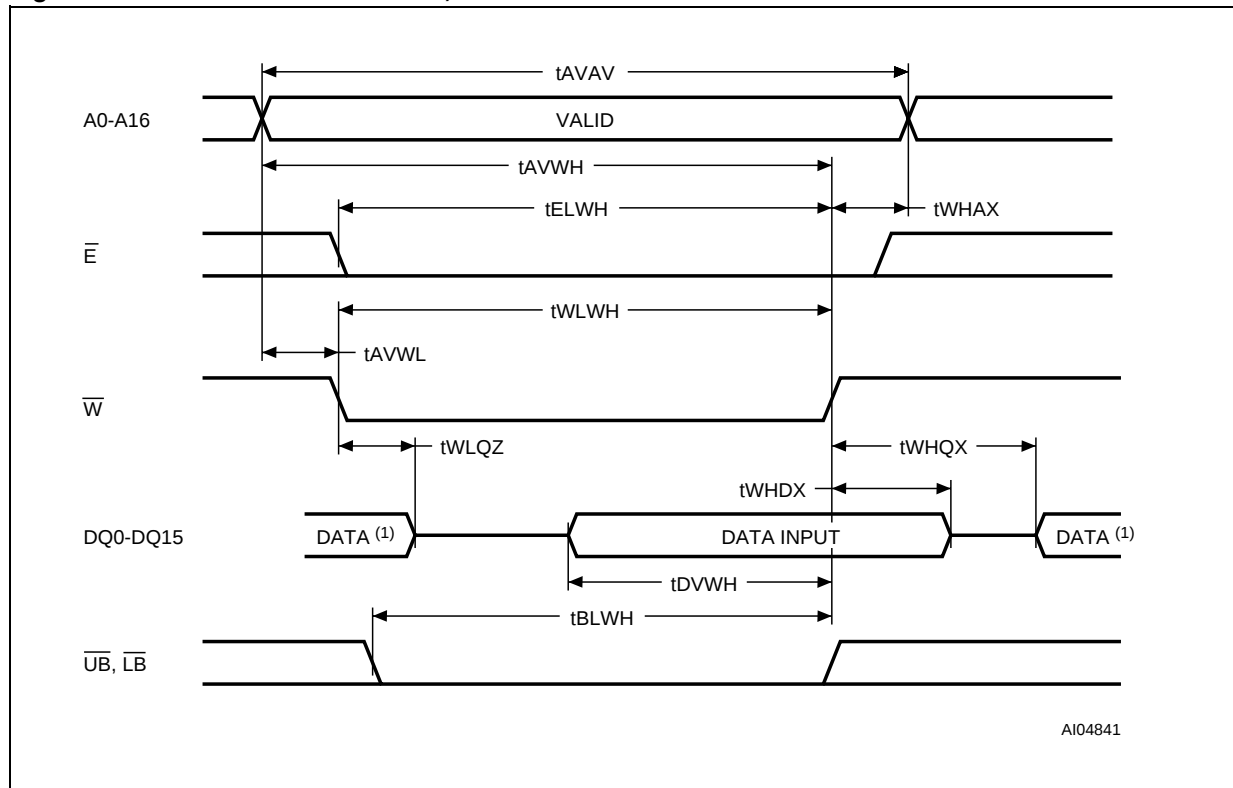


Figure 12. Chip Enable Controlled, Write AC Waveforms

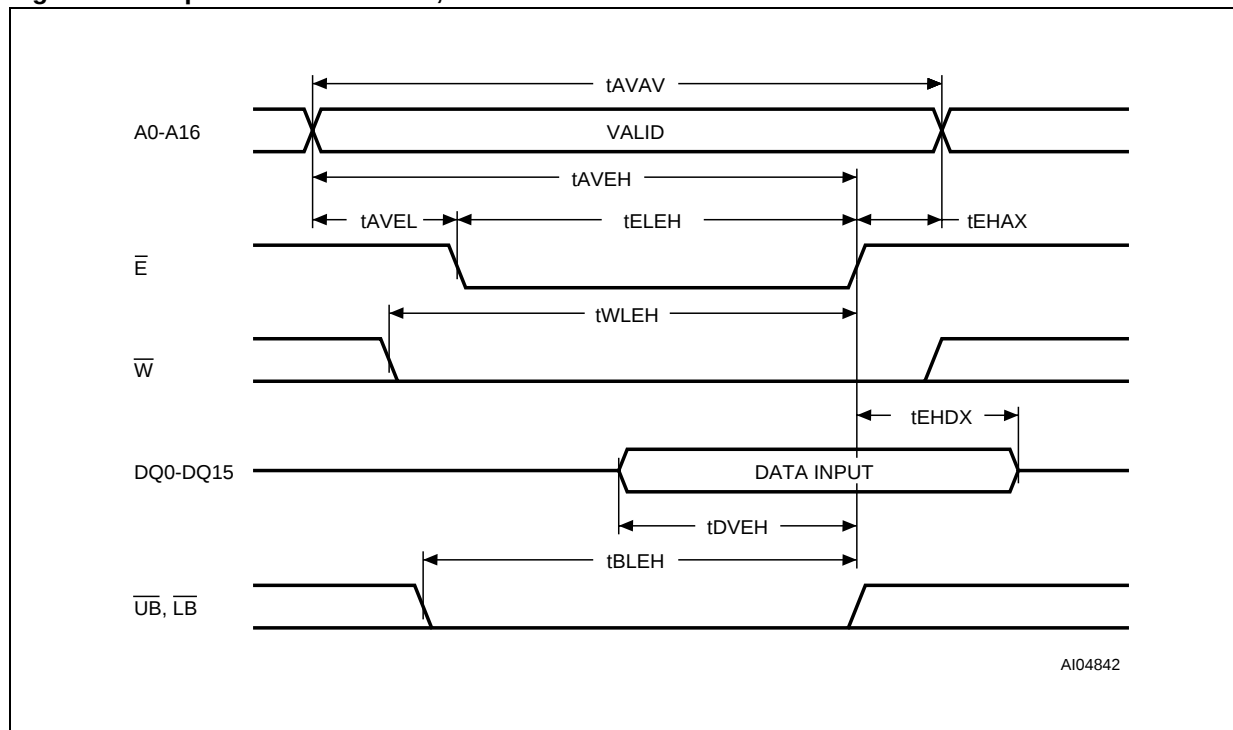
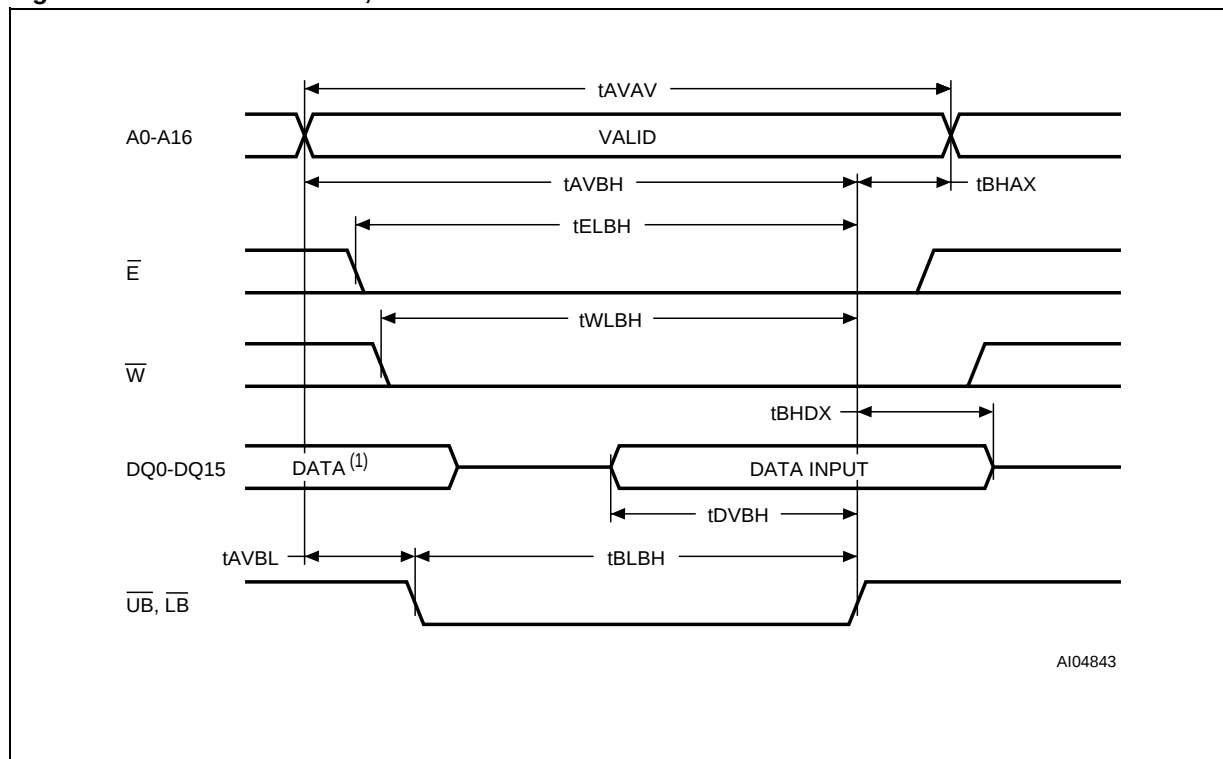


Figure 13.  $\overline{UB}/\overline{LB}$  Controlled, Write AC Waveforms

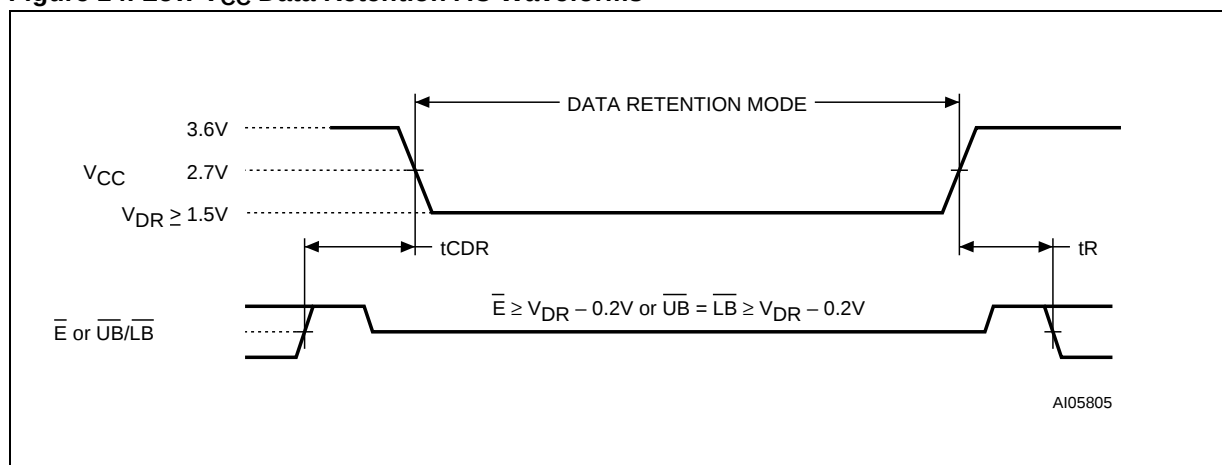
Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

Table 8. Write Mode AC Characteristics

| Symbol             | Parameter                                                                       |     | M68AW128M |    | Unit |
|--------------------|---------------------------------------------------------------------------------|-----|-----------|----|------|
|                    |                                                                                 |     | 55        | 70 |      |
| $t_{AVAV}$         | Write Cycle Time                                                                | Min | 55        | 70 | ns   |
| $t_{AVBH}$         | Address Valid to $\overline{LB}$ , $\overline{UB}$ High                         | Min | 45        | 60 | ns   |
| $t_{AVBL}$         | Address Valid to $\overline{LB}$ , $\overline{UB}$ Low                          | Min | 0         | 0  | ns   |
| $t_{AVEH}$         | Address Valid to Chip Enable High                                               | Min | 45        | 60 | ns   |
| $t_{AVEL}$         | Address valid to Chip Enable Low                                                | Min | 0         | 0  | ns   |
| $t_{AVWH}$         | Address Valid to Write Enable High                                              | Min | 45        | 60 | ns   |
| $t_{AVWL}$         | Address Valid to Write Enable Low                                               | Min | 0         | 0  | ns   |
| $t_{BHAX}$         | $\overline{LB}$ , $\overline{UB}$ High to Address Transition                    | Min | 0         | 0  | ns   |
| $t_{BHDX}$         | $\overline{LB}$ , $\overline{UB}$ High to Input Transition                      | Min | 0         | 0  | ns   |
| $t_{BLBH}$         | $\overline{LB}$ , $\overline{UB}$ Low to $\overline{LB}$ , $\overline{UB}$ High | Min | 45        | 60 | ns   |
| $t_{BLEH}$         | $\overline{LB}$ , $\overline{UB}$ Low to Chip Enable High                       | Min | 45        | 60 | ns   |
| $t_{BLWH}$         | $\overline{LB}$ , $\overline{UB}$ Low to Write Enable High                      | Min | 45        | 60 | ns   |
| $t_{DVBH}$         | Input Valid to $\overline{LB}$ , $\overline{UB}$ High                           | Min | 25        | 30 | ns   |
| $t_{DVEH}$         | Input Valid to Chip Enable High                                                 | Min | 25        | 30 | ns   |
| $t_{DVWH}$         | Input Valid to Write Enable High                                                | Min | 25        | 30 | ns   |
| $t_{EHAX}$         | Chip Enable High to Address Transition                                          | Min | 0         | 0  | ns   |
| $t_{EHDX}$         | Chip enable High to Input Transition                                            | Min | 0         | 0  | ns   |
| $t_{ELBH}$         | Chip Enable Low to $\overline{LB}$ , $\overline{UB}$ High                       | Min | 45        | 60 | ns   |
| $t_{ELEH}$         | Chip Enable Low to Chip Enable High                                             | Min | 45        | 60 | ns   |
| $t_{ELWH}$         | Chip Enable Low to Write Enable High                                            | Min | 45        | 60 | ns   |
| $t_{WHAX}$         | Write Enable High to Address Transition                                         | Min | 0         | 0  | ns   |
| $t_{WHDX}$         | Write Enable High to Input Transition                                           | Min | 0         | 0  | ns   |
| $t_{WHQX}^{(1)}$   | Write Enable High to Output Transition                                          | Min | 5         | 5  | ns   |
| $t_{WLBH}$         | Write Enable Low to $\overline{LB}$ , $\overline{UB}$ High                      | Min | 45        | 60 | ns   |
| $t_{WLEH}$         | Write Enable Low to Chip Enable High                                            | Min | 45        | 60 | ns   |
| $t_{WLQZ}^{(1,2)}$ | Write Enable Low to Output Hi-Z                                                 | Max | 20        | 20 | ns   |
| $t_{WLWH}$         | Write Enable Low to Write Enable High                                           | Min | 45        | 60 | ns   |

Note: 1. At any given temperature and voltage condition,  $t_{WLQZ}$  is less than  $t_{WHQX}$  for any given device.

2. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 14. Low  $V_{CC}$  Data Retention AC WaveformsTable 9. Low  $V_{CC}$  Data Retention Characteristics

| Symbol            | Parameter                              | Test Condition                                                                                                 | Min        | Typ | Max | Unit    |
|-------------------|----------------------------------------|----------------------------------------------------------------------------------------------------------------|------------|-----|-----|---------|
| $I_{CCDR}^{(1)}$  | Supply Current (Data Retention)        | $V_{CC} = 1.5V, \bar{E} \geq V_{CC} - 0.2V$ or $\overline{UB} = \overline{LB} \geq V_{CC} - 0.2V, f = 0^{(3)}$ |            | 4.5 | 9   | $\mu A$ |
| $t_{CDR}^{(1,2)}$ | Chip Deselected to Data Retention Time |                                                                                                                | 0          |     |     | ns      |
| $t_R^{(2)}$       | Operation Recovery Time                |                                                                                                                | $t_{AVAV}$ |     |     | ns      |
| $V_{DR}^{(1)}$    | Supply Voltage (Data Retention)        | $\bar{E} \geq V_{CC} - 0.2V$ or $\overline{UB} = \overline{LB} \geq V_{CC} - 0.2V, f = 0$                      | 1.5        |     |     | V       |

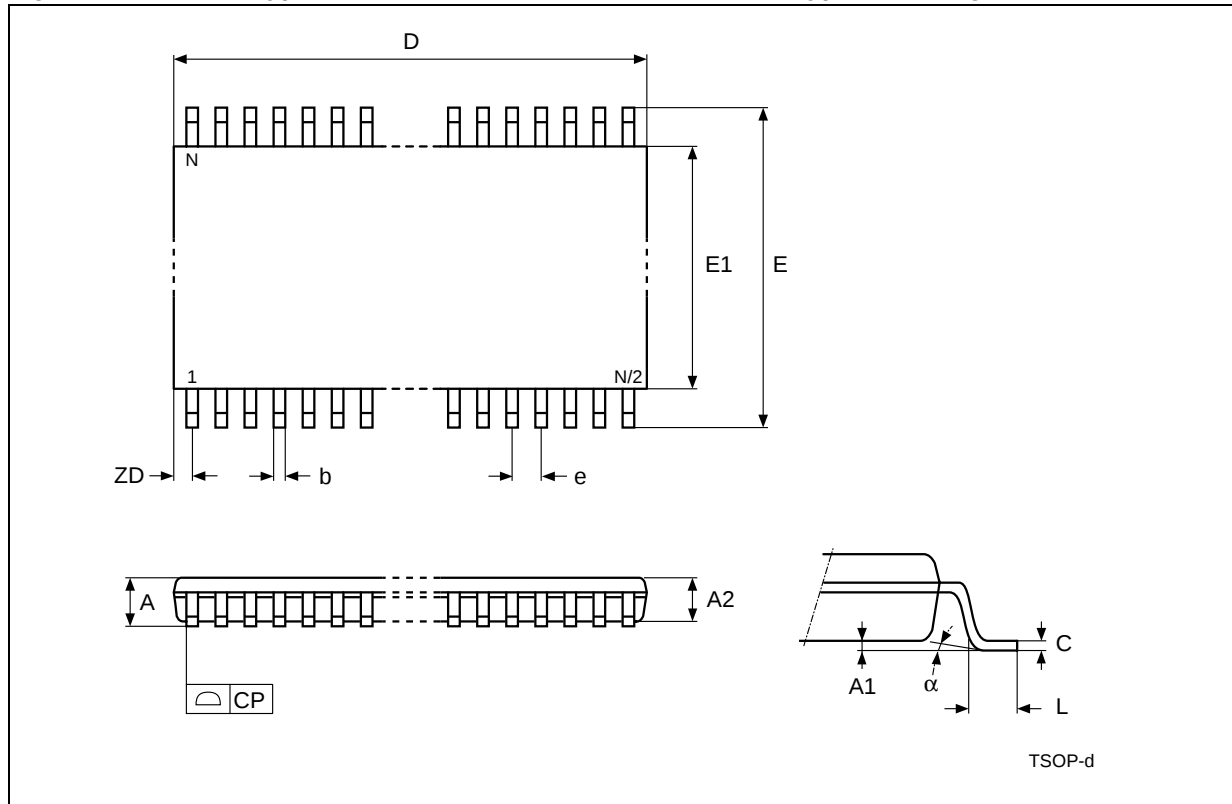
Note: 1. All other Inputs at  $V_{IH} \geq V_{CC} - 0.2V$  or  $V_{IL} \leq 0.2V$ .

2. Tested initially and after any design or process changes that may affect these parameters.  $t_{AVAV}$  is Read cycle time.

3. No input may exceed  $V_{CC} + 0.2V$ .

## PACKAGE MECHANICAL

Figure 15. TSOP44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Outline

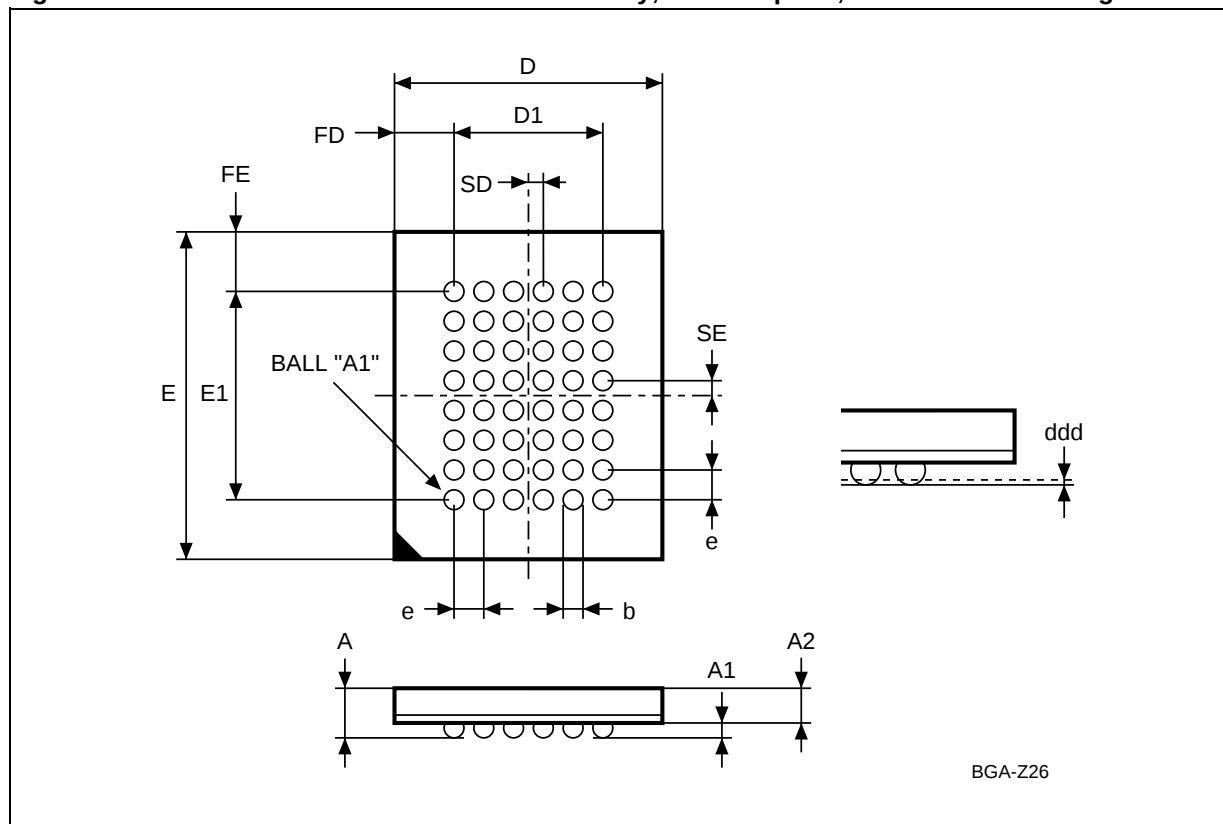


Note: Drawing is not to scale.

Table 10. TSOP 44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Mechanical Data

| Symbol   | millimeters |       |       | inches |        |        |
|----------|-------------|-------|-------|--------|--------|--------|
|          | Typ         | Min   | Max   | Typ    | Min    | Max    |
| A        |             |       | 1.200 |        |        | 0.0472 |
| A1       |             | 0.050 | 0.150 |        | 0.0020 | 0.0059 |
| A2       |             | 0.950 | 1.050 |        | 0.0374 | 0.0413 |
| b        | 0.350       |       |       | 0.0138 |        |        |
| c        |             | 0.120 | 0.210 |        | 0.0047 | 0.0083 |
| D        | 18.410      | —     | —     | 0.7248 | —      | —      |
| e        | 0.800       | —     | —     | 0.0315 | —      | —      |
| E        | 11.760      | —     | —     | 0.4630 | —      | —      |
| E1       | 10.160      | —     | —     | 0.4000 | —      | —      |
| L        | 0.500       | 0.400 | 0.600 | 0.0197 | 0.0157 | 0.0236 |
| ZD       | 0.805       | —     | —     | 0.0317 | —      | —      |
| $\alpha$ |             | 0°    | 5°    |        | 0°     | 5°     |
| CP       |             |       | 0.100 |        |        | 0.0039 |
| N        | 44          |       |       | 44     |        |        |

Figure 16. TFBGA48 6x8mm - 6x8 Active Ball Array, 0.75mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 11. TFBGA48 6x8mm - 6x8 Active Ball Array, 0.75mm pitch, Package Mechanical Data

| Symbol | millimeters |       |       | inches |        |        |
|--------|-------------|-------|-------|--------|--------|--------|
|        | Typ         | Min   | Max   | Typ    | Min    | Max    |
| A      |             |       | 1.200 |        |        | 0.0472 |
| A1     |             | 0.260 |       |        | 0.0102 |        |
| A2     |             |       | 0.900 |        |        | 0.0354 |
| b      |             | 0.350 | 0.450 |        | 0.0138 | 0.0177 |
| D      | 6.000       | 5.900 | 6.100 | 0.2362 | 0.2323 | 0.2402 |
| D1     | 3.750       | —     | —     | 0.1476 | —      | —      |
| ddd    |             |       | 0.100 |        |        | 0.0039 |
| E      | 8.000       | 7.900 | 8.100 | 0.3150 | 0.3110 | 0.3189 |
| E1     | 5.250       | —     | —     | 0.2067 | —      | —      |
| e      | 0.750       | —     | —     | 0.0295 | —      | —      |
| FD     | 1.125       | —     | —     | 0.0443 | —      | —      |
| FE     | 1.375       | —     | —     | 0.0541 | —      | —      |
| SD     | 0.375       | —     | —     | 0.0148 | —      | —      |
| SE     | 0.375       | —     | —     | 0.0148 | —      | —      |

## PART NUMBERING

**Table 12. Ordering Information Scheme**

|                                                                                                                                                                |          |   |   |    |    |   |   |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|---|---|----|----|---|---|
| Example:                                                                                                                                                       | M68AW128 | M | L | 55 | ZB | 6 | T |
| <b>Device Type</b>                                                                                                                                             |          |   |   |    |    |   |   |
| M68                                                                                                                                                            |          |   |   |    |    |   |   |
| <b>Mode</b>                                                                                                                                                    |          |   |   |    |    |   |   |
| A = Asynchronous                                                                                                                                               |          |   |   |    |    |   |   |
| <b>Operating Voltage</b>                                                                                                                                       |          |   |   |    |    |   |   |
| W = 2.7 to 3.6V                                                                                                                                                |          |   |   |    |    |   |   |
| <b>Array Organization</b>                                                                                                                                      |          |   |   |    |    |   |   |
| 128 = 2 Mbit (128K x16)                                                                                                                                        |          |   |   |    |    |   |   |
| <b>Option 1</b>                                                                                                                                                |          |   |   |    |    |   |   |
| M = 1 Chip Enable; Write and Standby from $\overline{UB}$ and $\overline{LB}$                                                                                  |          |   |   |    |    |   |   |
| <b>Option 2</b>                                                                                                                                                |          |   |   |    |    |   |   |
| L = L-Die                                                                                                                                                      |          |   |   |    |    |   |   |
| <b>Speed Class</b>                                                                                                                                             |          |   |   |    |    |   |   |
| 55 = 55 ns<br>70 = 70 ns                                                                                                                                       |          |   |   |    |    |   |   |
| <b>Package</b>                                                                                                                                                 |          |   |   |    |    |   |   |
| ND = TSOP 44 Type II<br>ZB = TFBGA48: 0.75 mm pitch                                                                                                            |          |   |   |    |    |   |   |
| <b>Operative Temperature</b>                                                                                                                                   |          |   |   |    |    |   |   |
| 1 = 0 to 70°C<br>6 = -40 to 85°C                                                                                                                               |          |   |   |    |    |   |   |
| <b>Shipping</b>                                                                                                                                                |          |   |   |    |    |   |   |
| Blank = Standard Packing<br>T = Tape & Reel Packing<br>E = Lead-free and RoHS Package, Standard Packing<br>F = Lead-free and RoHS Package, Tape & Reel Packing |          |   |   |    |    |   |   |

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

## REVISION HISTORY

**Table 13. Document Revision History**

| Date         | Version | Revision Details                                                                                                                                                                                                                   |
|--------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| July 2001    | -01     | First Issue.                                                                                                                                                                                                                       |
| 10-Dec-2001  | -02     | Document completely revised.                                                                                                                                                                                                       |
| 18-Feb-2002  | -03     | Tables 2, 7, 8 and 9 clarified.                                                                                                                                                                                                    |
| 25-Mar-2002  | -04     | Read and Standby Mode AC Characteristics table clarified (Table 7).<br>Low V <sub>CC</sub> Data Retention Characteristics table clarified (Table 9).                                                                               |
| 17-June-2002 | -05     | Minor changes.                                                                                                                                                                                                                     |
| 09-Oct-2002  | 5.1     | Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 05 equals 5.0).<br>Part number modified. |
| 20-Apr-2004  | 6.0     | Lead-free package version added.                                                                                                                                                                                                   |
| 24-Sep-2004  | 7.0     | t <sub>PU</sub> and t <sub>PD</sub> updated in Table 7.                                                                                                                                                                            |

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