ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE2708
Integrated Circuit
NMOS, 8K UV EPROM, 450ns

Description:

The NTE2708 is an ultra–violet light–erasable, electrically programmable read only memory. It has 8, 192 bits organized as 1024 words of 8–bit length. This device is fabricated using N–channel silicon–gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull–up resistors. Each output can drive one Series 74 or 74LS TTL circuit without external resistors. The data outputs for the NTE2708 are three–state for OR tying multiple devices on a common bus.

This EPROM is designed for high–density fixed memory applications where fast turn arounds and/or program changes are required. This device is designed for operation from 0° to +70°C and is supplied in a 24–Lead DIP package for insertion in mounting–hole rows on 600–mil (15.2 mm) centers.

Features:

- 1024 X 8 Organization
- All Inputs and Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Performance Ranges:
  Max Access: 450ns
  Min Cycle: 450ns
- 3–State Outputs for OR–Ties
- 8–Bit Output
- Plug–Compatible Pin–Outs Allowing Interchangeability

Absolute Maximum Ratings: (T_A = 0° to +70°C, Note 1 unless otherwise specified)

Supply Voltage, V_{CC} (Note 2) . . . . . –0.3 to +15V
Supply Voltage, V_{DD} (Note 2) . . . . . –0.3 to +20V
Supply Voltage, V_{SS} (Note 2) . . . . . –0.3 to +15V
All Input Voltage (except program) (Note 2) . . . . . –0.3 to +20V
Program Input (Note 2) . . . . . –0.3 to +35V
Output Voltage (operating, with respect to V_{SS}) . . . . . –2 to +7V
Operating free–air temperature range . . . . . 0°C to 70°C
Storage temperature Range . . . . . –55°C to 125°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permenant damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this specification is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Note 2. Under absolute maximum ratings, voltage values are with respect to the most–negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

Operation (Read Mode):

Address (A0–A9)

The address–valid interval determines the device cycle time. The 10–bit positive–logic address is decoded on–chip to select one of the 1024 words of 8–bit length in the memory array. A0 is the least–significant bit and A9 is the most–significant bit of the words address.

Chip Select, Program Enable [$\overline{CS}$ (PE)]

When the chip select is low, all eight outputs are enabled and the eight–bit addressed word can be read. When the chip select is high, all eight outputs are in a high–impedance state.

Data Out (Q1–Q8)

The chip must be selected before the eight–bit outputs word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three–state outputs are in a high–impedance state. The outputs will drive TTL circuits without external components.

Program

The program pin must be held below V_{CC} in the read mode.

Operation (Program Mode):

Erase

Before programming, the NTE2708 is erased by exposing the chip through the transparent lid to high–intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity x exposure time) is fifteen watt–seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the “1” state.

Programming

Programming consists of successively depositing a small amount of charge to a selected memory cell that is to be changed from the erased high state to the low state. A low can be changed to a high only by erasure. Programming is normally accomplished on a PROM or EPROM Programmer. Programming must be done at room temperature (+25°C) only.

To Start Programming

First bring the $\overline{CS}$ (PE) pin to +12V to disable the outputs and convert them to inputs. This pin is held high for the duration of the programming sequence. The first word to be programmed is addressed (it is customary to begin with the “0” address) and the data to be stored is placed on the Q1–Q8 program inputs. Then a +25V program pulse is applied to the program pin. After 0.1 to 1.0 milliseconds the program pin is brought back to 0V. After at least one microsecond the word address is sequentially changed to the next location, the new data is set up and the program pulse is applied.

Programming continues in this manner until all words have been programmed. This constitutes one of N program loop. The entire sequence is then repeated N times with N x $t_{W(PR)} \geq 100$ ms. Thus, if $t_{W(PR)} = 1$ ms; then N = 100, the minimum number of program loops required to program the EPROM.

To Stop Programming

After cycling through the N program loops, the last program pulse is brought to 0V, then Program Enable [$\overline{CS}$ (PE)] is brought to V_{IL} which takes the device out of the program mode. The data supplied by the programmer must be removed before the address is changed since the program inputs are now data outputs and change of address could cause a voltage conflict on the output buffer. Q1–Q8 outputs are invalid up to 10 microseconds after the program enable pin is brought from $V_{IH(PE)}$ to V_{IL}.

Recommended Operating Conditions:

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{BB}	–4.75	–5	–5.25	V
	V_{CC}	4.75	5	5.25	V
	V_{DD}	11.4	12	12.6	V
	V_{SS}	–	0	–	V
High–Level Input Voltage (Except Program & Program Enable)	V_{IH}	2.4	–	V_{CC}+1	V
High–Level Program Enable Input Voltage	$V_{IH(PE)}$	11.4	12	12.6	V
High–Level Program Input Voltage	$V_{IH(PR)}$	25	26	27	V
Low–Level Input Voltage (Except Program)	V_{IL}	V_{SS}	–	0.65	V
Low–Level Program Input Voltage V_{IL}(PR) max ≤ V_{IH}(PR) –25V	$V_{IL(PR)}$	V_{SS}	–	1	V
High–Level Program Pulse Input Current (Sink)	$I_{IH(PR)}$	–	–	40	mA
Low–Level Program Pulse Input Current (Source)	$I_{IL(PR)}$	–	–	3	mA
Operating Free–Air Temperature	T_A	0	–	70	°C

Electrical Characteristics: (T_A = 0° to +70°C, Note 3 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High–level Output Voltage	V_{OH}	I_{OH} = –100µA	3.7	–	–	V
Low–level Output Voltage	V_{OL}	I_{OH} = –1mA	2.4	–	–	V
Input Current (Leakage)	I_I	I_{OL} = 1.6mA	–	–	0.45	µA
Output Current (Leakage)	I_O	$\overline{CS}$(PE) = 5V	–	1	10	µA
Supply Current from V_{BB}	I_{BB}	T_A = 70°C	–	30	45	mA
Supply Current from V_{CC}	I_{CC}	All Inputs High, $\overline{CS}$(PE) = 5V, T_A = 0°C (Worst Case)	–	6	10	mA
Supply Current from V_{DD}	I_{DD}		–	50	65	mA
Power Dissipation	$P_{D(AV)}$		–	–	800	mW

Note 3. All typical values are at T_A = 25°C and nominal voltages.

Capacitance: (T_A = 0° to +70°C, f = 1MH$_Z$, Note 3 unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	4	6	pF
Output Capacitance	C_O	–	8	12	pF

Note 3. All typical values are at T_A = 25°C and nominal voltages.

Switching Characteristics: (T_A = 0° to +70°C unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
Access Time from Address	C_L = 100 pF, 1 Series 74 TTL load, $t_{f(CS)}$, $t_{f(ad)}$ = 20ns	–	–	450	ns
Access Time from $\overline{CS}$		–	–	120	ns
Output Invalid from Address Change		0	–	–	ns
Output Disable Time (Note 4)		0	–	120	ns
Read Cycle Time		450	–	–	ns

Note 4. Value calculated from 0.5 volt delta to measured output level.

T_A = +25°C Program Characteristics Over Recommended Supply Voltage Range:

Parameter	Symbol	Min	Typ	Max	Unit
Pulse Width, Program Pulse	$t_{w(PR)}$	0.1	–	1.0	ms
Transition Times (Except Program Pulse)	t_T	–	–	20	ns
Transition Times, Program Pulse	$t_{T(PR)}$	50	–	2000	ns
Address Setup Time	$t_{su(ad)}$	10	–	–	µs
Data Setup Time	$t_{su(da)}$	10	–	–	µs
Program Enable Setup Time	$t_{su(PE)}$	10	–	–	µs
Address Hold Time	$t_{h(ad)}$	1000	–	–	ns
Address Hold Time after Program Input Data Stopped	$t_{h(ad, da R)}$	0	–	–	ns
Data Hold Time	$t_{h(da)}$	1000	–	–	ns
Program Enable Hold Time	$t_{h(PE)}$	500	–	–	ns
Delay Time, $\overline{CS}$ (PE) Low to Address Change	$t_{CL, adX}$	0	–	–	ns

Pin Connection Diagram