Data sheet acquired from Harris Semiconductor
SCHS209A

February 1998 - Revised July 2000

CD74HC4067, CD74HCT4067

High-Speed CMOS Logic 16-Channel Analog Multiplexer/Demultiplexer

Features

- **Wide Analog Input Voltage Range**
- **Low "ON" Resistance**
  - **V_{CC} = 4.5V . . . . . 70Ω (Typ)**
  - **V_{CC} = 6V . . . . . 60Ω (Typ)**
- **Fast Switching and Propagation Speeds**
- **"Break-Before-Make" Switching. . . . . 6ns (Typ) at 4.5V**
- **Available in Both Narrow and Wide-Body Plastic Packages**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{O}C to 125^{O}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The CD74HC4067 and CD74HCT4067 devices are digitally controlled analog switches that utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range. They are bidirectional switches thus allowing any analog input to be used as an output and vice-versa. The switches have low "on" resistance and low "off" leakages. In addition, these devices have an enable control which when high will disable all switches to their "off" state.

Ordering Information

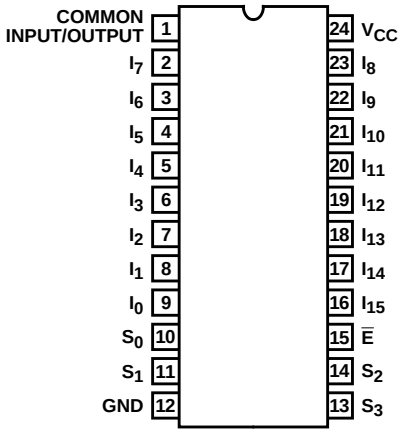
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE
CD74HC4067E	-55 to 125	24 Ld PDIP
CD74HC4067M	-55 to 125	24 Ld SOIC
CD74HC4067SM	-55 to 125	24 Ld SSOP
CD74HCT4067M	-55 to 125	24 Ld SOIC

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die is available that meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

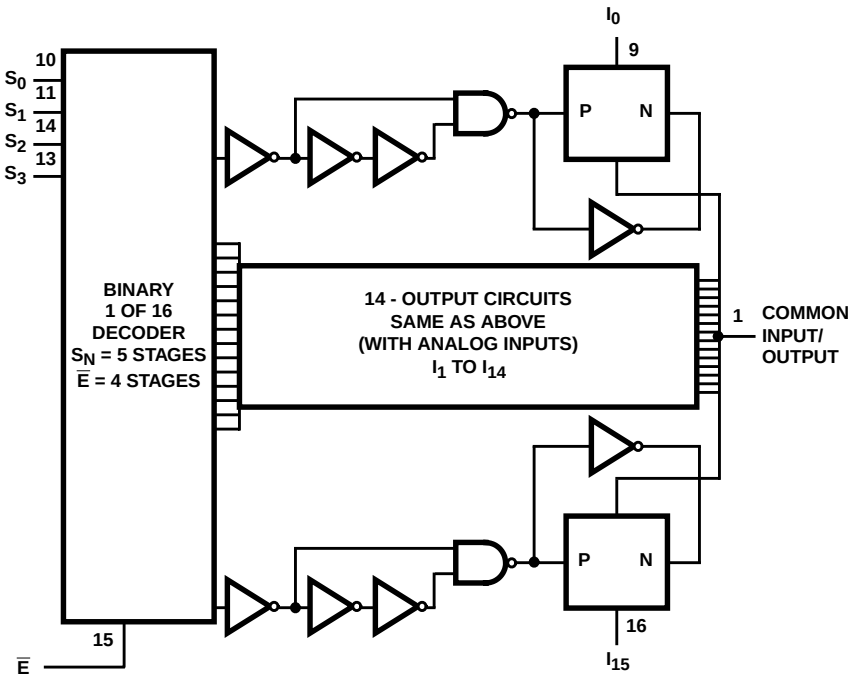
Pinout

CD74HC4067, CD74HCT4067
(PDIP, SOIC, SSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



TRUTH TABLE

S0	S1	S2	S3	$\overline{E}$	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

NOTE:
H = High Level
L = Low Level
X = Don't Care

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}
(Voltages Referenced to Ground) . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, I_O
For -0.5V < V_O < V_{CC} + 0.5V . . . . . ±25mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^oC/W$)
E Package	67
M Package	46
SM Package	63

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is calculated in accordance with JESD 51.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
Maximum "ON" Resistance I_O = 1mA	R_{ON}	V_{CC} or GND	V_{CC} or GND	4.5	-	70	160	-	200	-	240	Ω
				6	-	60	140	-	175	-	210	Ω
		V_{CC} to GND	V_{CC} to GND	4.5	-	90	180	-	225	-	270	Ω
				6	-	80	160	-	200	-	240	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR_{ON}	-	-	4.5	-	10	-	-	-	-	-	Ω
				6	-	8.5	-	-	-	-	-	Ω
Switch "Off" Leakage Current 16 Channels	I_{IZ}	$\overline{E}$ = V_{CC}	V_{CC} or GND	6	-	-	±0.8	-	±8	-	±8	µA
Logic Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current I_O = 0mA	I_{CC}	V_{CC} or GND	-	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5	-	-	0.8	-	0.8	-	0.8	V
Maximum "ON" Resistance I_O = 1mA	R_{ON}	V_{CC} or GND	V_{CC} or GND	4.5	-	70	160	-	200	-	240	Ω
		V_{CC} to GND	V_{CC} to GND	4.5	-	90	180	-	225	-	270	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR_{ON}	-	-	4.5	-	10	-	-	-	-	-	Ω
Switch "Off" Leakage Current 16 Channels	I_{IZ}	$\overline{E} = V_{CC}$	V_{CC} or GND	6	-	-	±0.8	-	±8	-	±8	µA
Logic Input Leakage Current	I_I	V_{CC} or GND (Note 5)	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	-	6	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 4)	V_{CC} -2.1	-	-	-	100	360	-	450	-	490	µA

NOTES:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.
5. Any voltage between V_{CC} and GND.

HCT Input Loading Table

INPUT	UNIT LOAD
S_0 - S_3	0.5
$\overline{E}$	0.3

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay Time Switch In to Out	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
		C_L = 15pF	5	-	6	-	-	-	-	-	ns
Switch Turn On $\overline{E}$ to Out	t_{PZH}, t_{PZL}	C_L = 50pF	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	69	-	83	ns
			6	-	-	47	-	59	-	71	ns
		C_L = 15pF	5	-	23	-	-	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Switch Turn On Sn to Out	t_{PZH}, t_{PZL}	C_L = 50pF	2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
			6	-	-	51	-	64	-	76	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
Switch Turn Off $\overline{E}$ to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	69	-	83	ns
			6	-	-	47	-	59	-	71	ns
		C_L = 15pF	5	-	23	-	-	-	-	-	ns
Switch Turn Off Sn to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	2	-	-	290	-	365	-	435	ns
			4.5	-	-	58	-	73	-	87	ns
			6	-	-	49	-	62	-	74	ns
		C_L = 50pF	5	-	21	-	-	-	-	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 6, 7)	C_{PD}	-	5	-	93	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay Time Switch In to Out	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C_L = 15pF	5	-	6	-	-	-	-	-	ns
Switch Turn On $\overline{E}$ to Out	t_{PZH}, t_{PZL}	C_L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
Switch Turn On Sn to Out	t_{PZH}, t_{PZL}	C_L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
Switch Turn Off $\overline{E}$ to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	5	-	23	-	-	-	-	-	ns
Switch Turn Off Sn to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	4.5	-	-	58	-	73	-	87	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 6, 7)	C_{PD}	-	5	-	96	-	-	-	-	-	pF

NOTES:

6. C_{PD} is used to determine the dynamic power consumption, per package.
7. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	V_{CC} (V)	HC/HCT	UNITS
Switch Frequency Response Bandwidth at -3dB (Figure 2)	Figure 4, Notes 8, 9	4.5	89	MHz
Sine Wave Distortion	Figure 5	4.5	0.051	%
Feedthrough Noise $\overline{E}$ to Switch	Figure 6, Notes 9, 10	4.5	TBE	mV
Feedthrough Noise S to Switch			TBE	mV
Switch "OFF" Signal Feedthrough (Figure 3)	Figure 7	4.5	-75	dB
Switch Input Capacitance, C_S		-	5	pF
Common Capacitance, C_{COM}		-	50	pF

NOTES:

8. Adjust input level for 0dBm at output, f = 1MHz.
9. V_{IS} is centered at $V_{CC}/2$.
10. Adjust input for 0dBm at V_{IS}.

Typical Performance Curves

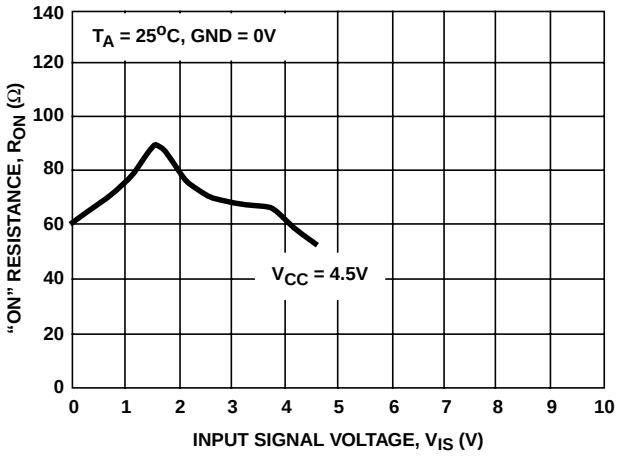


FIGURE 1. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

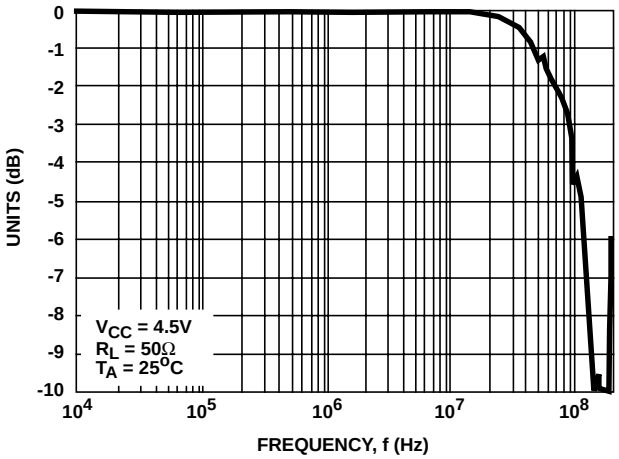


FIGURE 2. TYPICAL SWITCH FREQUENCY RESPONSE

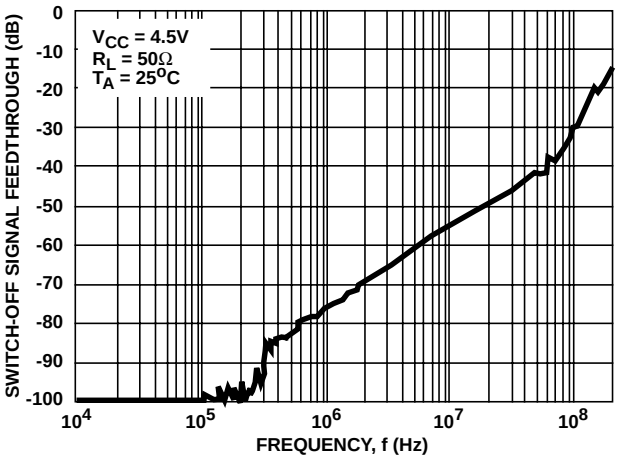


FIGURE 3. TYPICAL SWITCH-OFF SIGNAL FEEDTHROUGH vs FREQUENCY

Analog Test Circuits

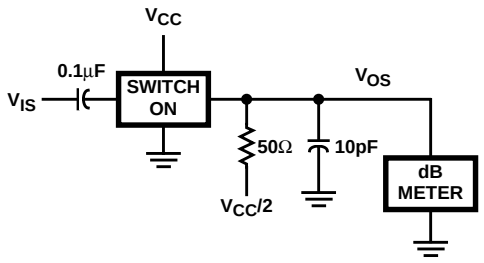


FIGURE 4. FREQUENCY RESPONSE TEST CIRCUIT

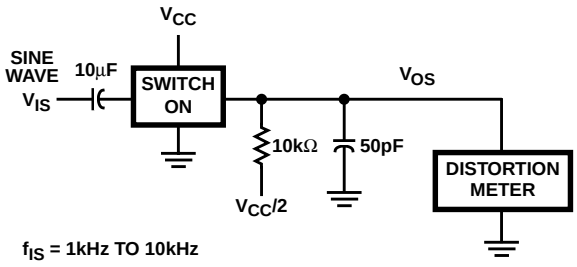


FIGURE 5. SINE WAVE DISTORTION TEST CIRCUIT

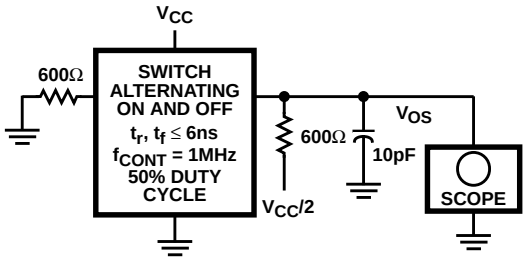


FIGURE 6. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

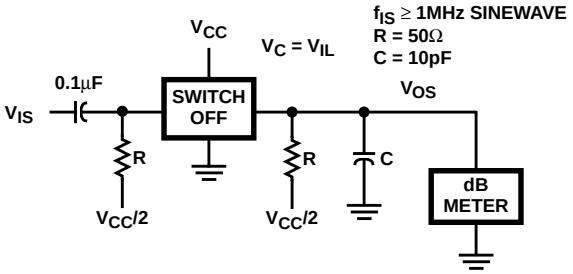


FIGURE 7. SWITCH OFF SIGNAL FEEDTHROUGH TEST CIRCUIT

Test Circuits and Waveforms

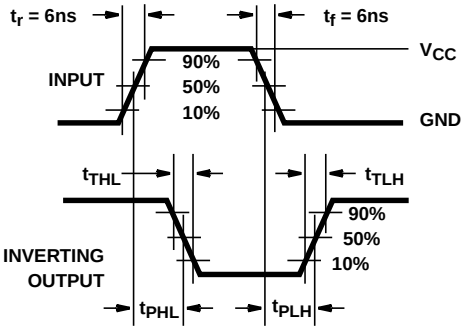


FIGURE 8. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

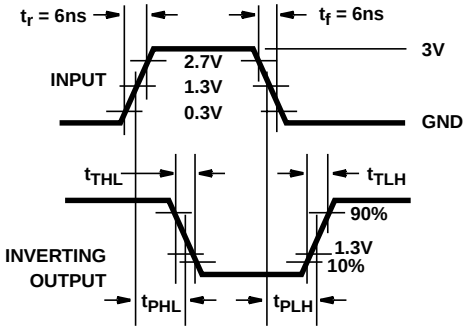


FIGURE 9. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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